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Extending Bridge++ Lattice Simulation Code to Vector Processors

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We report our recent extension of Bridge++, a general-purpose code set for numerical simulations of lattice gauge theories, to the latest vector processor, NEC SX-Aurora TSUBASA. The Bridge++ project aims at developing a readable, extensible, and portable workbench with sufficiently high performance. Based on the code set we investigate fast algorithms for parallel numerical calculations, and code optimization techniques. While the major target of the code set has been cluster systems with scalar processors, we are now extending it to various architectures such as GPUs and processors with wide SIMD registers. In this talk, we introduce our framework for accommodating these platforms, and present the optimization for the vector processor.

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