Status of Belle II DAQ upgrade & our contributions

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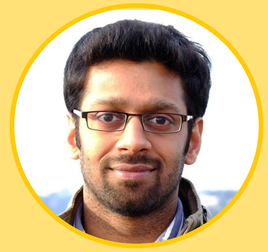


Abstract

To meet the future luminosity projected data rates at Belle II, its data acquisition system needs to be upgraded. By *replacing the existing COPPER electronics readout boards* with **new high-density PCI-express-based boards**, we not only prepare for the future operation of SuperKEKB but also *get rid of the outdated hardware and highly simplify the entire DAQ system*. Planned development & the current status of Belle II DAQ Upgrade project is presented.

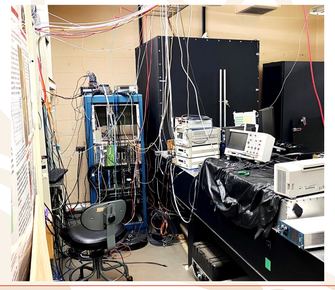
Why upgrade?

- **Outdated hardware**, several **discontinued parts** preventing future repair
- Only **marginally support projected data rates** as SuperKEKB approaches its target luminosity
- **High CPU usage** in current readout boards
- **COPPERs are the next bottleneck (~1 Gbps)**
- **Vast electronics**: ~600 HSLBs, ~200 COPPER boards, several FTSWs, etc.

Test benches at UH & KEK

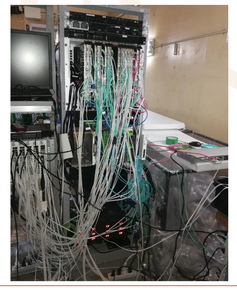
At UHM

✓ 1 PCIe40 board
✓ TOP & KLM test bench
✓ Few dummy FEE



At KEK

➢31 PCIe40 boards, for upgrade & testing.
➢TOP, SVD, CDC, & ARICH test benches

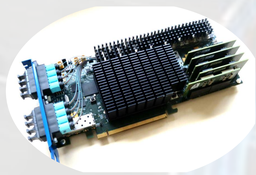


Introduction

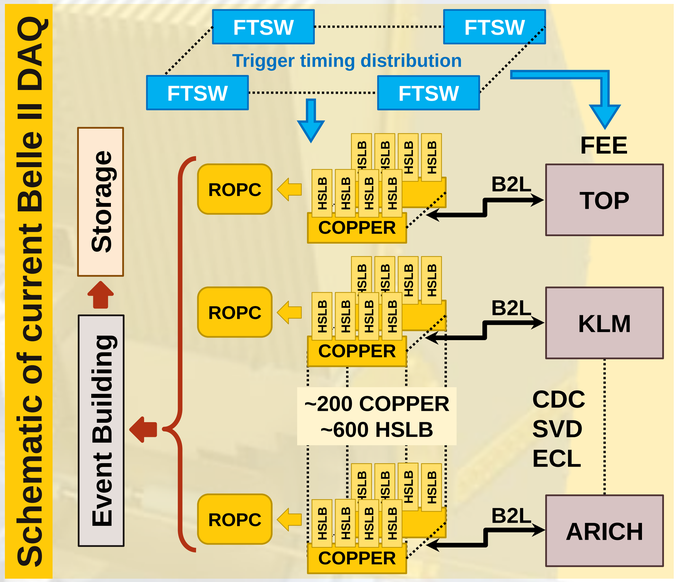
- Common unified readout system for all sub-detectors (except PXD)
  - **COPPER** – *Common Pipeline Platform for Electronics Readout*
  - **HSLB** – *High-speed Link Board*
- Unified timing and trigger distribution system (with FTSWs) for all FEE, readouts, & event building.
- Data after event building is stored on dedicated data storage servers

New readout board (PCIe40)

- Houses an **Intel Arria10 FPGA** and **supports 96 optical links** → *Simplifies the whole DAQ*
- **Fully instrumented**: all voltages, currents & temperatures measured
- **100 Gbps over the PCI Express bus**
- Board developed by CPPM, Marseille, firmware & software being developed by IJC Lab, Orsay, France



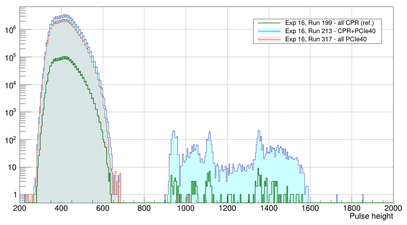
- Project plans to **replace all existing COPPER & HSLB boards** (~800).
- **~800 boards → only 19 PCIe40 boards.**



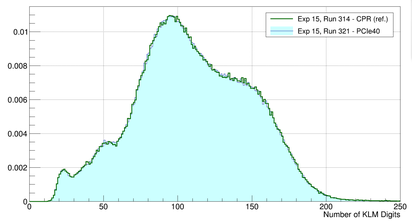
SLC & DAQ test results

- **Slow control (SLC) comparison tests**
  - Similar performance w/o DAQ, with DAQ, **PCIe40 outperforms COPPER at higher trigger rates**.
- **Full configuration** of 64 **TOP** FE and 32 **KLM** FE at KEK have been tested **with PCIe40**.
- **Data quality comparison tests** with all TOP & KLM FEE.

TOP data quality result



KLM data quality result



Current status & plan

- **PCIe40 FW & SW development is now complete.**
- Formatted DAQ software & unpackers for various sub-detectors are under test & development.
- Full SLC support is added & thoroughly tested allowing,
  - Basic FE register read/write/stream operations
  - Full configuration of the FEE for data readout
  - Monitoring FE voltages, currents, temp., etc.
- Plan on switching TOP & KLM sub-detectors to PCIe40 during summer shutdown of 2021.
- We have been preparing for the switch-over.
  - Dedicated ROPCs have been prepared.
  - Dedicated FTSWs have also been prepared.

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