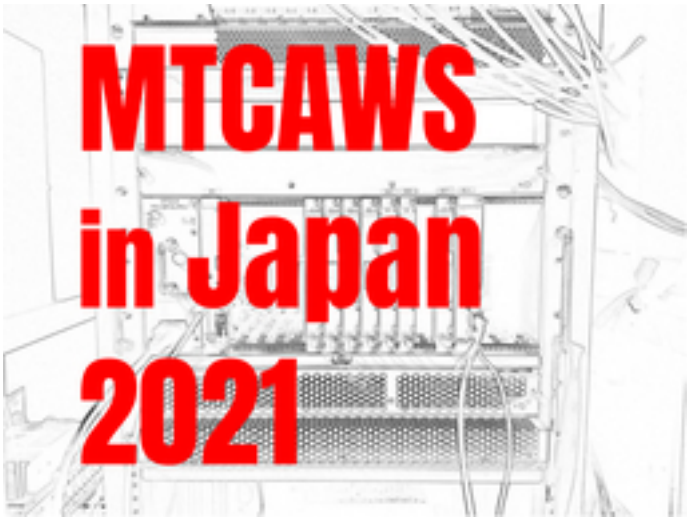
MTCA workshop for accelerator and physics in Japan

Tuesday 26 October 2021 - Thursday 28 October 2021

Virtual (Zoom)



Book of Abstracts

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Welcome address

Author: Takashi Kobayashi[1]

[1] *Director of the J-PARC Center*

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μTCA(MTCA.0) FPGA-Boards Development and Applications at KEK-Tsukuba

Author: Tetsuya Kobayashi[1]

[1] *KEK*

At KEK-Tsukuba Site, Micro-TCA(MTCA.0)-based FPGA boards were developed for LLRF control systems in 2009. EPICS-IOC is embedded into them. Our MTCA-based systems were applied to accelerators at KEK ahead of other facilities in the world, and they are successfully working in the beam operation. In this talk, some reminiscences of our struggles with the development of original FPGA boards will be presented, and MTCA application state in our facilities will be also reported.

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Timing synchronization system for beam injection from SACLA to SPRING-8 storage ring

Author: Takashi Ohshima [1]

[1] *JASRI*

We developed a timing synchronization system for injection from the linac of the XFEL machine, SACLA, to the storage ring (SR) of SPring-8. This injection scheme is demanded by the low-emittance upgraded ring in the future. Since the RF frequencies of the linac and the SR do not have an integer multiples relation, we have to introduce a new scheme to synchronize the beam ejection timing of the linac to the desired RF bucket timing of the SR. The new system was implemented to the MTCA.4 standard modules. The control of the bucket address is done according to the pre-defined injection table. The system was installed to the linac and the measured timing jitter was better than 4 ps in rms, which was enough to obtain high injection efficiency. This injection scheme has been adopted for the user operation of SPring-8 since February 2020.

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MTCA.4 based LLRF control systems for J-PARC synchrotrons

Author: Yasuyuki Sugiyama [1]

[1] *KEK*

MTCA.4 based LLRF control systems have been developed for synchrotrons of the Japan Proton Accelerator Research Complex (J-PARC). The J-PARC synchrotrons consist of the Rapid Cycling Synchrotron (RCS) and the Main Ring synchrotron(MR). Since the magnetic alloy loaded untuned RF cavity systems are used in both synchrotrons, multi-harmonic amplitude and phase control is essential and required to compensate a heavy beam loading. A MTCA.4 shelf with the DESY-type RF backplane is employed in developed LLRF control system to fit several AMC boards for controlling RF cavities. The multi-harmonic vector RF voltage control function is implemented in AMC to control the cavity RF voltage. The cavity voltage signal for the vector sum calculation and the beam phase feedback signal are exchanged between AMC boards via the MTCA backplane. The LLRF control system for the RCS was successfully deployed in 2019 and contributed to the achievement of stable acceleration of the high-intensity beam up to the design intensity, 8.3e13 protons per pulse. The prototype system for the MR was tested and used in the beam operation since 2020 to suppress unwanted harmonics. We plan to deploy the developed system to the MR during the shut-down period in 2021.

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DMMC Stamp and WIENER power supply

Author: Tomokazu Murakoshi [1]

Co-author: Fuminori Suzuki [2]

[1] *Embeck*

[2] *Embeck*

DMMC Stamp: DESY microTCA Technology LAB Launch the DMMC-Stamp. Embeck is responsible for domestic sales. We will first introduce you to this wonderful, small component. WIENER Power supply Low Noise 1000W PS for MTCA.4: we will introduce the features and performance.

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Next-generation open architecture MTCA field and Vadatech MTCA.4 lineup introduction

Author: Moriaki Hakuta[1]

[1] *LHS*

Current status of application fields for open architecture standard products after VME / Compact-PCI and Introducing Vadatech's MTCA product lineup and FPGA-equipped high-speed AD / DA products.

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Realization of high precision analog pattern output module by MicroTCA.4

Author: Naoki Kawamura [1]

[1] *Hitachi Zosen Corporation*

In the past, bus systems such as VME have been used for accelerator control and other systems that require stability, high reliability, and environmental resistance. For several decades, we have been designing and manufacturing VME bus boards and supplying systems. However, it has been more than 30 years since the birth of the VME standard, and the communication speed of the bus is inferior to that of the VME standard, and there are concerns about product supply in terms of maintainability. This time, we adopted the micro TCA bus standard as a module used in the pattern waveform output unit for controlling the paint bump power supply for J-PARC, which was conventionally built on the VME bus, and produced 2-channel 16-bit DA conversion analog modules as a replacement for the conventional unit. The pattern output board of the micro TCA bus standard makes the pre-set 16-bit data output patterns while synchronizing with the 1MHz clock, and outputs two types of output patterns, current patterns and voltage patterns of the paint bump power supply. This presentation will give an overview of the analog output module applying the micro TCA bus and the performance of the replacement evaluation with a conventional VME system.

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Development of a LLRF control system at WERC

Author: Tetsuro Kurita [1]

[1] *WERC*

A new LLRF control system for the synchrotron at WERC is in under development. The current system consisted of DDS (Direct Digital Synthesizer), DSP (Digital Signal Processor) and analog RF circuits has been working for 20 years with making a continuous improvement in it. However the current system becomes deteriorated and can not be maintained. The new system utilizes modern FPGAs and MicroTCA.4. The new system consists of three AMCs. One is for feedback control of RF frequency and the others are for processing beam position signals. We describe details of the system and the progress of the off-beam commissioning in this report.

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Synchronization of several EtherCAT networks by new multi-network EtherCAT AMC client

Author: Herbert Erd[1]

[1] *N.A.T*

Certain scenarios in industry and scientific research require to synchronize different EtherCAT networks with a high accuracy. The more precise the time stamp requirements become, the more difficult this task gets using classical solutions. By means of a newly developed AMC module, the time signals can be synchronously fed into and read from up to 8+1 independent EtherCAT networks. This provides a new possibility to connect classical industrial solutions to high performance MicroTCA systems in a flexible and cost-efficient way. The talk will compare this new solution to classical ones and high-light the benefits for users such as the European XFEL, Hamburg, Germany, where it will be used to connect to the installed MicroTCA systems.

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More flexible and cost-efficient x86 and non-x86 based compute power for MicroTCA systems

Author: Herbert Erd[1]

[1] *N.A.T*

One of today's setback in MicroTCA is the limited availability of (latest) x86 CPU generations in AMC formfactor. To overcome this situation and to provide more flexibility to the market N.A.T has developed a new carrier for COMex modules in AMC format which allows customers to select processing power based on exact needs, i.e. payload or control, from a small 2-core Celeron up to powerful 6 core XEON, made of the latest x86 CPU generation. The new COMex AMC carrier can host COMex modules based on TYPE 6 and 7 and is not limited to CPUs from Intel®. The new CPU carrier in AMC format will provide more flexibility and scalability to MicroTCA systems. It is a logical step in system design, from N.A.T.'s existing NAT-MCH-RTM module to the upcoming requirements addressed by the next generation of MicroTCA, providing more power, more bandwidth and higher bandwidth per AMC.

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MTCA.4 Crates: Introduction to the hardware infrastructure

Author: Christian Ganninger[1]

Co-author: Jasmin Goelzenleuchter [2]

[1] *nVent*

[2] *nVent SCHROFF*

nVent SCHROFF has committed itself to support the Big Science community with a broad portfolio of MTCA.4 crates as well as a full range of adjacent accessories like AMC front panels, filler panels, air blockers and guide rails. This presentation shows the range of nVent SCHROFF crates from 1U, 3U, and development crates up to the various versions of 12 Slots crates with different options and backplane topologies. In addition, the accessories will be presented and some hints are given on how and when to use filler panels.

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Overview of MMC stamp software development kit

Author: Patrick Huesmann[1]

[1] *DESY*

The Module Management Controller (MMC) is a mandatory component of every AMC board. DESY is developing, maintaining and licensing a turn-key MMC solution that is used on several hundred boards in different facilities - on DESY's own products as well as on third-party AMC boards developed by industrial customers and project partners. With the growing number of different boards, a clear separation between common code shared across boards and board-specific code becomes crucial - to keep the codebase maintainable as well as to provide a high-level API for AMC board developers who should be able to focus on their application without having to care about the low-level workings of the MMC. The high-level API makes a software development kit (SDK) possible, which is offered to MMC Stamp System-on-Module customers who wish to customize the pre-programmed

firmware according to their needs. This presentation gives a brief overview of the SDK and the high-level API it provides to AMC board developers.

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Status and future plans of the MicroTCA.4 compliant LO and CLK generation module

Author: Uros Mavric [1]

[1] *DESY*

The DRTM-LOG1300 (uLOG) is a MicroTCA.4 compliant LO and CLK generation module. It has been operating on EuXFEL for several years now. Currently other experiments expressed their interest for the LO and CLK generation modules operating at different reference frequencies. However not all the required LO and CLK frequencies can be generated using the currently implemented architecture. In parallel we have started a collaboration with the company KVG Quartz Crystal Technology GmbH to produce and test the newly produced modules. In this talk we will present other possible LO and CLK generation techniques which can provide LO and CLK signals with reference frequencies 500 MHz, 3 GHz and others. It is possible to order all these modules from KVG Quartz Crystal Technology GmbH.

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MicroTCA.4 projects at Sirius light source

Author: Daniel Tavares[1]

[1] *Sirius/LNLS*

The MicroTCA.4 standard has been employed at Sirius light source for a few accelerator systems: electron and photon BPM electronics, fast orbit feedback and timing receiver for distributed power supplies. In total 22 MicroTCA.4 crates run routinely at Sirius for users operation. This talk will describe the existing systems and short term plans. Special focus will be given to the issues found and lessons learned.

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Survey on MTCA in Japanese accelerators

Author: Fumihiko Tamura[1]

[1] *J-PARC Center*

MTCA is expected to be the next-generation platform for accelerator controls and many applications of MTCA are found in the acclerators in the world, while it seems slow to spread to the Japanese accelerator facilities. To investigate the reason, a small survey was performed in 2020 among KEK and J-PARC members, who are working for LLRF, monitors, and control systems. The survey results and the issues that were identified, are reported.

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Timing and low level RF control system of new injector LINAC for NEW SUBARU

Author: Eito Iwai [1]

[1] *JASRI*

A new linear accelerator was constructed for the New SUBARU (NS), a 1.5 GeV synchrotron radiation facility. The accelerating frequencies used at the new linac are 238 MHz, 476 MHz, 2856 MHz (SB), and 5712 MHz (CB). The required accuracy for the amplitude and phase of the accelerating field are 8E-4 and 0.2 degree, respectively in the most severe case. Also, the master trigger of the linac must be synchronized with both the aimed bucket timing of the ring and the linac master clock. To fulfill these requirements, the timing system and Low-Level RF (LLRF) control system were developed using the modules of Micro Telecommunication Computing Architecture 4 (MTCA.4) standard. The master trigger and the clock of the linac are generated at the master unit located near the LLRF station of the ring, and are delivered to four LLRF subunits of the linac through the optical links. The amplitude and phase of the accelerating field are controlled based on In-phase and Quadrature (IQ) scheme. The achieved stabilities in rms are 7E-4 in amplitude and 0.2 degree in phase, which satisfy the requirements. The operation of the NS has been carried out stably since April 2021 without any significant faults.

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Uniform communication over the MTCA interconnect and network

Author: Kazuro Furukawa[1]

[1] *KEK*

A low-level RF controller has been developed for the accelerator controls for SuperKEKB, Superconducting RF Test facility (STF) and Compact-ERL (cERL) at KEK. The feedback mechanism will be performed on Virtex-5 FPGA with 16-bit ADCs and DACs. The card was designed in the form-factor of an advanced mezzanine card (AMC) for a MicroTCA shelf. An embedded EPICS IOC on the PowerPC core in FPGA will provide the global controls through channel access (CA) protocol on the backplane interconnect of the shelf. No other mechanisms are required for the external linkages. CA is exclusively employed in order not only to make the AMC cards to communicate with each other, but also to communicate with central controls and with an embedded IOC on a Linux-based PLC for slow controls.

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LLRF system based on MTCA.4 boards for the J-PARC Linac

Author: Kenta Futatsukawa [1]

[1] *KEK*

In the J-PARC linac, the low-level radio frequency (LLRF) system with the digital feedback (DFB) and the digital feedforward (DFF) based on the cPCI platform was adopted for the satisfaction of amplitude and phase stabilities. It was operated without serious problems. However, it has been used since the beginning of the J-PARC and are more than fifteen years into the development. The increase of the failure frequency for this system is expected. In addition, it is difficult to maintain it for some discontinued boards of DFB and DFF and the older OS and developing environment

of software. Therefore, we had developed the new digitizer based on MTCA.4 boards for the LLRF system of the next generation. We installed and operated the seventeen digitizers at DTL3 and SDTL stations from the summer shutdown of 2020. In addition, we will install the three digitizers and one the MTCA.4 system, which is used to control four stations at MEBT1, in this summer. The project and the status of the LLRF system based on MTCA.4 for the J-PARC linac are introduced.

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Status of MTCA.4 standard based LLRF control board for the linear accelerator of the STF-2 and the ILC

Author: Toshihiro Matsumoto[1]

[1] *KEK*

In the International Linear Collider (ILC), the RF power generated with a single RF source (10 MW multi-beam klystron) is supplied to 39 superconducting cavities, and the amplitude and phase of each cavity are operated by vector sum-feedback control to keep the accelerating electric field and phase constant in single RF unit. At the Superconducting Test Facility (STF) of the High Energy Accelerator Research Organization (KEK), the STF-2 accelerator has been constructed and operated for the research and development of the ILC. In order to build a minimum configuration of the low-level RF control system for the ILC, the MTCA.4 standard based digital control board using ZYNQ have been developed for the LLRF system of the STF2 accelerator. The present status of the digital control board developed at STF and the future plan for ILC are reported.

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Adoption of the micro-TCA to the next KEK-PF LLRF system

Author: Daichi Naito [1]

[1] *KEK*

We plan to replace the low-level RF (LLRF) system at the KEK-PF. The present LLRF system is composed of analog modules, while the new system will be composed of digital boards which are based on the μTCA.4 standards. On the other hand, we will also adopt the μTCA to the monitor system for the transient beam loading effect. In this presentation, we introduce the present RF system, the overview of the new LLRF system, and the monitor system.

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Utilization of a unique MicroTCA.4-based digitizer for monitoring comb-like beam at the J-PARC Linac

Author: Ersin Cicek[1]

[1] *KEK*

The J-PARC linac beam pulse, formed by a chopper system placed at the MEBT, consists of a series of intermediate pulses with a comb-like structure synchronized with the rf frequency of the rapid cycling synchrotron (RCS). With a general-purpose digitizer, performing signal processing depending on the presence or absence of such an intermediate pulse is challenging. Besides, monitoring the entire macro pulse cannot be achieved on the current digitizer during the beam operation. However,

sequentially measuring and monitoring the comb-like beam, stable operation with less beam loss can be achieved even at higher beam intensity in the J-PARC. To this end, a beam monitor digitizer, including a digital signal processing function, that complies with the MicroTCA.4 (Micro Telecommunications Computing Architecture.4) standard has been developed. We present the architecture and implementation of the beam monitor digitizer within this paper.

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Planned upgrade of the LLRF system at the STF vertical test stand at KEK

Author: Mathieu Omet [1]

[1] *KEK*

The RF system currently used at the vertical test stand at the Superconducting RF Test Facility (STF) at KEK was established more than two decades ago and is all analog. It was decided to upgrade the controller part with a state-of-the-art MicroTCA.4-based LLRF system, allowing self-excited loop (SEL) operation. The realization of this upgrade is planned to be performed in collaboration with DESY.

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4th Generation NAT-MCH

Author: Herbert Erd[1]

[1] *N.A.T*

After more than 15 years and the 3rd MCH generation being currently deployed, the next generation 4 MCH is will become available soon, providing new features and functions. N.A.T will explain how to transit from today's MCH will to the 4th generation MCH and what the differences and benefits are. Also, the new generation MCH is designed to meet the upcoming requirements addressed by the next generation of MicroTCA, providing more power, more bandwidth and higher bandwidth.

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Digitizers for Big Physics

Author: Kacper Matuszynski[1]

[1] *Teledyne SP Devices*

Teledyne SP Devices provides world-leading modular data acquisition systems. As a long-term partner of MicroTCA Technology Lab, it offers various solutions in μTCA.4 form. Apart from getting a brief overview of the existing portfolio of products, you will get a glimpse of future developments. New functions and implementations will be highlighted and discussed. For example, a new way to take benefit of open FPGA architecture by defining a custom algorithm for advanced trigger requirements. We empower engineers and scientists to capture complex data enabling discovery and differentiated products.

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Experience with MTCA.4 LLRF systems at DESY

Author: Christian Schmidt [1]

[1] *DESY*

The first MTCA.4 LLRF system at DESY has been tested at the Free Electron LASer in Hamburg FLASH back in 2010. Since then, more and more accelerator facilities within DESY have been equipped with this technology. Today, the European XFEL is operated with a LLRF system consisting of more than 50 MTCA.4 crates. Maintaining all facilities in a twenty-four-seven on-call service allowed us to gain a lot of experience with these system over the last years. Especially the operation in a radiation prone and non-accessible environment demands a continuous improvement of the reliability and development of automation routines. As a next step an upgrade of parts of the LLRF systems at FLASH is planned which are in operation since almost 10 years.

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Development of the MicroTCA specification: Preparing the next generation

Author: Kay Rehlich[1]

[1] *DESY*

To keep the MicroTCA standard viable over many years it must follow the development of technology. A PICMG working group was formed to incorporate faster Ethernet and PCIe communication into the standard. This talk will discuss the direction and challenges of the next generation MicroTCA standard.

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AMC □□□□

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□□MCH□□□□□□

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MTCA □□□□□□□□□□□□□

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MTCA.4 □□ RTM□eRTM□□□

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SPring-8 / SACLA □□□□□□□□□□□□□□□□□ MTCA.4 □□□

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Zoom □□□□□□□□

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Electromagnetic Compatibility (EMC) and Analog Design Aspects in MicroTCA Crates (□□□□□□□)