TEL™'s Patterning Approaches Toward High NA EUV Lithography

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In this talk, we review state-of-the-art technologies to solve patterning issues aiming for the high-NA EUV generation. Advanced patterning technology for high-NA EUV lithography is being developed for further miniaturization of device patterns. Along with the miniaturization of pattern sizes, demands for resist resolution, roughness, sensitivity, pattern defects, and critical dimension control are increasing. We will discuss EUV technology trends and TEL™'s new approaches for the EUV challenges.

Reference

Outlook for high-NA EUV patterning: a holistic patterning approach to address upcoming challenges

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Holistic litho-etch development to address patterning challenges towards high NA EUV

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Seiji Nagahara, Ph.D. is Senior Director / Senior Chief Engineer in Tokyo Electron Ltd (TEL). He now works for marketing and development of the next generation coater and developer equipment and technologies for future lithography in TEL.

Prior to joining TEL, he was a lithographer in Renesas Electronics, NEC Electronics, and NEC. He researched lithography related technologies in a variety of places including IMEC (Belgium), University of California, Berkeley (USA), Argonne National Laboratory (USA), EIDEC (Japan) and Toshiba (Japan) in addition to TEL.

He took Bachelor, Master, and Ph.D. degrees in Engineering at Osaka University, Japan. He is active as an author of technical papers, book chapters, and patents in patterning technologies. He also contributes to the academic and technical societies as a committee member such as steering committee chair of MNC2023.