# D_RD_27: Study of modern FPGA device and associated new technology, and search for possible application in High Energy experiments

Yun-Tsung Lai

on behalf of the D_RD_27 group

KEK IPNS

*ytlai@post.kek.jp*
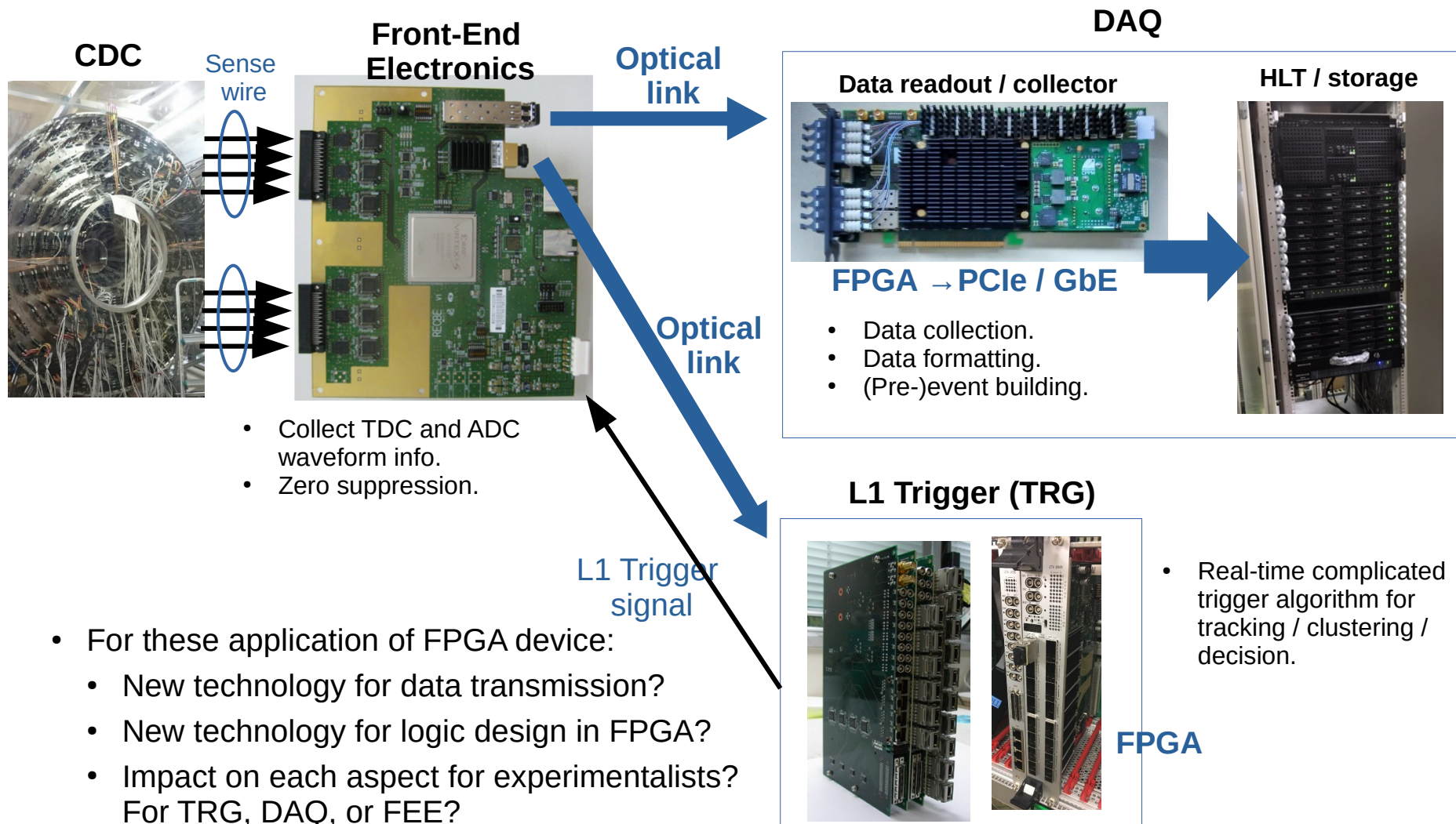
2023 Joint Workshop of TYL/FJPPL and FKPPL
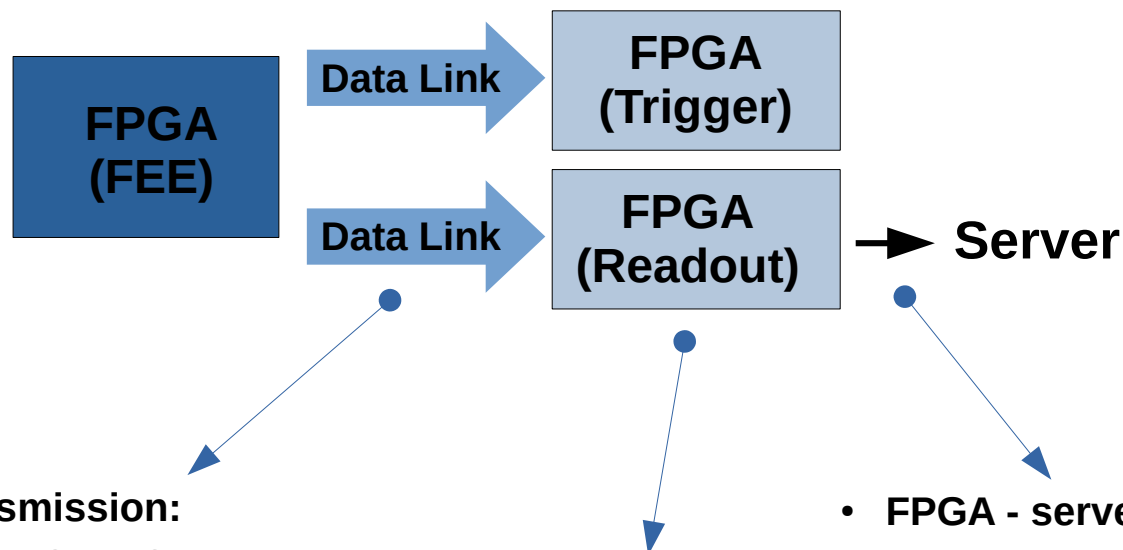
@ Ochanomizu University

11th May, 2023

# Application of FPGA in HEP experiments

- Here we use Belle II Central Drift Chamber (CDC) as an example.

**CDC**

Sense wire

**Front-End Electronics**



- Collect TDC and ADC waveform info.
- Zero suppression.

**Optical link**

**Optical link**

L1 Trigger signal

**DAQ**

**Data readout / collector**

**HLT / storage**

**FPGA → PCIe / GbE**

- Data collection.
- Data formatting.
- (Pre-)event building.

**L1 Trigger (TRG)**

- Real-time complicated trigger algorithm for tracking / clustering / decision.

**FPGA**

- For these application of FPGA device:
  - New technology for data transmission?
  - New technology for logic design in FPGA?
  - Impact on each aspect for experimentalists? For TRG, DAQ, or FEE?

```
FPGA          Data Link      FPGA
(FEE)         ────────▶      (Trigger)

              Data Link      FPGA
              ────────▶      (Readout)  ──▶  Server
```

**FPGA - FPGA transmission:**
- Optical link with FPGA MGT and optical modules.
- Non-Return-to-Zero (NRZ).
- Different encoding based on protocol design purposes. e.g. 8B/10B and 64B/66B.
    - <10 Gbps for DAQ.
    - <25 Gbps for TRG.

- Strong **FPGA devices** with:
    - Larger number of cells.
    - Larger data bandwidth.

  are critical for the usage in:
    - **TRG**: complicated algorithm implementation.
    - **DAQ**: collect and process large data.

**FPGA - server transmission:**
- Data transmission and system slow control.
- GbE, PCI-Express, VME, etc.
- PCI-Express is the most popular one nowadays: PCIe40(CRU) in ALICE, LHCb, and Belle II.
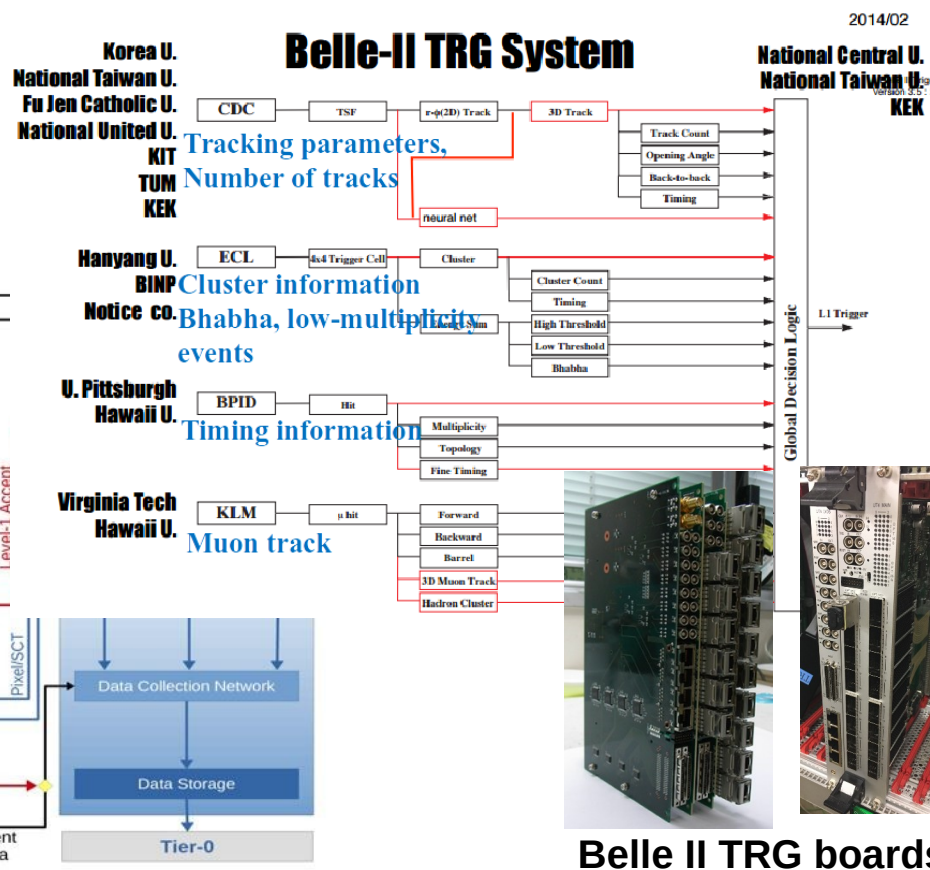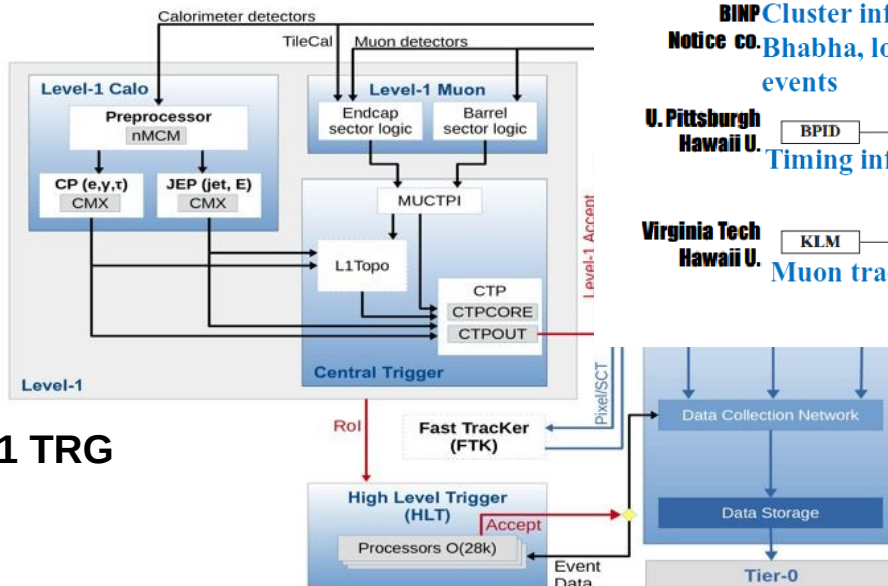
# L1 Trigger system (TRG)

- For TRG purpose, complicated algorithm is implemented to process detector raw data in real-time.

- Larger number of cells: improve the logic itself, resolution of triggering, and reduce the background rate.

- Utilization of machine-learning in the logic design.
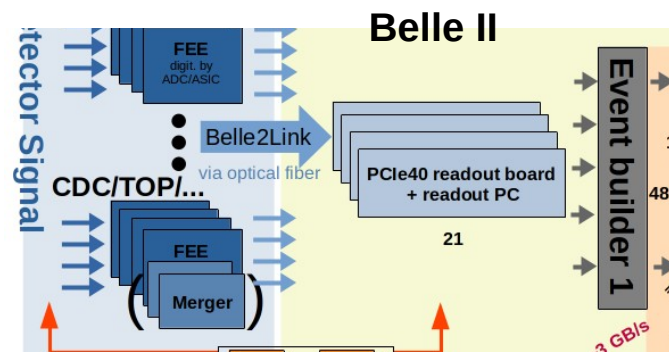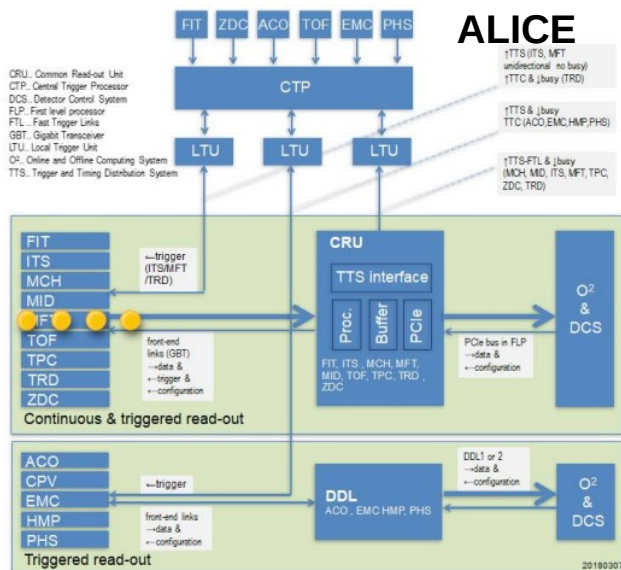
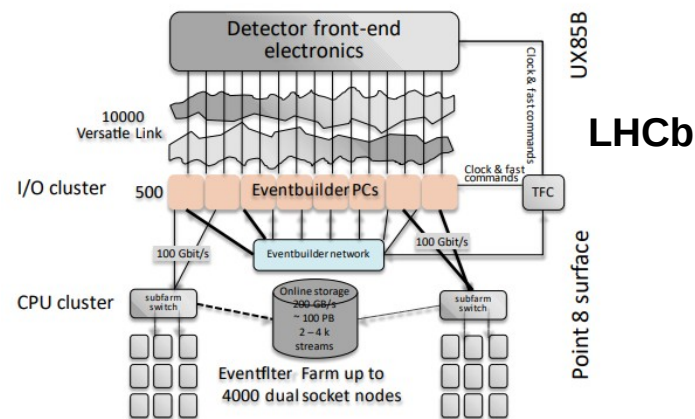**ATLAS Muon Trigger processor**



**ATLAS L1 TRG**

**Belle II TRG boards**
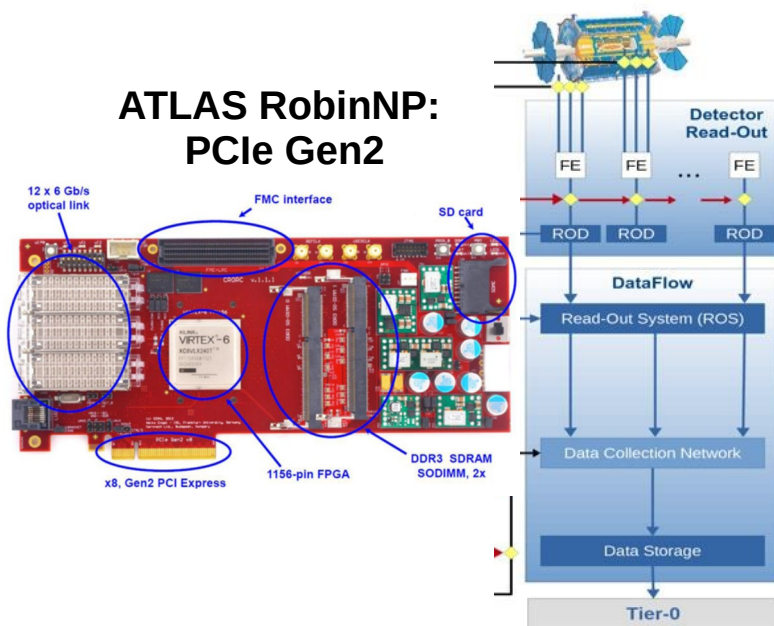
- Readout:
PCI-Express has been
the most popular solution
for FPGA→server interface.

**ALICE**
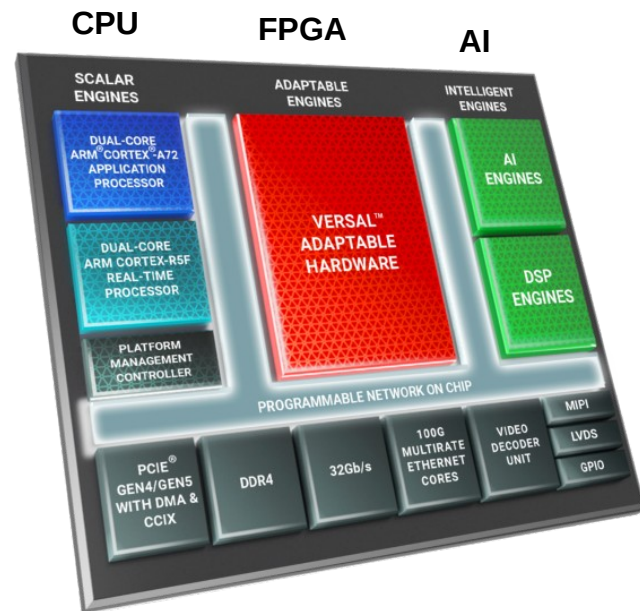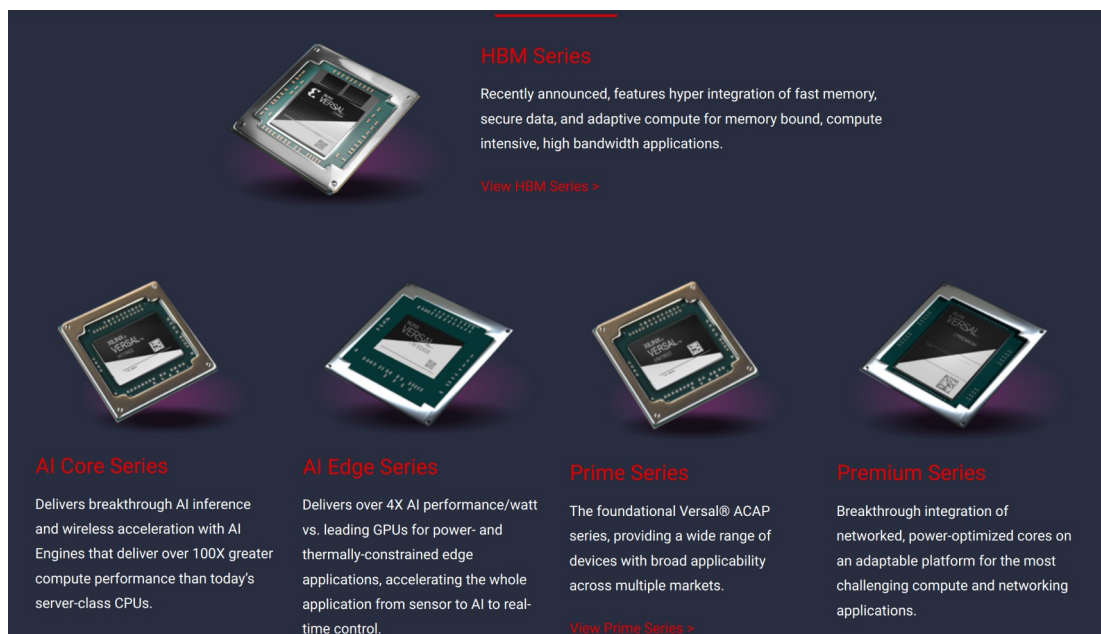
**Belle II**

**PCIe40: PCIe Gen3**

**ATLAS RobinNP:
PCIe Gen2**

**LHCb**

# Versal project

- KEK together with Japanese HEP community purchased a few evaluation kits of the Xilinx Versal series FPGA.

  - Plan: Common and general studies on the new technologies for future electronics device's R&D.

- The features of different Versal series:

  - AI/DSP engine: interface to implement ML core into firmware.

  - High Bandwidth Memory (HBM).

  - Larger number of cells + High transmission bandwidth.



**HBM Series**

Recently announced, features hyper integration of fast memory, secure data, and adaptive compute for memory bound, compute intensive, high bandwidth applications.

View HBM Series >

**AI Core Series**

Delivers breakthrough AI inference and wireless acceleration with AI Engines that deliver over 100X greater compute performance than today's server-class CPUs.

**AI Edge Series**

Delivers over 4X AI performance/watt vs. leading GPUs for power- and thermally-constrained edge applications, accelerating the whole application from sensor to AI to real-time control.

**Prime Series**

The foundational Versal® ACAP series, providing a wide range of devices with broad applicability across multiple markets.

View Prime Series >

**Premium Series**

Breakthrough integration of networked, power-optimized cores on an adaptable platform for the most challenging compute and networking applications.

**CPU** **FPGA** **AI**



source: Xilinx website

# Members for our proposed project

- IJCLab and KEK has been collaborating for PCIe40 upgrade in Belle II DAQ for a long time.
  - Technical support for new generation of PCI-Express.
- Experts of Belle II and ATLAS, TRG and DAQ in KEK participates in this project.
  - R&D for future electronics device based on Versal FPGA universal for different experiments.

| France | | | Japan | | |
|---|---|---|---|---|---|
| Name | Institute | | Name | Institute | |
| Daniel Charlet | IJCLab Orsay | PCIe readout device for Belle II / LHCb | Yun-Tsung Lai | KEK IPNS | E-sys, Belle II |
| Patrick Robbe | | | Manobu Tanaka | | E-sys |
| Tak-Shun Lau | | | Makoto Tomoto | | ATLAS |
| Emi Kou | | | Satoru Yamada | | Belle II |
| | | | Yutaka Ushiroda | | Belle II |
| | | | Kunihiro Nagano | | ATLAS |
| | | | Taichiro Koga | | Belle II |
| | | | Yu Nakazawa | | Belle II |

# Evaluable kits for Versal
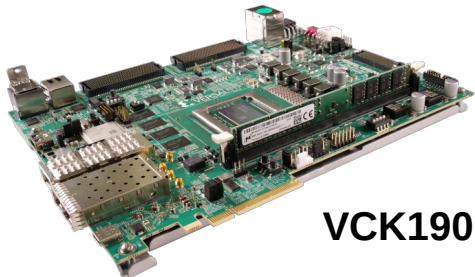


**VCK190**

- Features the VC1902 Versal AI Core series
- For using AI and DSP engines with greater compute performance that current server class CPUs.
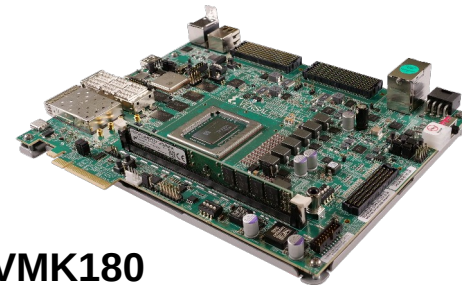


**VMK180**

- Features the VM1802 Versal™ Prime series
- The world's first adaptive compute acceleration platform (ACAP)
- A software programmable infrastructure and connectivity

Yu Nakazawa-san in our group has purchased it.



**VCK5000**

- Features the Versal AI Core Series
- For (AI) Engine development with Vitis and AI Inference development



**VPK120**

KEK has purchased it for collaboration study purpose.

- Features Versal™ Premium series VP1202
- Multiple high-speed connectivity option
- Massive serial bandwidth, security, and compute density.
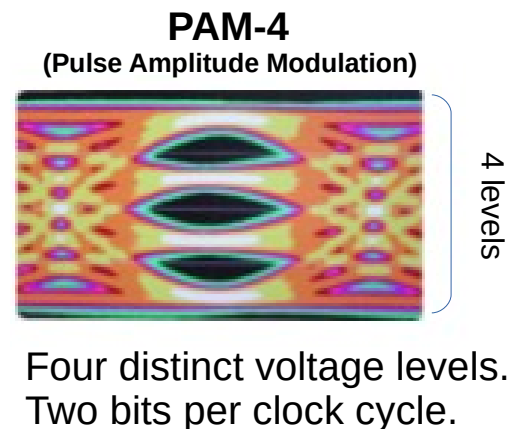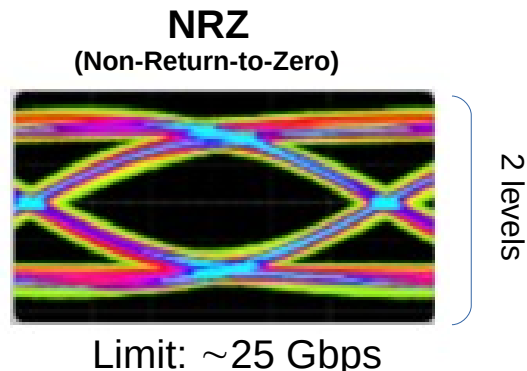
# New technology in Versal FPGA: PAM-4

- Present HEP devices mainly based on **Non-Return-to-Zero** (**NRZ**): Limit at 25~30 Gbps.
  - Belle II UT4 (UltraScale GTY) can operate with 25 Gbps stably using 64B/66B.
  - ATLAS muon trigger board reaches ~16 Gbps.

- **Pulse Amplitude Modulation (PAM-4):**
  - Four distinct voltage levels.
  - Xilinx UltraScale+: up to 58 Gbps. Versal premium (GTM): up to 112 Gbps.
  - PCIe Gen6: based on PAM-4.
  - Pioneer to study it in HEP community.

- **Work plan: With VPK120 GTM**
  - Higher error rate: firmware treatment in clock, check-sum, etc.
  - Gray code and different encoding scheme.
  - QSFP-DD lookback → 4*100 Gbps QSFP.
    - Optical oscilloscope could be helpful to further understand the property.
  - Develop general-purposed protocol for TRG.
  - DAQ: maybe still early, but studying the irradiation effect on it is also important.

**NRZ**
(Non-Return-to-Zero)



2 levels

Limit: ~25 Gbps

**PAM-4**
(Pulse Amplitude Modulation)



4 levels

Four distinct voltage levels.
Two bits per clock cycle.

source:
Xilinx

**VPK120**

# New technology in Versal FPGA: PCIe Gen5

- ALICE, LHCb and Belle II has been using the PCIe40(CRU): based on PCIe Gen3.

- New generation of PCI-Express comes out with a doubled bandwidth in few years.
  - Using proper device to study the properties of newer generation of PCI-Express is beneficial for the future readout device's development.

- **Work plan: With VPK120**, where PCIe Gen5 interface implemented with its GTY transceiver.
  - Host PC is also prepared,
    and the test bench is under preparation.
  - Start from simple register R/W function.
  - Make protocol (using DMA or so)
    for continuous readout, and
    study the performance of throughput.



**PCIe40: PCIe Gen3**

- An internship with Engineer background
  will stay in KEK for ~4 months to work for this.
  - Also for other preparations of technical works.
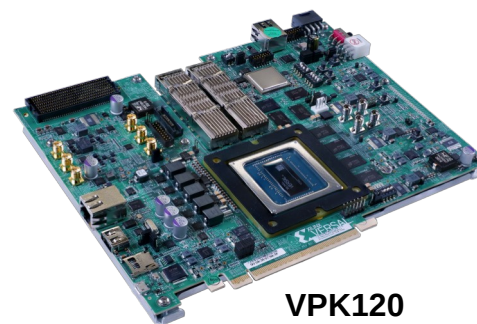


**VPK120**

# PCIe40 → PCIe400: ongoing work in IJCLab

- Reference: A ongoing project at France for future readout device: PCIe400

- Aim for 4 times larger bandwidth in 2026
  - More than 40 bi-directional links up to 26 Gbps (NRZ)
  - Use server memory or HBM2e
  - PCIe Gen5
  - Also reserved ports (QSFP112) for testing purpose on PAM-4.

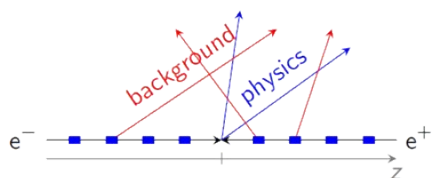- Plan for far future:
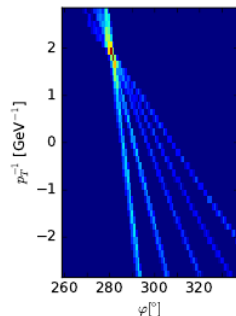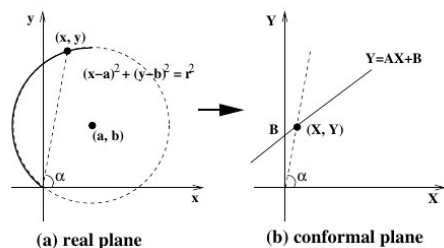  - A 800 GbE interface for 2032
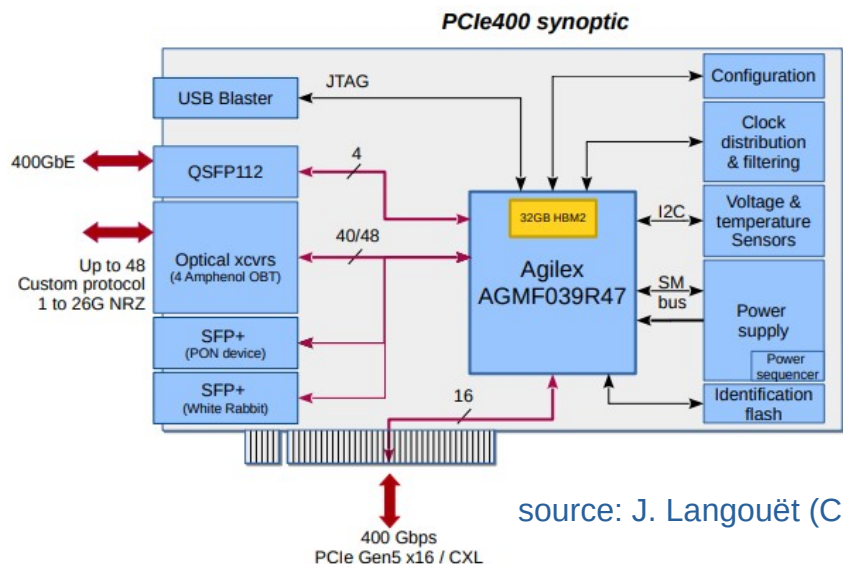


source: J. Langouët (CPPM)

- We expect the communication between KEK and IJCLab is helpful for the PCIe technical study.
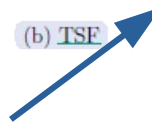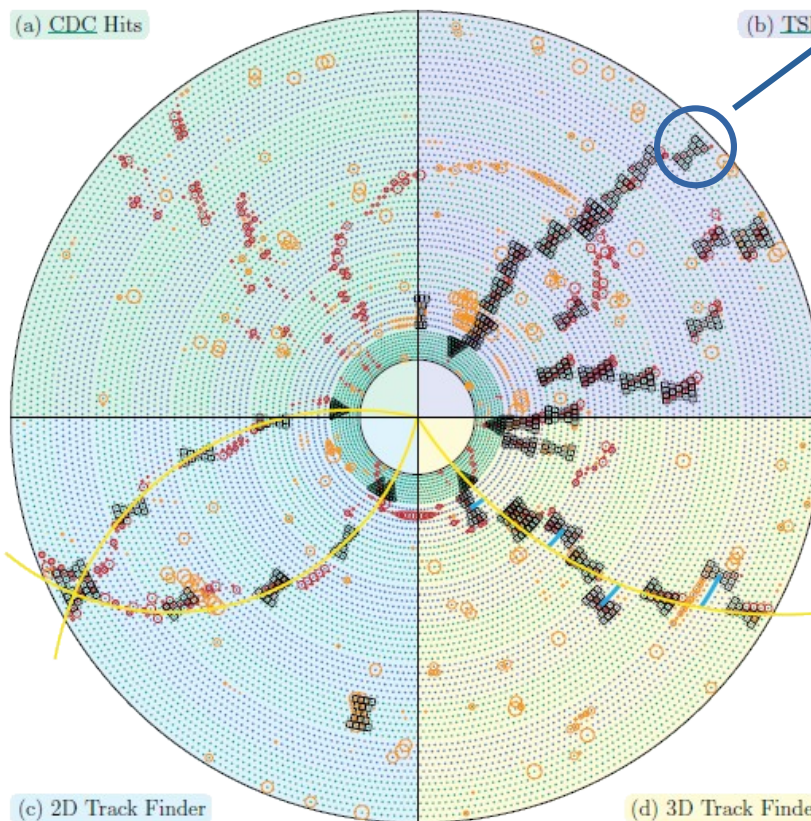
- L1 Trigger: Implementation of complicated physics algorithm in FPGA
  - How Belle II TRG does tracking in FPGA:

Inner TSF   Outer TSF

Track Segment:
Compromise on the granularity

(a) CDC Hits

(b) TSF

2D Track Finding:
Hough transformation.
Constraints on track condition.

$(x, y)$

$(x-a)^2 + (y-b)^2 = r^2$

$(a, b)$

$\alpha$

(a) real plane

$Y$

$Y = AX + B$

$B$   $(X, Y)$

$\alpha$

(b) conformal plane

Axial

Stereo

3D Track Finding:
Fitting with Stereo wire info

(c) 2D Track Finder

(d) 3D Track Finder

$\theta_{st}$ is greatly exaggerated
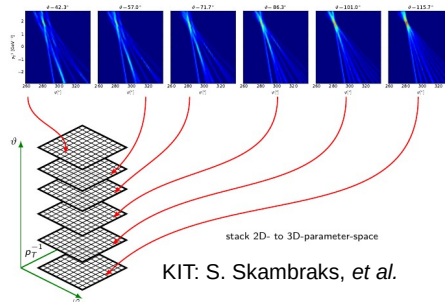
$e = \tan \lambda$
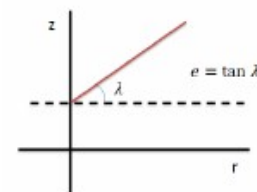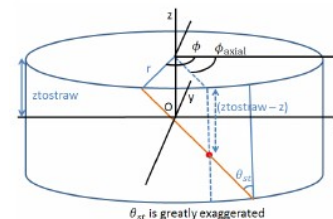
- Belle II Trigger board: Xilinx UltraScale XCVU080, XCVU160.
- ATLAS Muon Trigger processor: Xilinx UltraScale+ XCVU13P.

**Extension of more input info, Increasing granularity:**
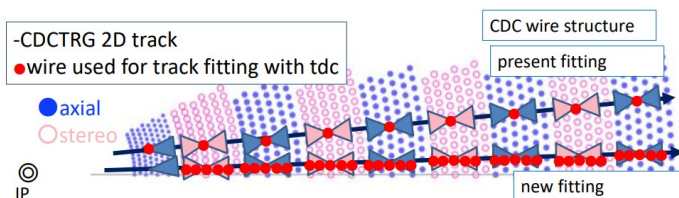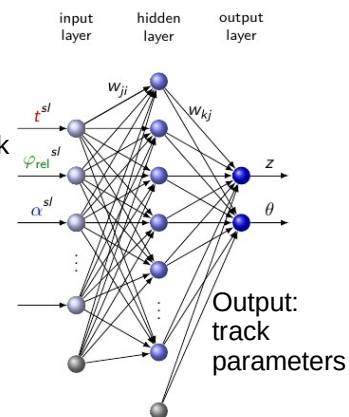


KEK: T. Koga, *et al*.

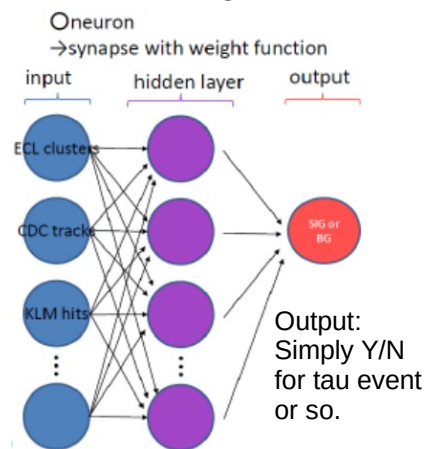**2D → 3D Hough tracking:**



KIT: S. Skambraks, *et al.*

**Neural Network 3D tracking:**

Already a sophisticated and working module. But less number of track can be processed.

KIT: S. Skambraks, *et al.*



Output: track parameters

**Neural Network for event categorization:**



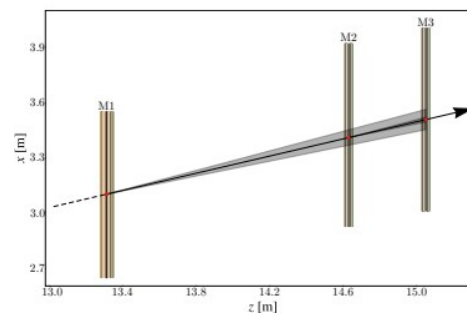Output: Simply Y/N for tau event or so.

KEK: T. Koga, R. Nomaru.

**ATLAS fast muon tracking with Neural Network:** arXiv:2202.04976



Also lots of other new ideas: GNN-based clustering, tracking ......

- To improve the performance of our HDL algorithms:

- **Go with the same way (finding/fitting)**:
  - Better precision or granularity
  - More info / less constraint e.g. ADC waveform.
  - Extra dimension. e.g. 2D→3D Hough.

- **Use machine-learning**:
  - NN for parameter calculation.
  - GNN on the global map.
  - NN for topological output.

*consider the selection for FPGA*

- Similar level of latency.
- **More FPGA resource and higher data transmission rate are desired**.

- **Premium series** with larger bandwidth (PAM-4).

- Utilize BRAM as neuron's LUT: hls4ml.
  - **FPGA resource**
  - Or **HBM** series

- Implement ML core into **AI engine** or **DSP engine** in new FPGA series.
  - **AI core, AI edge, Prime** series.

**VPK120**

**VCK190**          **VMK180**

# Trigger device for Belle II and ATLAS

- After comprehensive studies one the Versal FPGA series, we expect to develop a general and universal Trigger device for different experiments eventually.

**Belle II UT3**
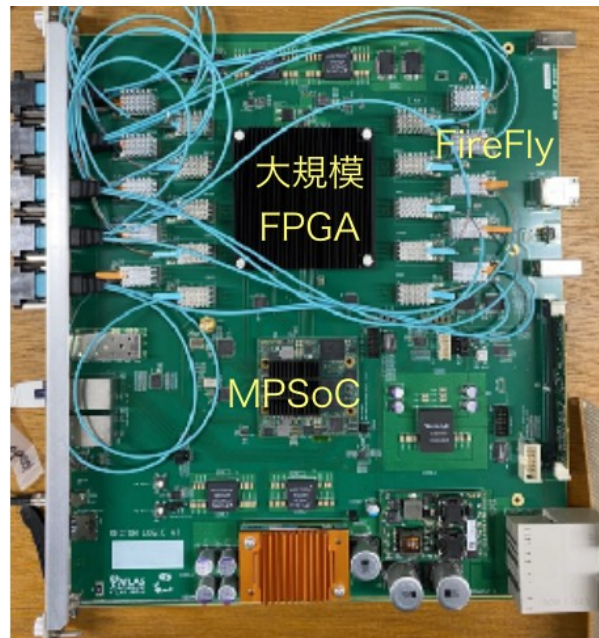
**Belle II UT4**

**ATLAS Muon Trigger processor**



Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

Xilinx UltraScale+
XCVU13P XCZU5EV
GTH,GTY: 16.8 Gbps
with 64B/66B

# Roadmap of the project

**1st year:**

- VCK5000, VPK120, and the host server have been set up in KEK.
- Study the properties of the fundamental functionalities:
  - GTM(PAM-4), PCIe Gen5, AI/DSP engine, CPU acceleration, etc.
- Prepare basic application for each of them for other members.

*Will purchase more kits (VMK180, VCK190) depending on other budgets*

**2nd year:**

- Make general transmission protocols for GTM(PAM-4), PCIe Gen5, and do performance study.
- Implement various L1 Trigger algorithm (Belle II and ATLAS) in the kits.
- Connect to existing Belle II or ATLAS system to take real-time data, and to check the trigger performance.

**3rd year:**

- Future universal device: readout or trigger.
  - Discussion.
  - Schematic/PCB design for the prototype boards.
  - Test with experiments people.

**IJCLab**: Hardware technical support, application at LHCb.

**E-sys**: project organization, technical and firmware development support, hardware R&D for future device.

**Belle II and ATLAS**: Algorithm development and other application for L1 trigger.

# Summary

- We started a project using the evaluation kits of the Xilinx Versal series FPGA with different experimental groups.

- For the application in experimental high energy physics, the new technologies associated to the FPGA device will be studied to develop general-purpose firmware/software modules.

- Based on research results, the development of universal device (such as Trigger or readout) for different experiments will be considered using these Versal FPGA or newer generation in the future.

- The collaboration between IJCLab group and KEK group will be helpful for the hardware technical R&D, and the experience exchange between E-sys, Belle II, ATLAS, and LHCb can have great impact for common development of future device or future experiment.

# Backup

# Resource of FPGA chips

| FPGA | # of cells (K) |
|---|---|
| XC6VHX380T (UT3) | 382 |
| XC6VHX565T (UT3) | 566 |
| XCVU080 (UT4) | 780 |
| XCVU160 (UT4) | 1621 |
| Versal AI Edge | 44-1139 |
| Versal AI Core | 540-1968 |
| Versal Prime | 329-2233 |
| Versal Premium | 833-7352 |
| Versal HBM | 3837-5631 |
| UltraScale+ HBM | 962-2852 |
| UltraScale+ 58G | 2252-3870 |
| UltraScale+ VU19P | 8938 |