The Future of Semiconductor Manufacturing
~ New Developments in Speed and Innovation ~

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We are now in the age of AI, and as we have seen with ChatGPT, the remarkable performance improvements of generative AI and its penetration into our daily lives will continue. The evolution and penetration of AI will continue at an accelerating pace and semiconductor technology supports this remarkable progress. Today's AI is realized by processing data using CPUs and GPUs, but their increased power consumption has become a major problem. This is a limitation of von Neumann's computing system, and in the future, dedicated, power-efficient AI processors specialized for each application will be needed. However, the rapid progress of AI requires speedy dedicated AI chips that can keep up with the rapid progress of AI.

The manufacturing process for advanced logic semiconductors is becoming more complex with each successive technology node. Today, it takes nearly six months to manufacture a wafer. In addition, the time required for the design and verification of dedicated chips is also increasing, and the reality is that it takes about three years from concept design to product shipment. This makes it difficult to supply dedicated chips in a timely manner in response to advances in AI. Therefore, there is a need for a new manufacturing technology that can provide high-yield products in a shorter period.

This is achieved by short TAT manufacturing using all single-wafer equipment. By processing the entire process in single-wafer tools, wafer fabrication can be performed quickly with minimization of variation during manufacturing. However, it isn't easy to improve yield in a short period using conventional methods. It is necessary to acquire more manufacturing information, analyze it, and feed it back to the design. In the past, the amount of data that could be obtained from manufacturing equipment and the sensitivity of analysis were insufficient, but with the remarkable improvement in computing power and advances in AI technology, it is now possible to extract appropriate information from large amounts of data. This has enabled MFD (Manufacturing for Design) to feedback information for optimal design from manufacturing technology, whereas in the past, the design was conducted in the form of DFM (design for manufacturing) with an awareness of the ease of manufacturing.

In addition, by providing a seamless manufacturing supporting service between the front-end process (wafer manufacturing) and the back-end process (packaging technology), it will be possible to provide high-performance products in a shorter period.

Evolved AI technology will not only facilitate data analysis but also circuit design technology. The time required for conventional design and verification can be shortened by using AI. By creating an environment that provides a seamless process from design to packaging using AI technology, it will be

possible to deliver high-performance semiconductor products to the market in half the time required by conventional methods. This method is called DMCO (Design and Manufacturing co-optimization) and is expected to become the mainstream of semiconductor manufacturing in the future.

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Dr. Kazunari Ishimaru joined Toshiba, Semiconductor Device Engineering Labs. in 1988 and engaged in the development of advanced SRAM/Logic technologies. From March 1997 to September 1998, he was a visiting industrial fellow at the University of California at Berkeley. From May 2006 to September 2010, he engaged in the development of 32nm~20nm CMOS platform technologies with IBM as Toshiba's representative (Vice President of R&D). After returning to Japan, he was in charge of logic product manufacturing at Oita operation as a senior manager. In 2013, he moved to the Center for Semiconductor Research and Development of Toshiba Semiconductor Company as a senior manager of the Advanced Memory Technology Development Dept. He became a Director of the Institute of Memory Technology R&D at Kioxia Corporation in 2022, and joined Rapidus Corporation in April 2023. He served IEDM committee member since 2001 and became a General Chair in 2011. He also served Scientific Advisory Board member of IMEC from 2014 to 2018. He was promoted to IEEE Fellow in 2014.