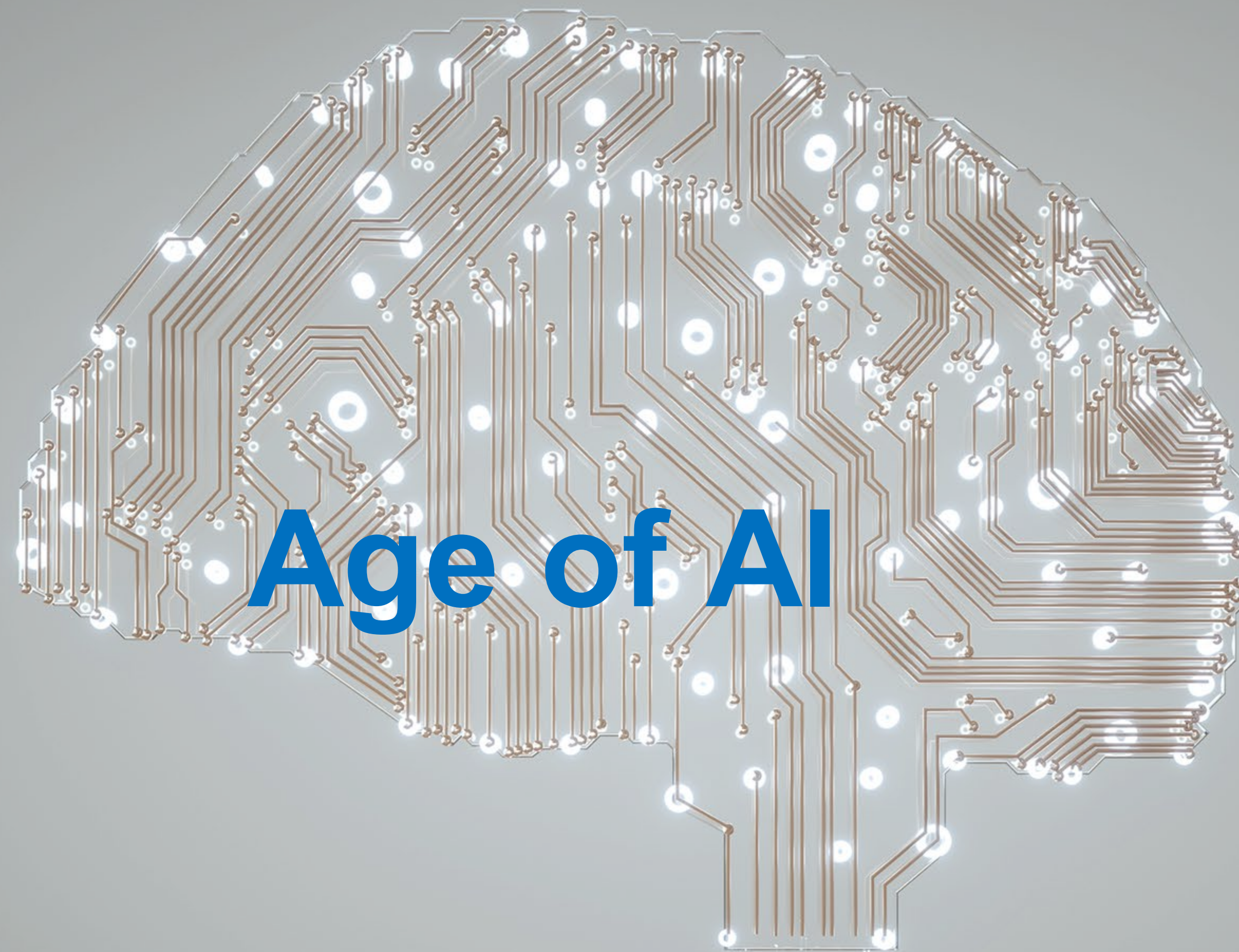




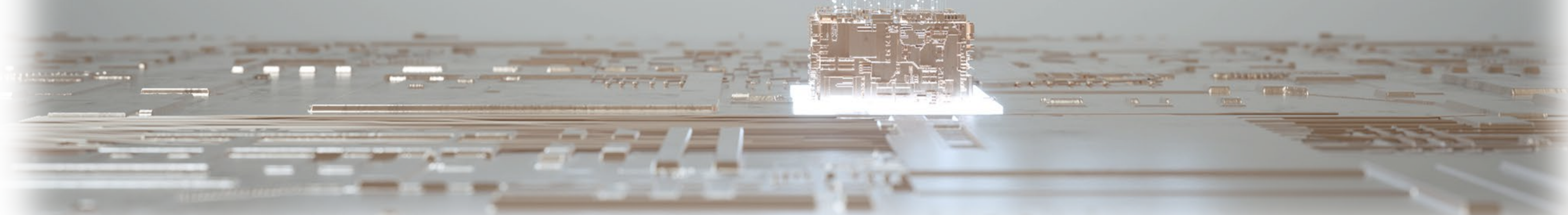
# "The Future of Semiconductor Manufacturing: New Developments in Speed and Innovation."

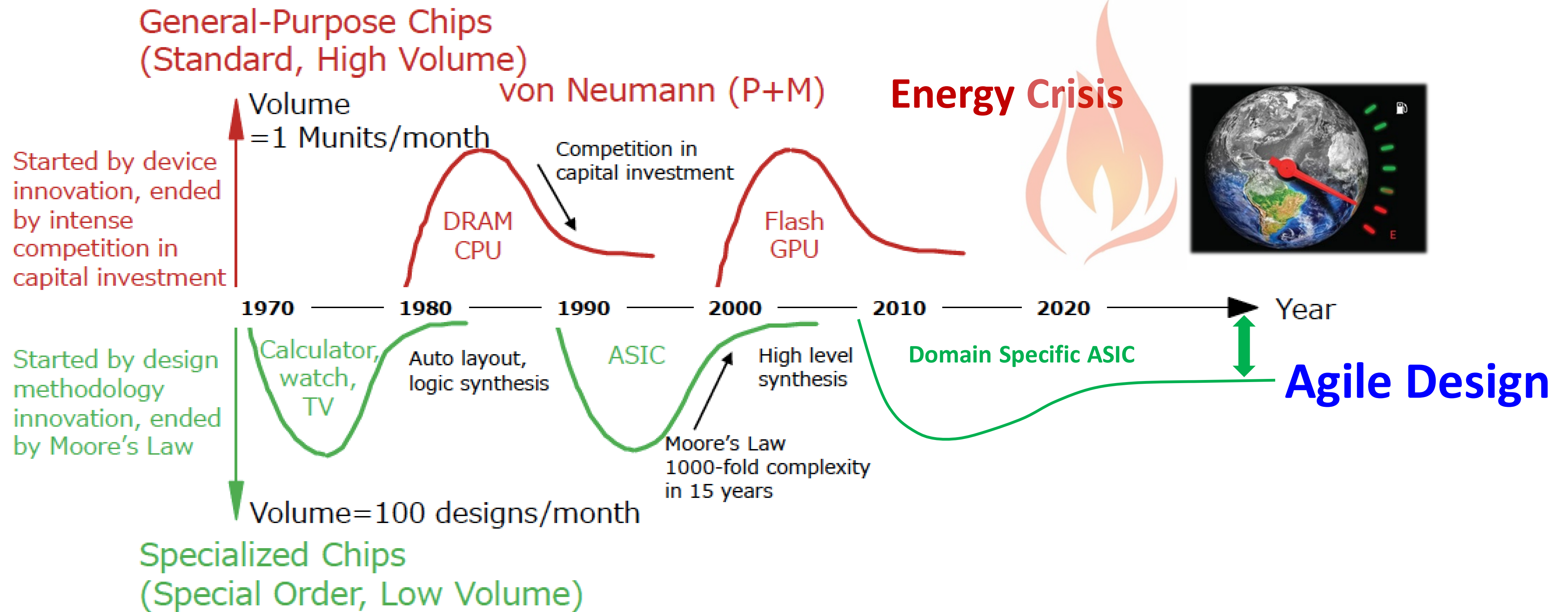
January 29th, 2024

**Kazunari Ishimaru, Ph.D./IEEE Fellow**  
Senior Managing Executive Officer,  
Silicon Technology Division  
Rapidus Corporation



# Age of AI



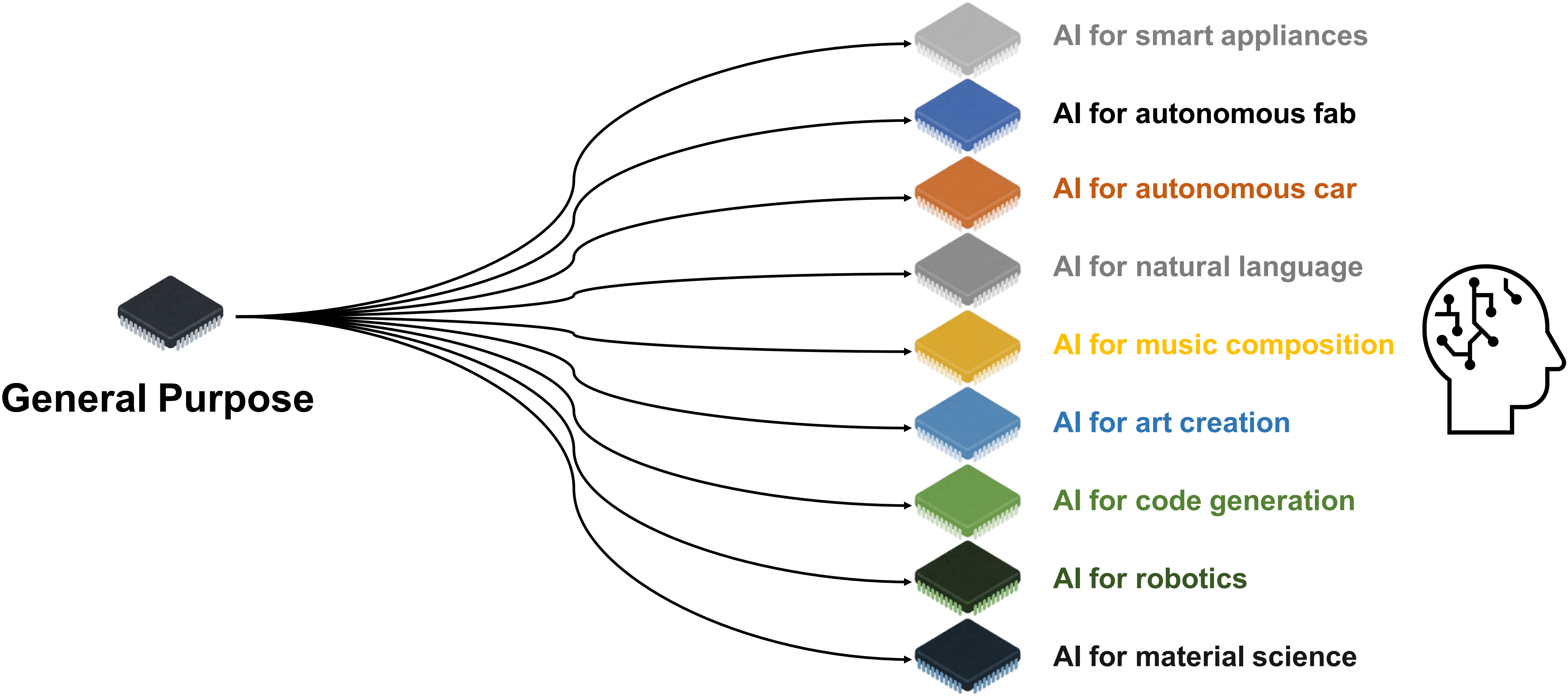


Source: T. Kuroda, ISSCC 2010 Panel Discussion, "Semiconductor Industry in 2025".

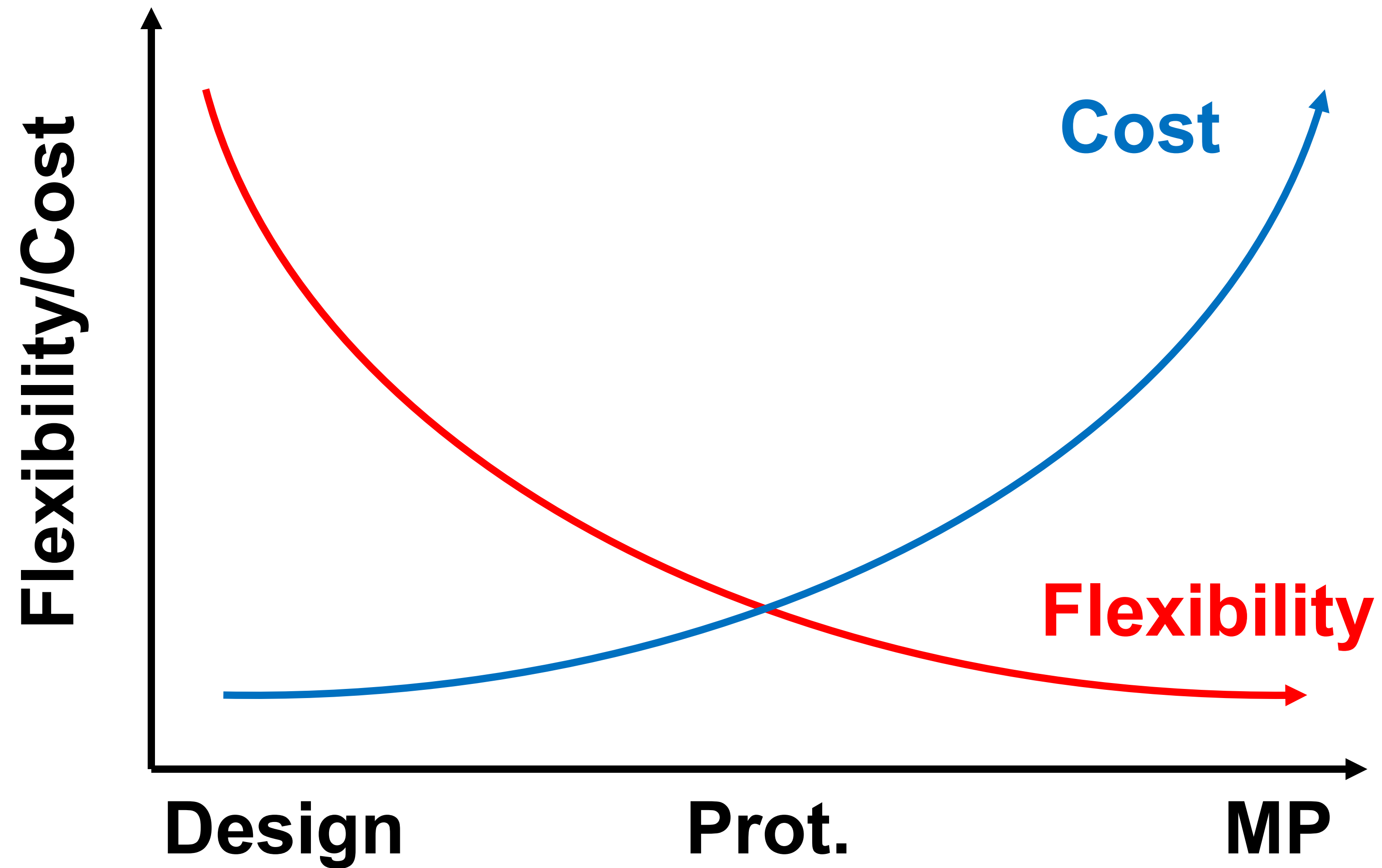
# Predicted in 2010 about Semiconductor Industry in 2025

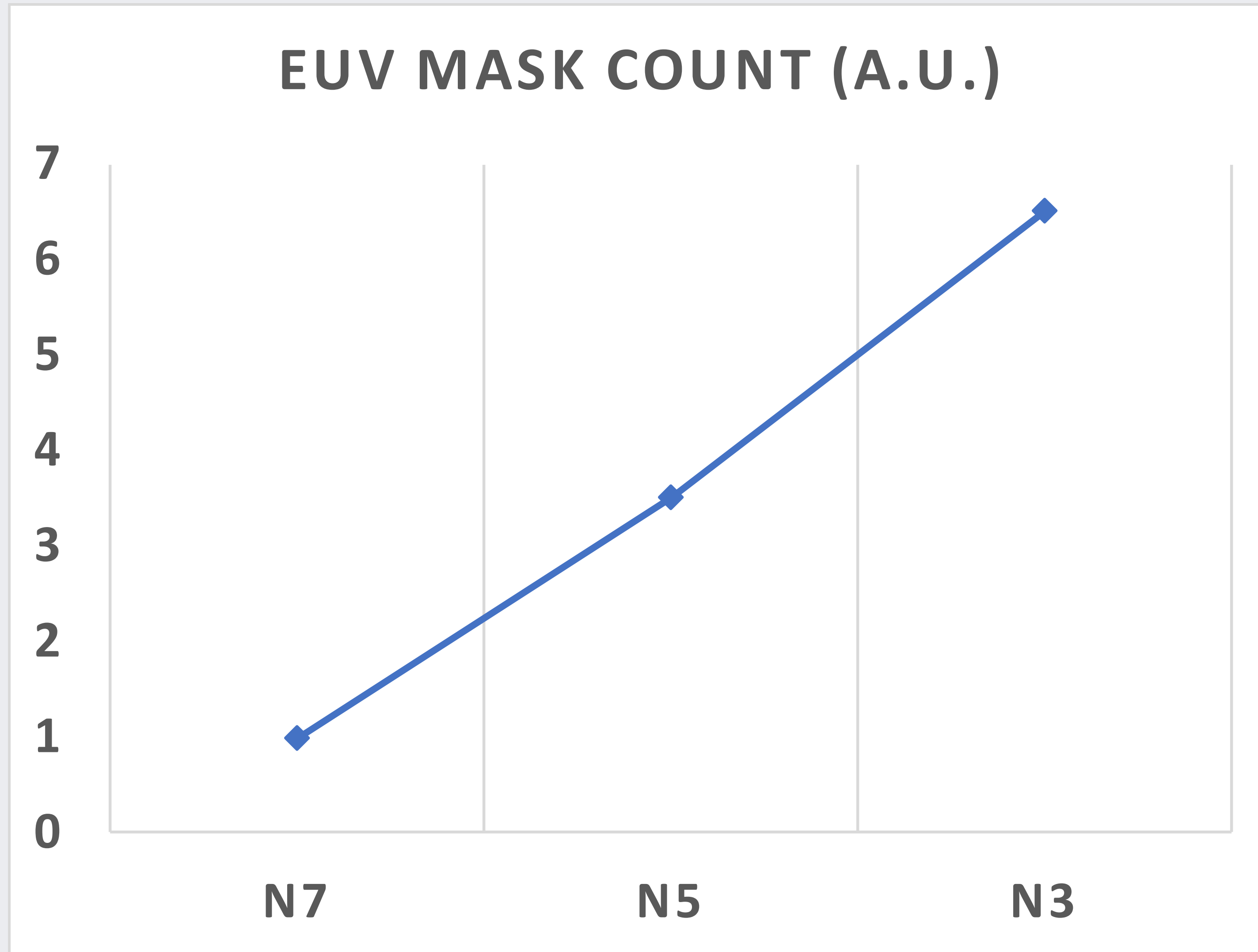
Source: <http://www.dlab.t.u-tokyo.ac.jp/en/message/chapter01.html>

# General Purpose to Specialization



# Conventional Design for Manufacturing (DFM)





# Focusing on Speed – A New Foundry Model



Design  
Solution



Front-end



Back-end

## World's Shortest Total Cycle-Time

高性能 半導体製品をめざして



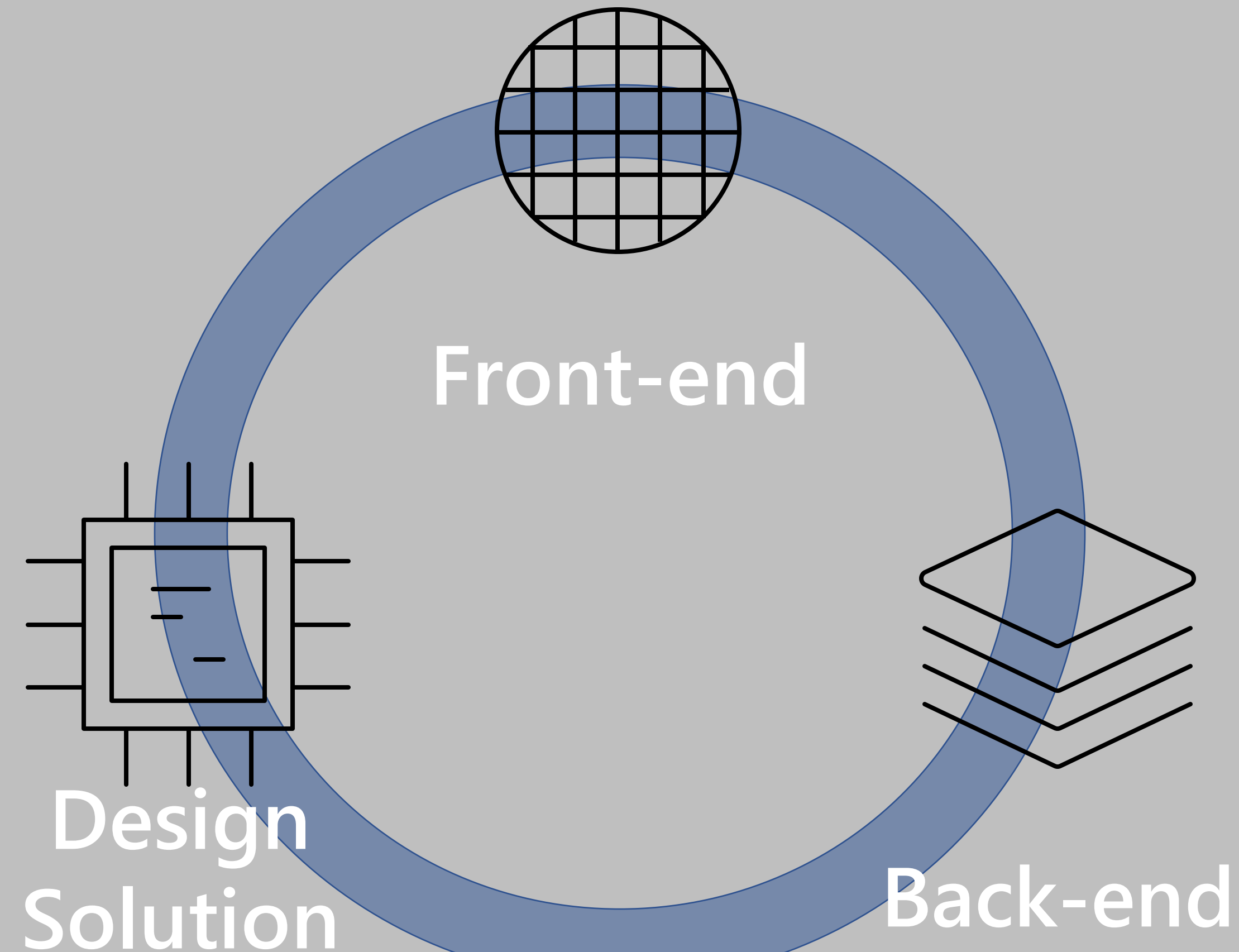
Design-Manufacturing Co-Optimization



# “RUMS” – A New Foundry Model for the Age of AI

“RUMS”

Rapid & Unified Manufacturing Service



# Co-optimize both Design & Manufacturing

DFM

Design for Manufacturing



Design  
Space

**DMCO**

Design-Manufacturing  
Co-Optimization



Manufacturing  
Space

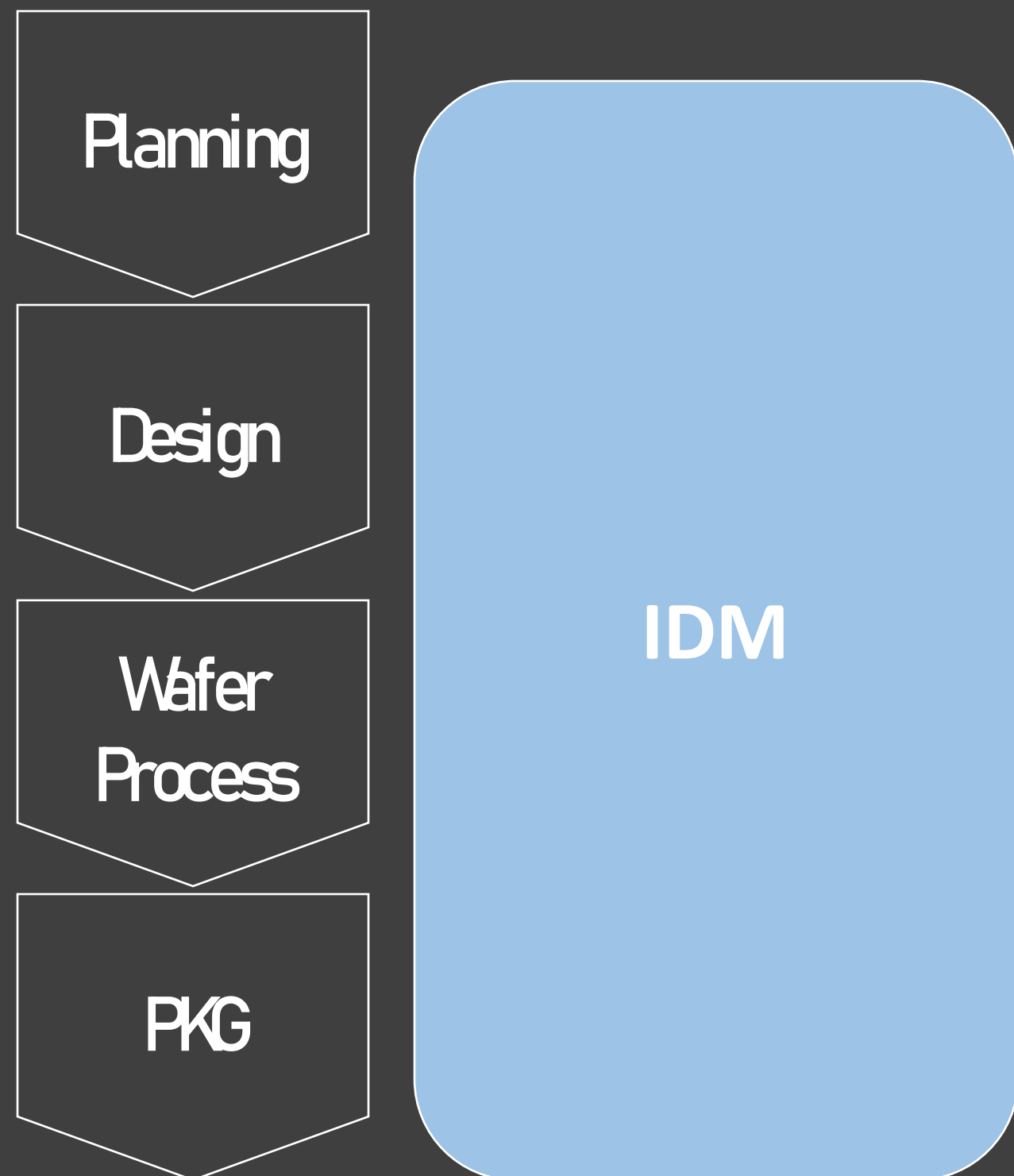
MFD

Manufacturing for Design

# “RUMS” – True Requirement for the Age of AI

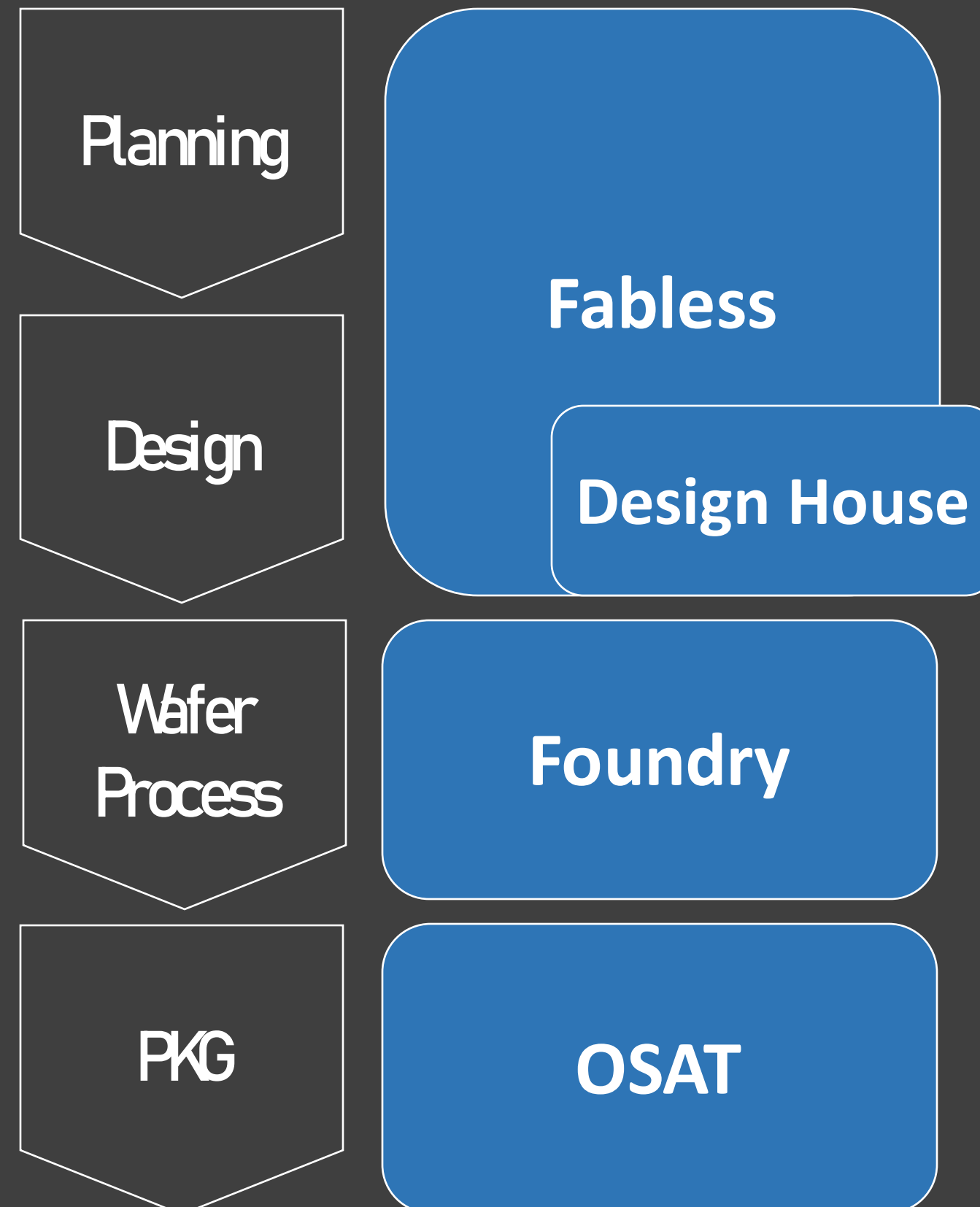
1

## Vertical Integration



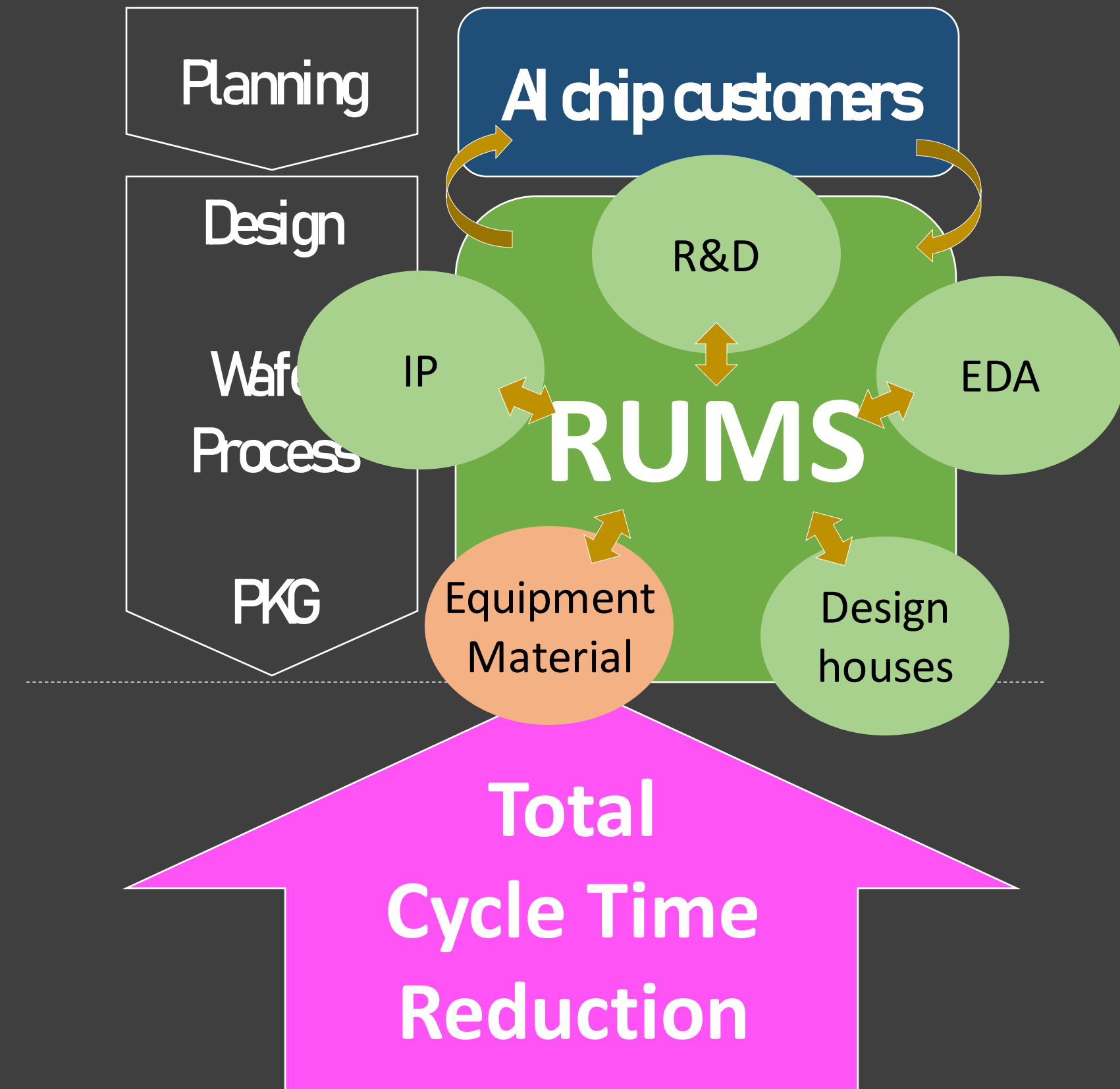
2

## Horizontal Specialization

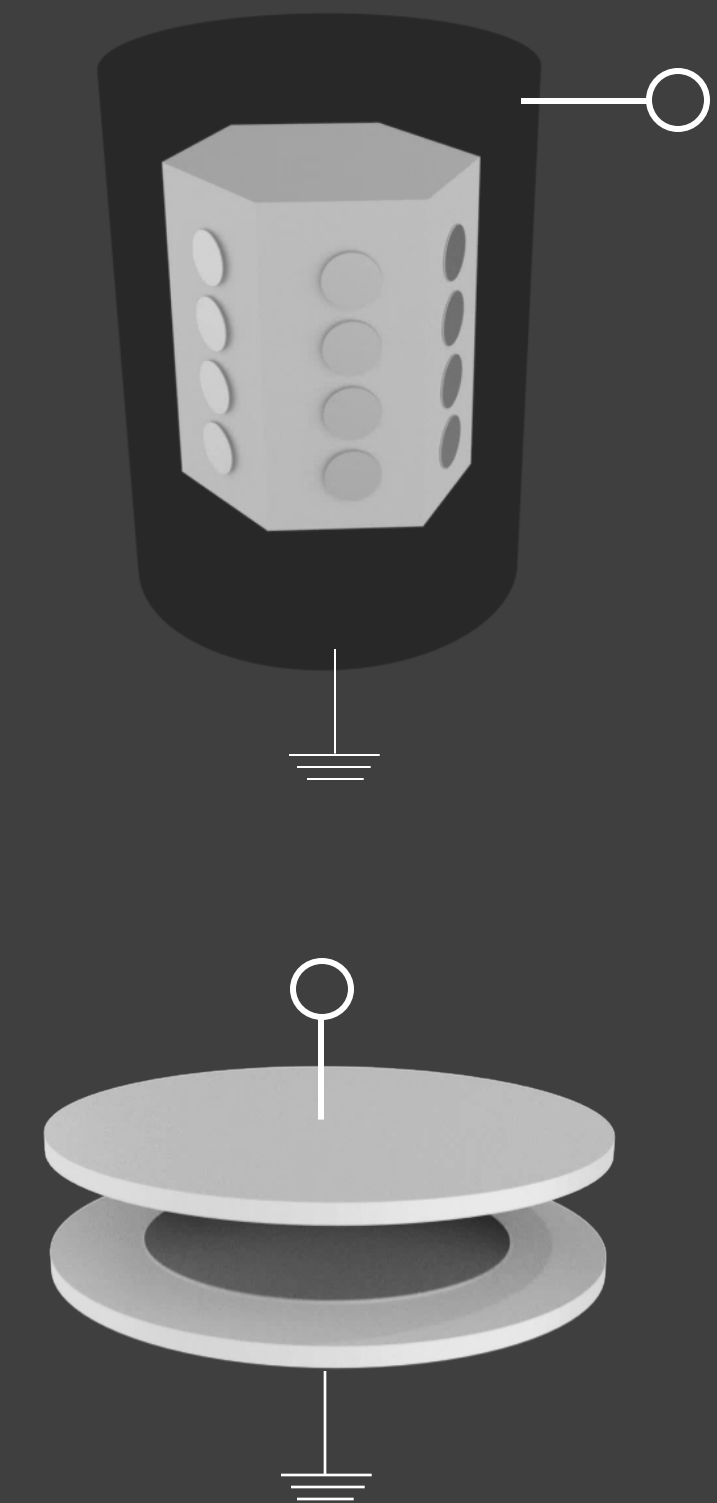
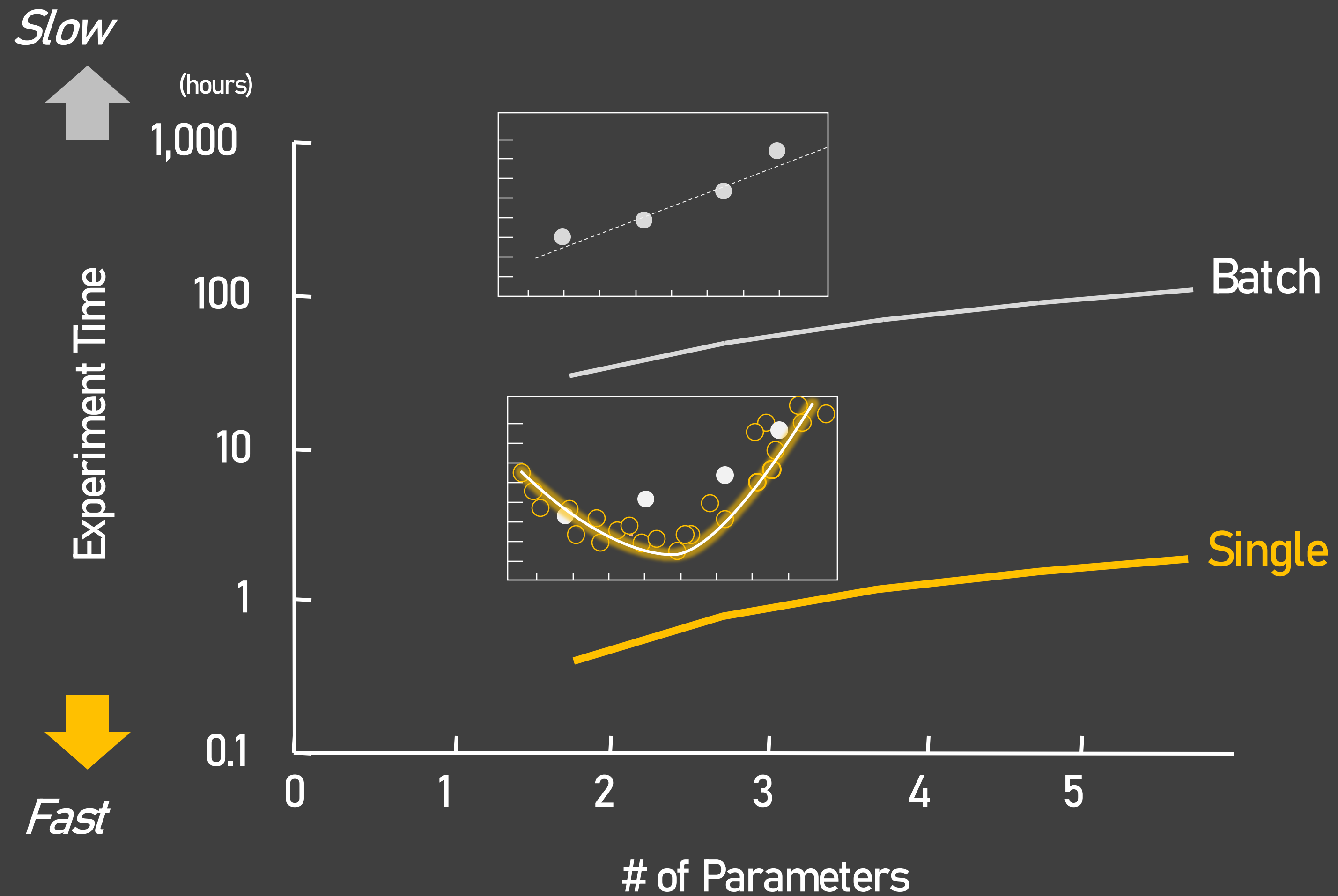


3

## Integrative Co-Creation

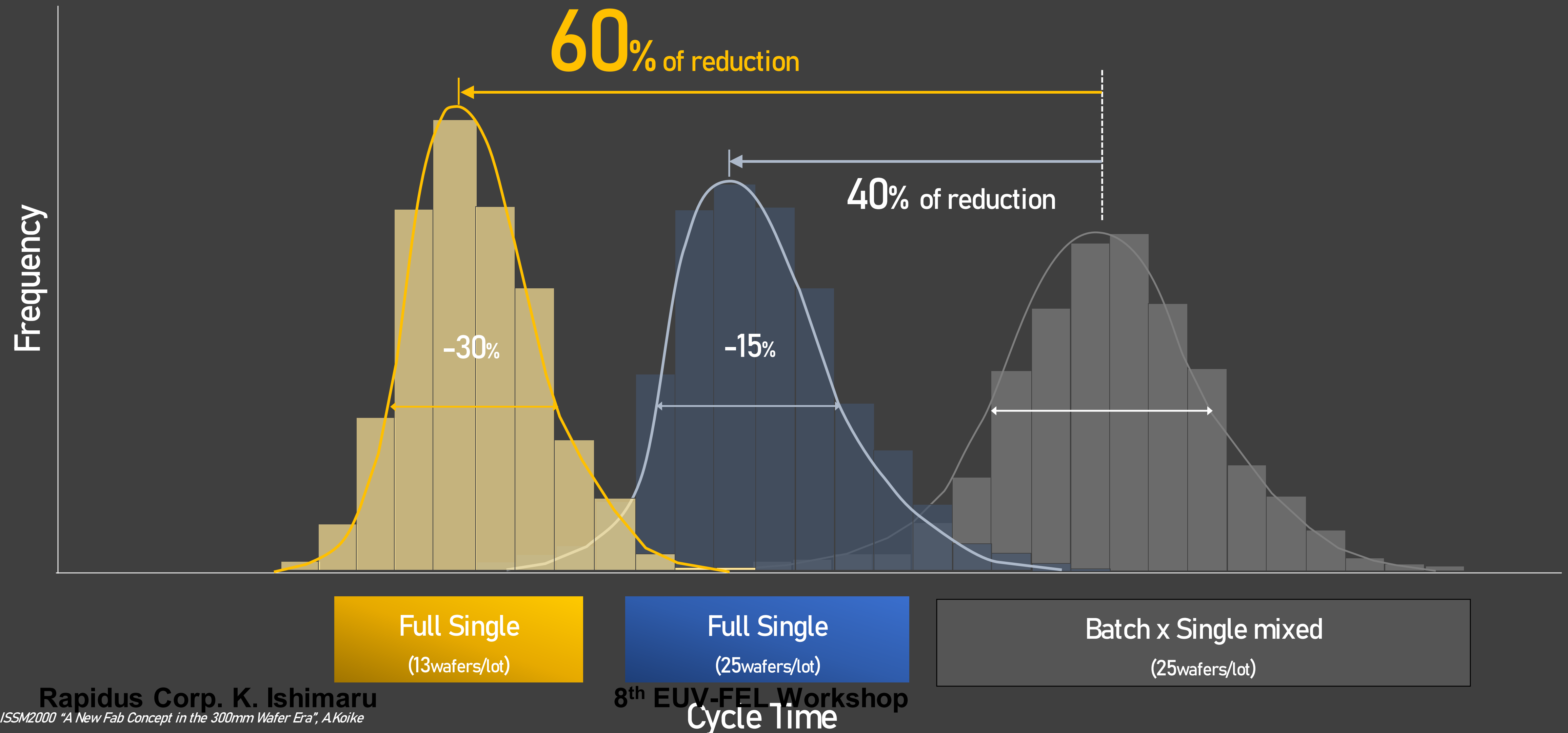


# Start Point of Innovative Idea

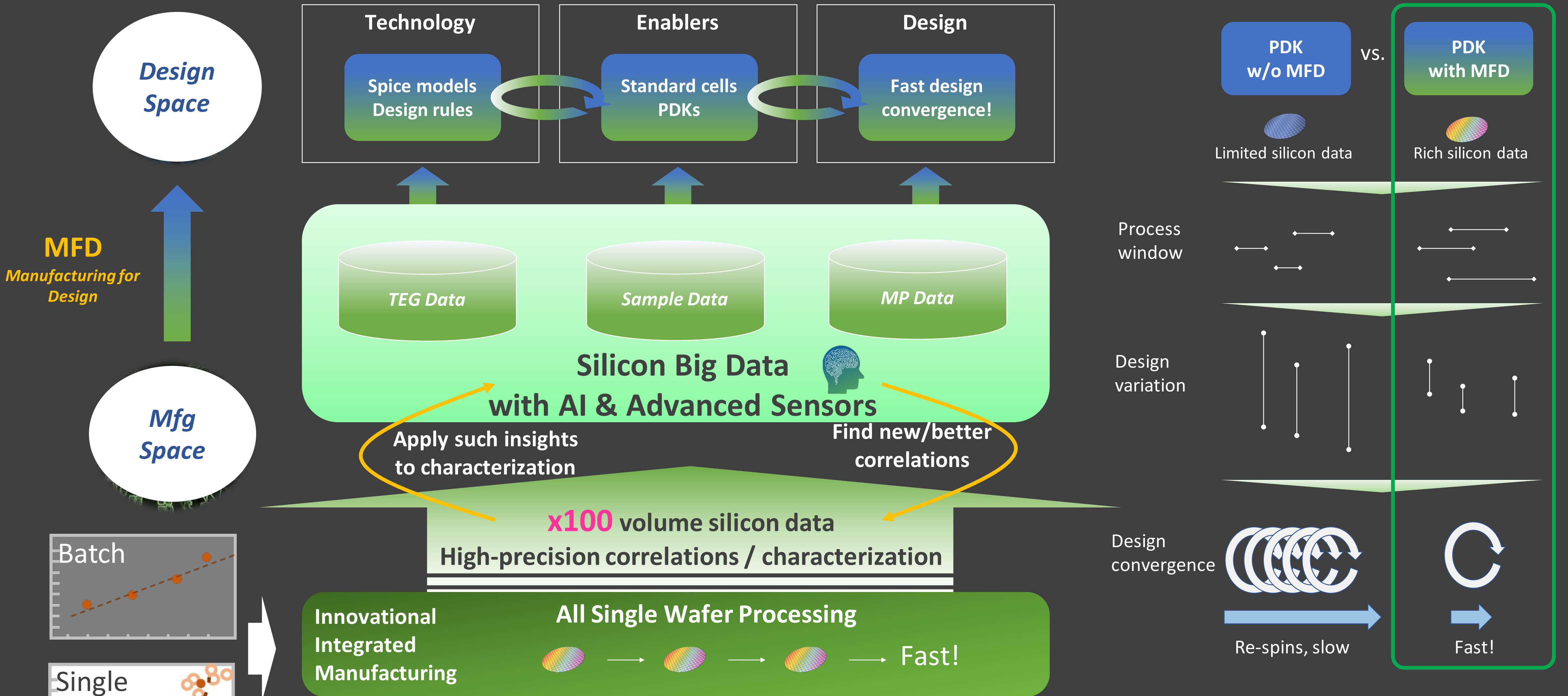


# Cycle Time Simulation

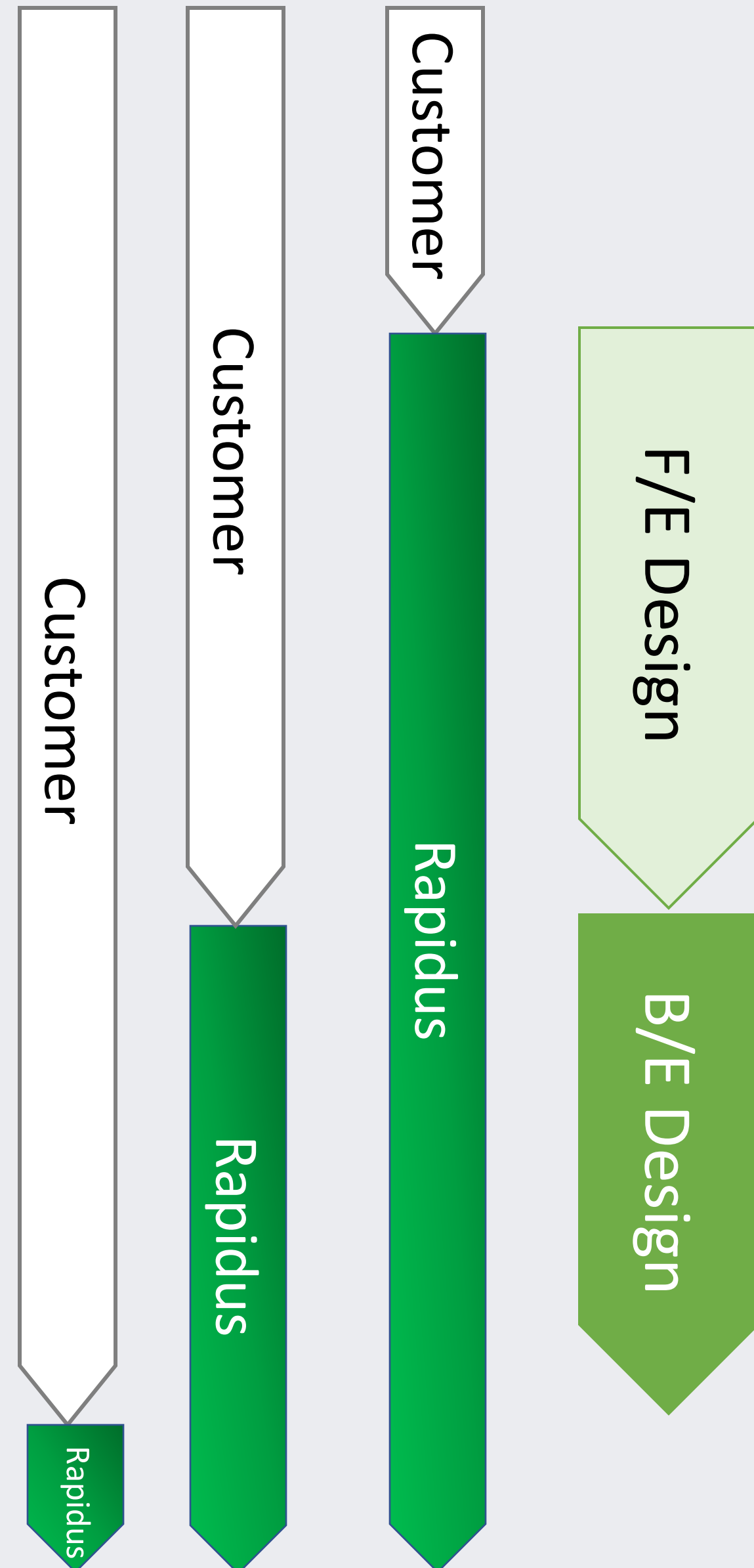
Rapidus is building a fab with all single wafer processing.



# Si-trained PDK and AI models



# Raads: Rapidus AI-Assisted Design Solutions



## 3 key components of Raads

### 1 Raads.Generator

- Generate machine readable codes from specifications in natural languages

### 2 Raads.Optimizer

- Find the optimal combination of parameters under given constraints.
  - ✓ Ex. Achieve least leakage while maintaining clock freq. XX GHz.

### 3 Raads.Navigator/.Manager

- Learn design cases with fast PPA convergence from the historical design, then accompany designers to navigate.
- Learn and optimize hierarchical layout blocks to achieve short-TAT.



1. Design Cycle Time < x ½ of conventional

2. Replicate experts w/ Raads.Navigator for parallelism



*Rapidus*