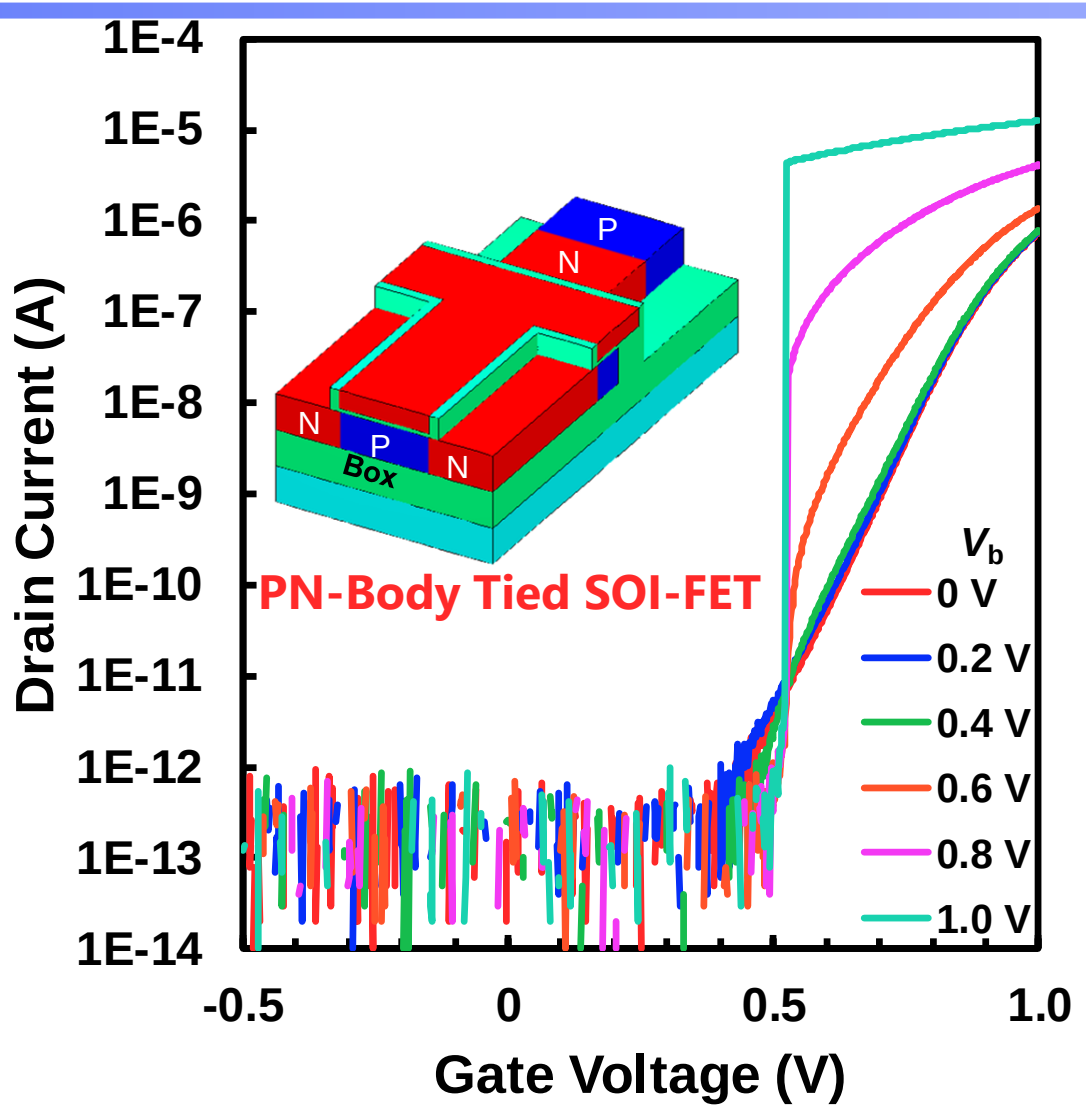
SOIPIX 量子イメージング研究会 2024

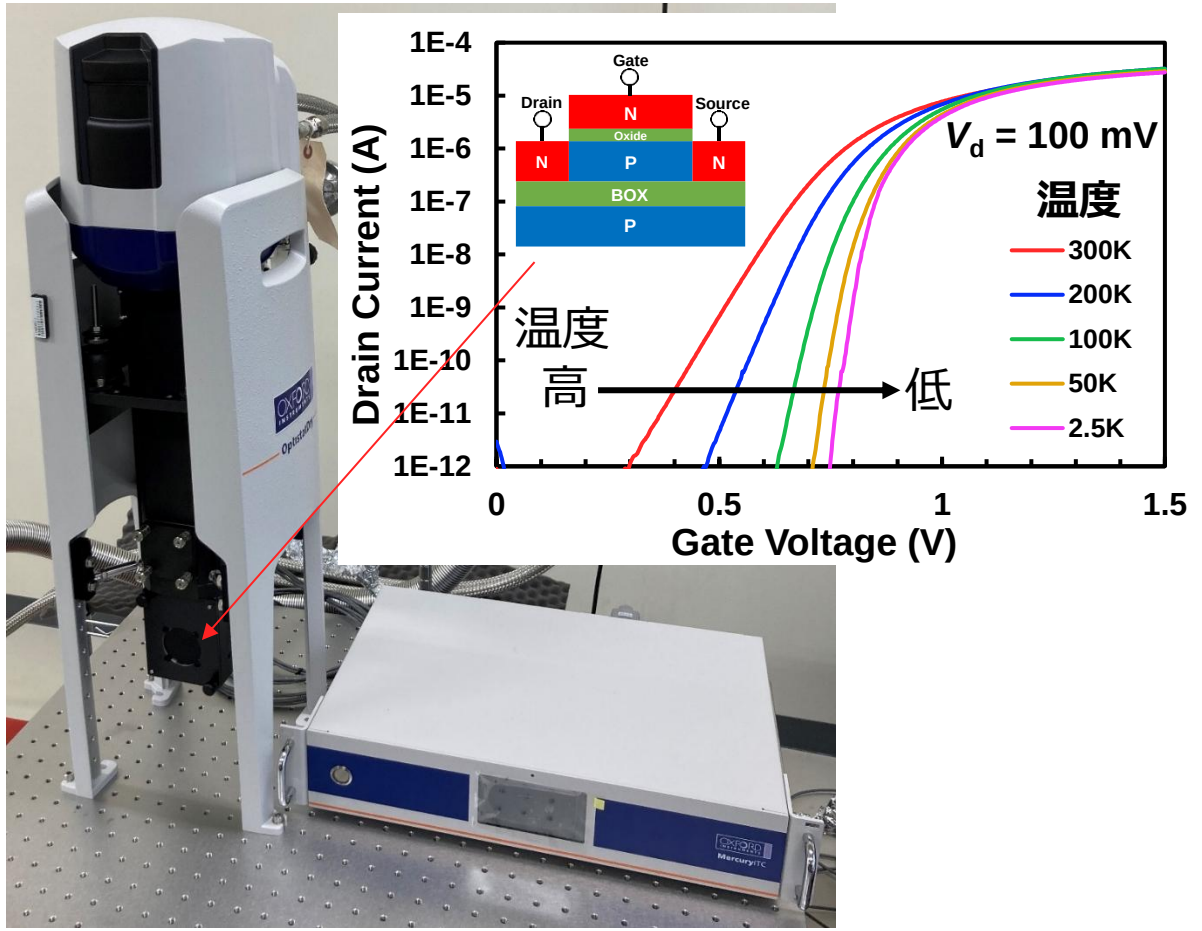
PN-Body Tied SOI-FET 及び Cyro-CMOSの研究進捗

金沢工業大学　森 貴之，井田 次郎

KIT Kanazawa Institute of Technology

研究内容





Steep Slope DeviceであるPN-Body Tied SOI-FET**と極低温下のSOI MOSFETについて研究**
(Cryo-CMOS)

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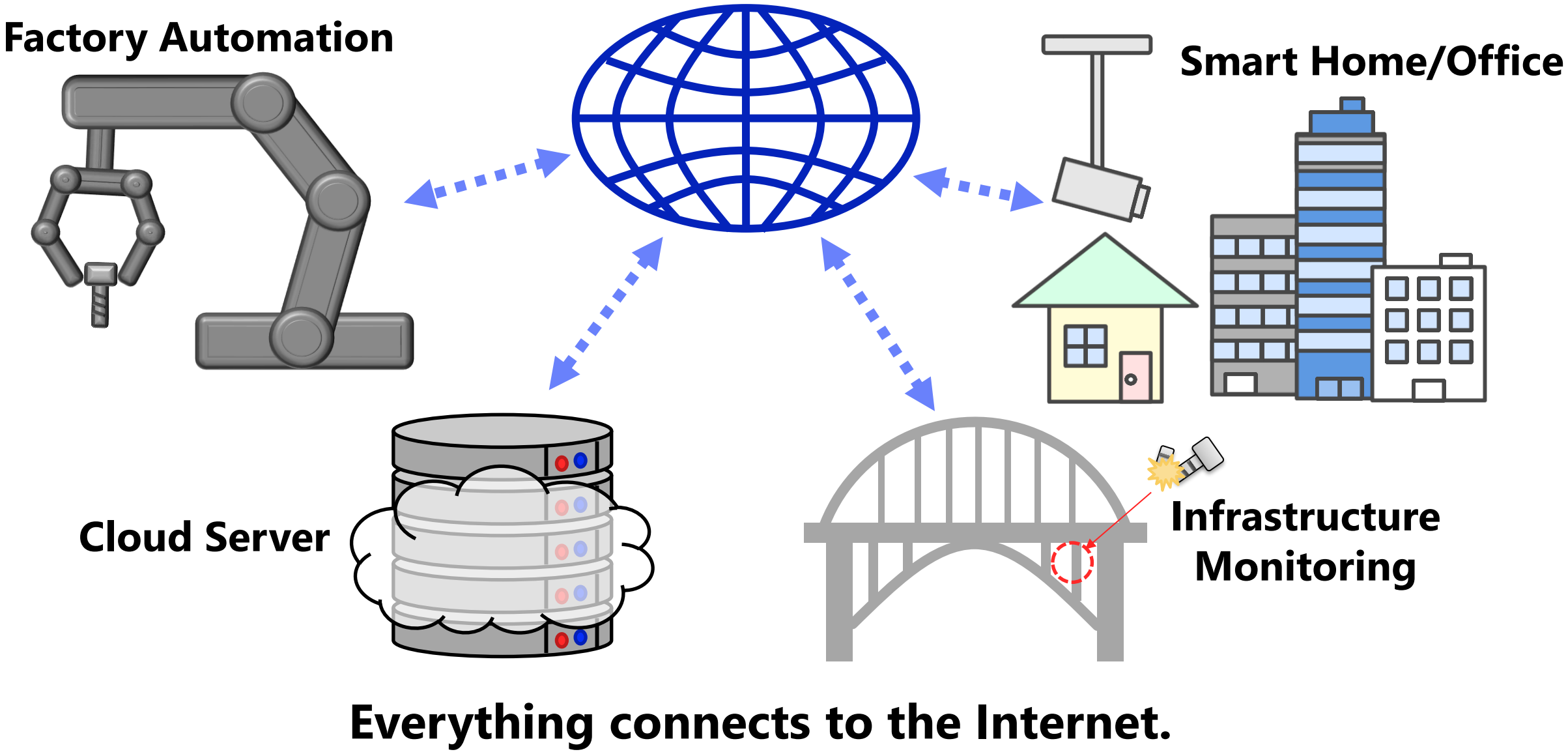
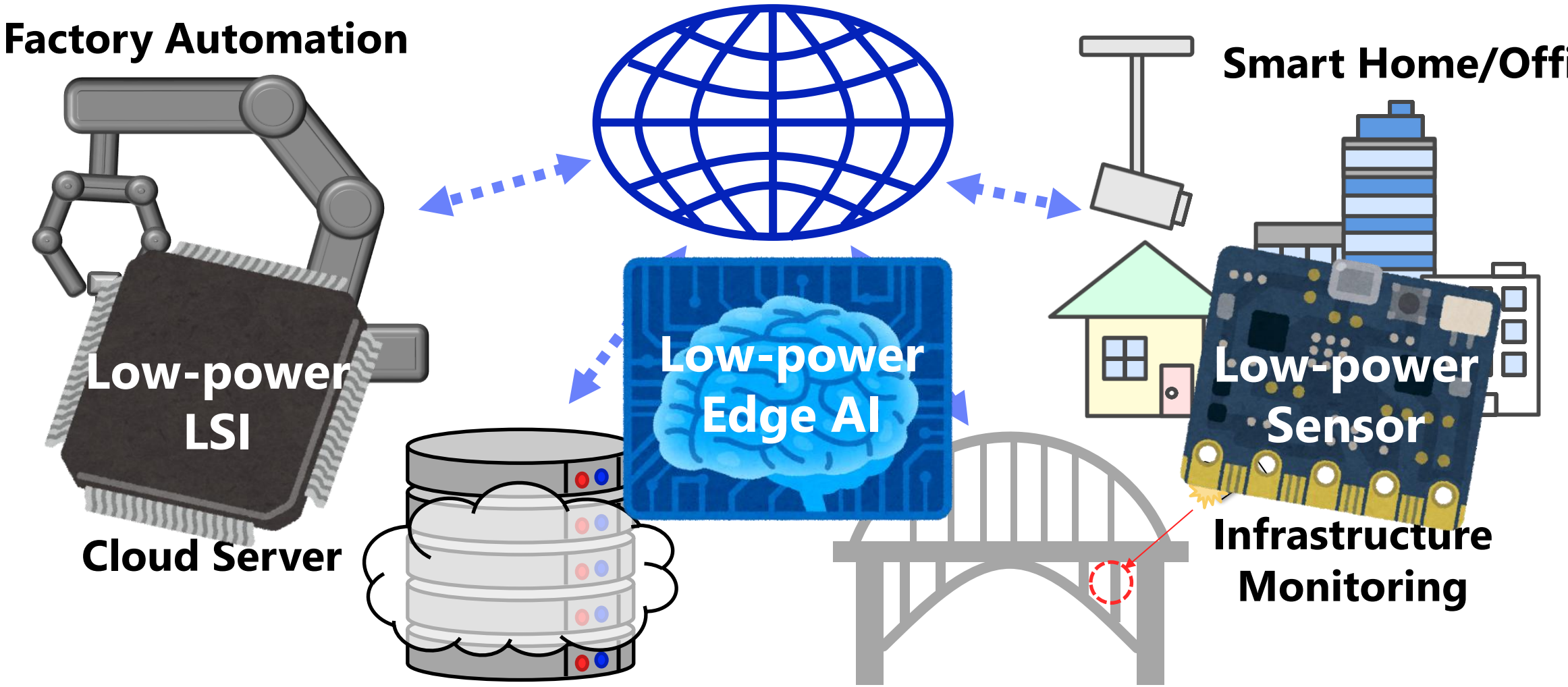
PN-Body Tied SOI-FET

研究背景



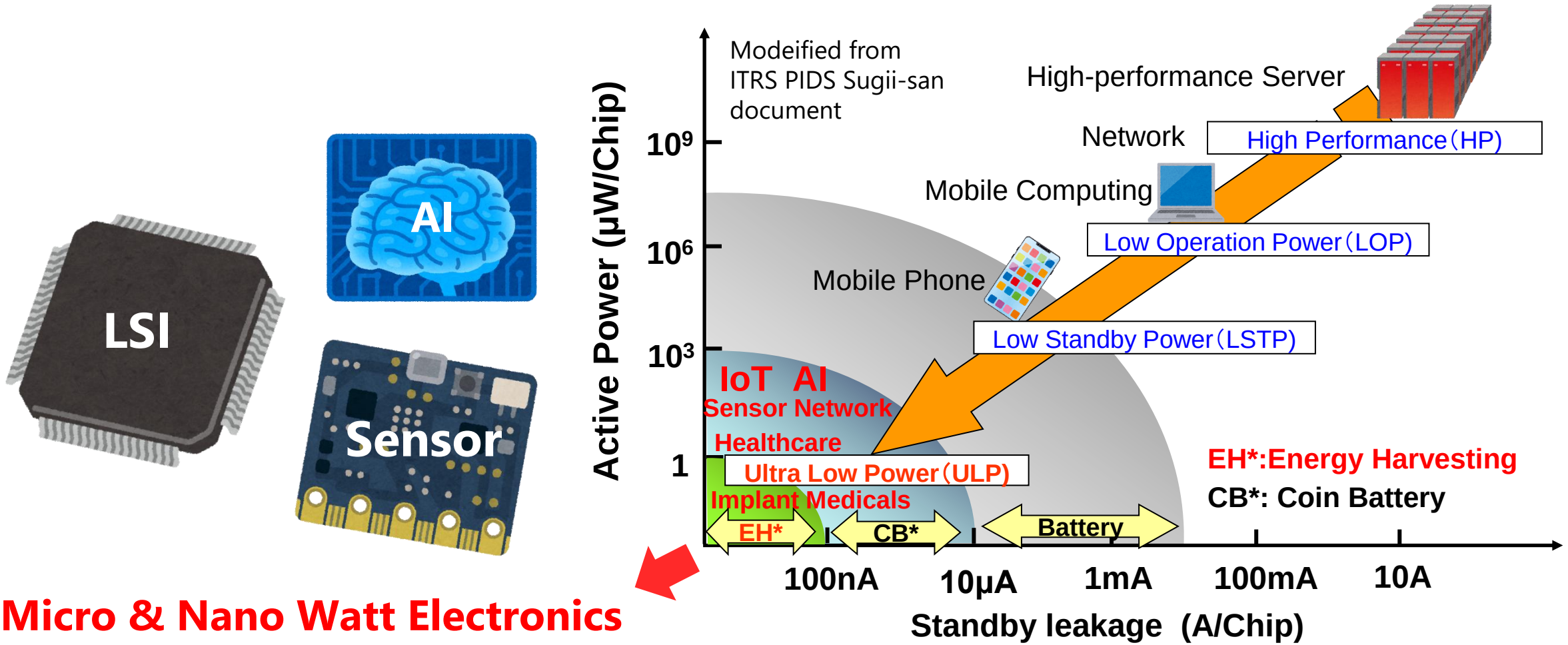
Everything connects to the Internet.

研究背景



Everything connects to the Internet.

極低消費電力LSIの必要性



大規模集積回路 (Large-Scale Integrated circuit : LSI)を
極低消費電力（バッテリーレス）で動作させなければならない

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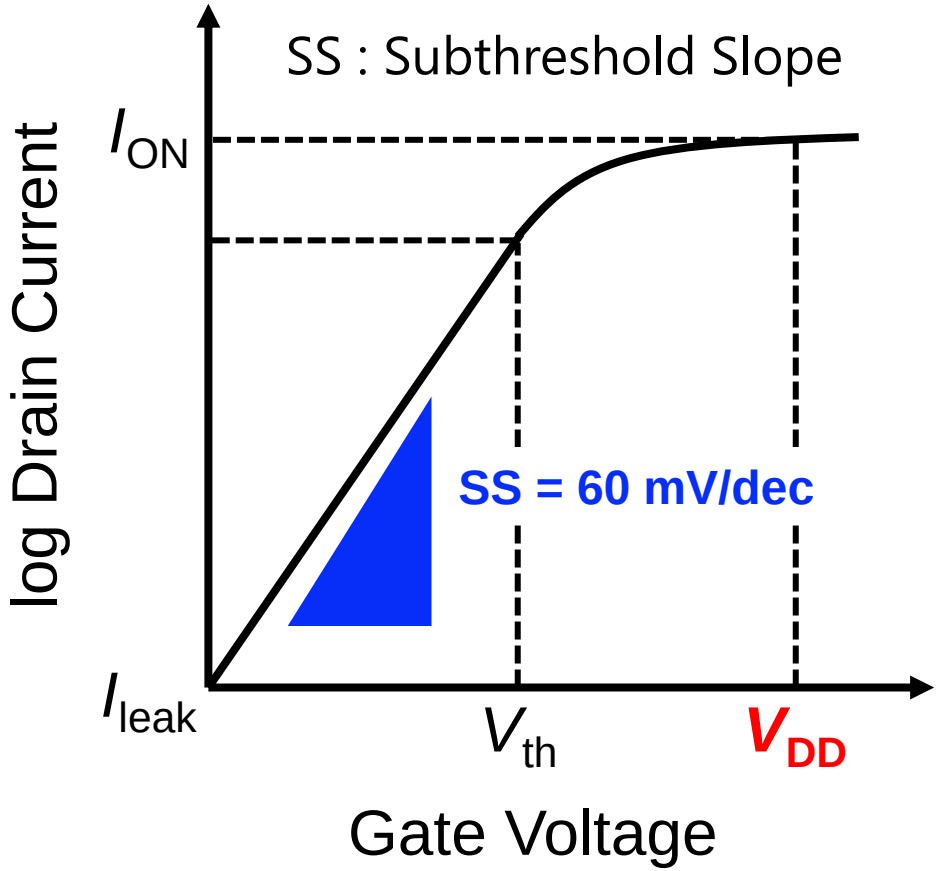
極低消費電力化に向けた MOSFET SS急峻化の必要性

Low supply voltage (V_{DD}) needs for low-power LSI



Power consumption of LSI

$$P_{\text{active}} \propto f \cdot C_{\text{load}} \cdot V_{\text{DD}}^2$$

$$P_{\text{standby}} \propto I_{\text{leak}} \cdot V_{\text{DD}}$$

Conventional MOSFET fundamental SS limitation (room temp.)

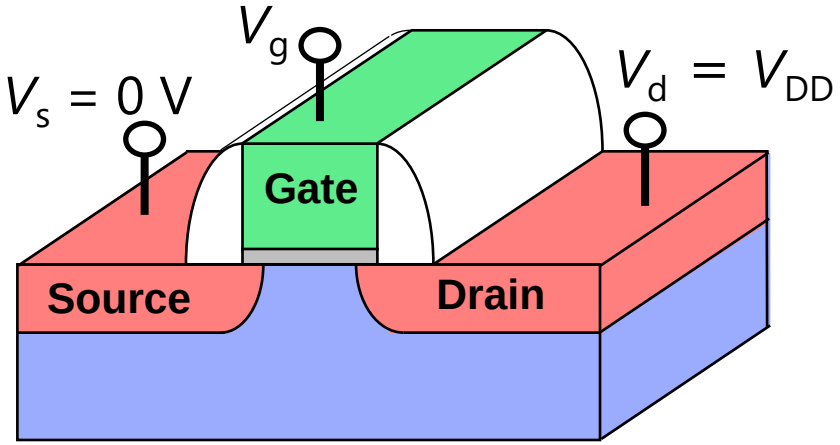
$$S = n\frac{kT}{q}\ln 10 \approx 60\,(\text{mV/dec})$$

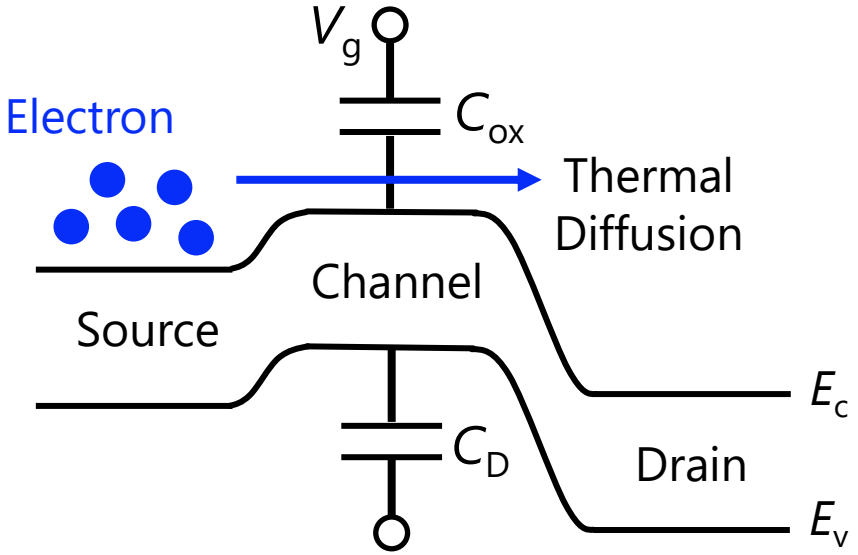
$$n = 1 + \frac{C_D}{C_{OX}}$$

Theoretical Limit

LSIの極低消費電力化にはSSの更なる急峻化が必要だが
従来のMOSFETには SSの理論下限が存在

極低消費電力化に向けた MOSFET SS急峻化の必要性





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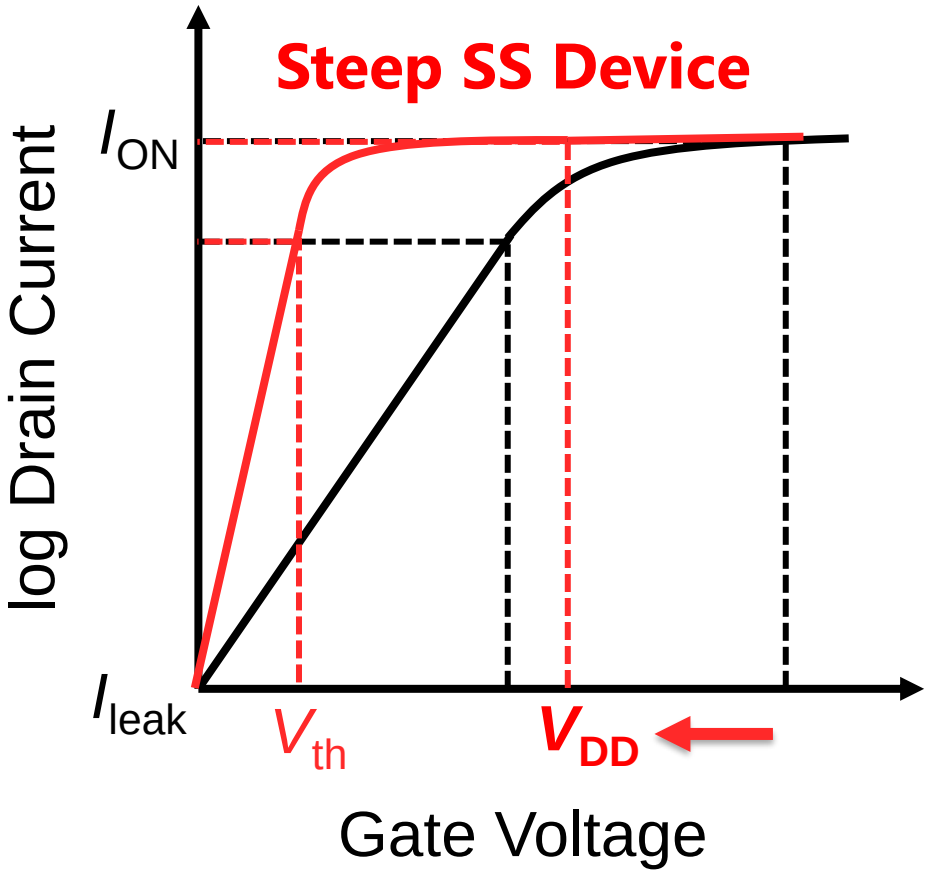
Steep subthreshold slope device



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Theoretical Limit

Steep Subthreshold Slope (SS) Device

従来のMOSFETとは異なる動作原理によるスイッチングが必要

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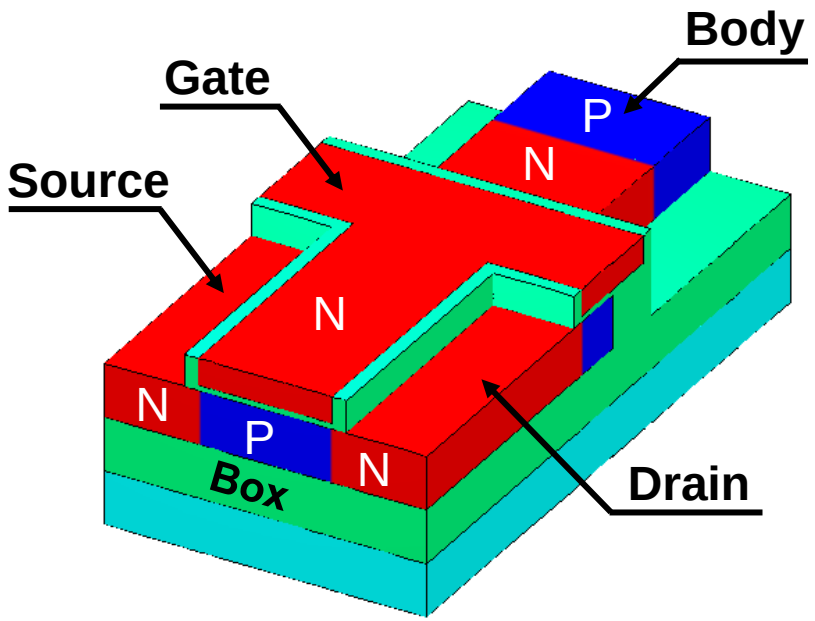
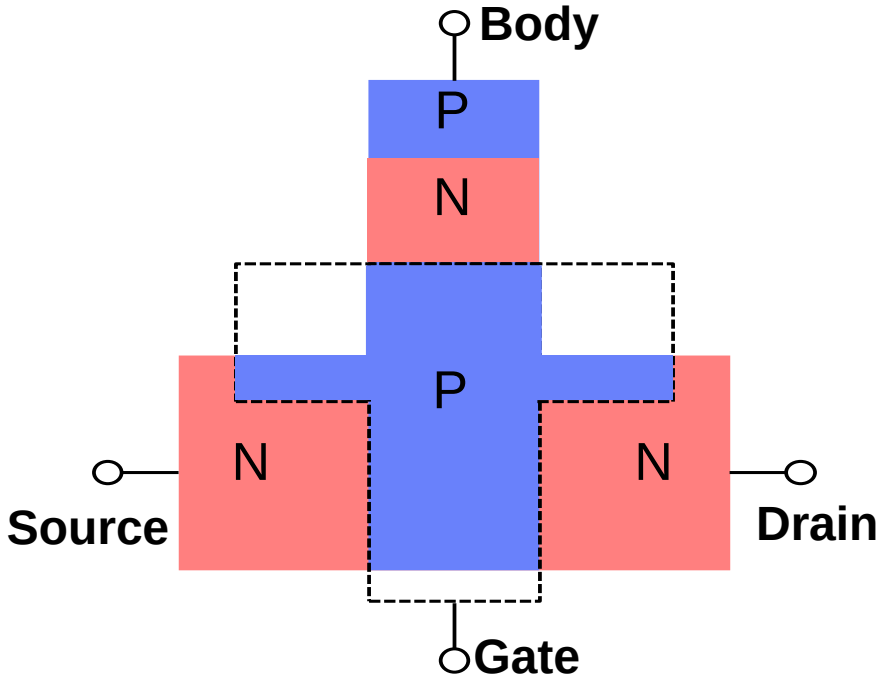
PN-Body Tied (PNBT) SOI-FET



Bird's eye view

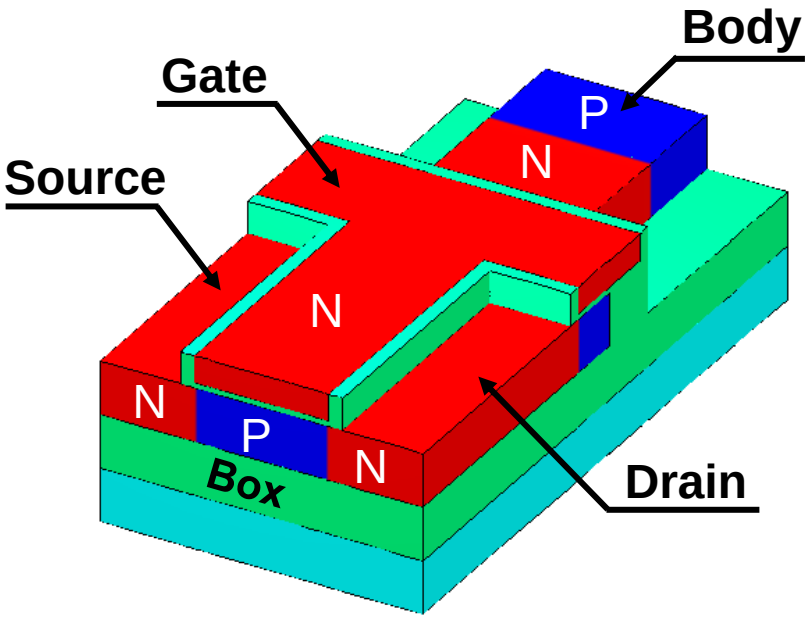


Top view

PNBT SOI-FET

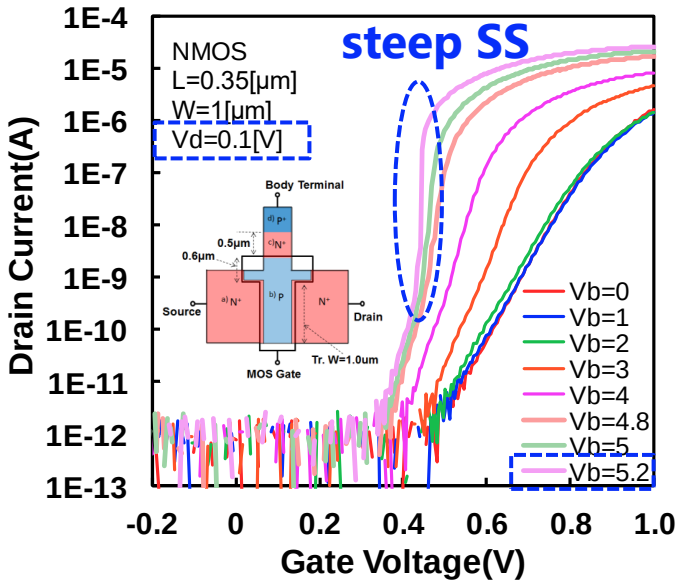
We proposed PN-Body Tied (PNBT) SOI-FET which has a **symmetry S/D** and demonstrated that PNBT SOI-FET has steep SS with **low drain voltage V_d (= 0.1 V).**

PN-Body Tied (PNBT) SOI-FET

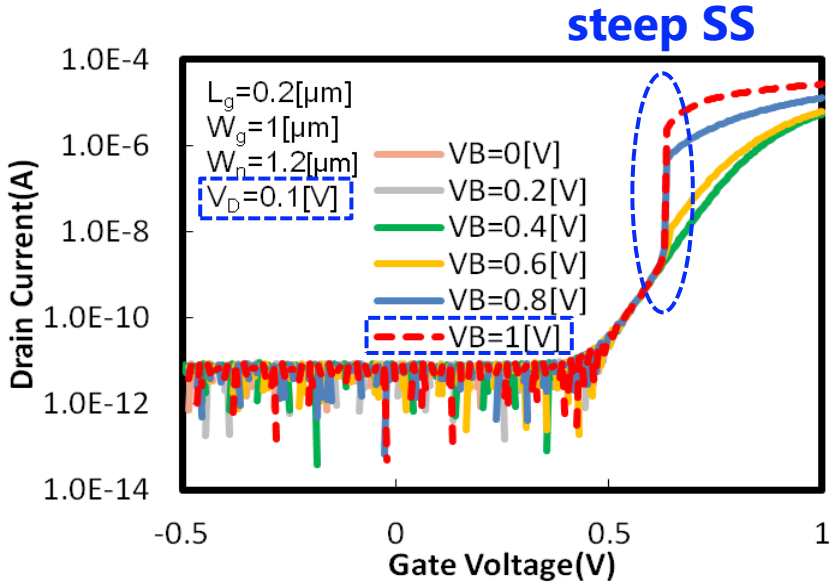


PNBT SOI-FET

J. Ida, *et al.*, *IEDM* 2015.



T. Yoshida *et al.*, *S3S* 2016.



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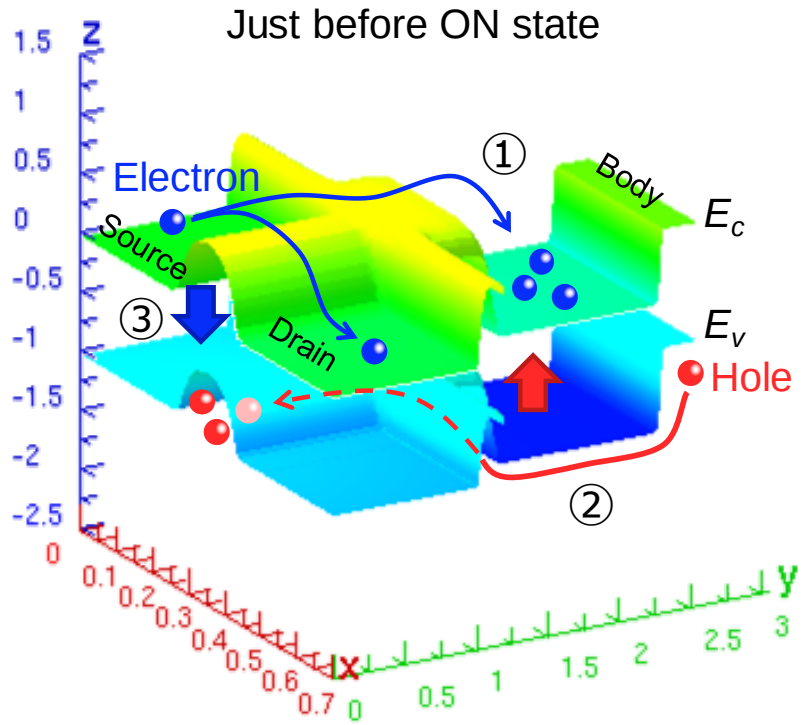
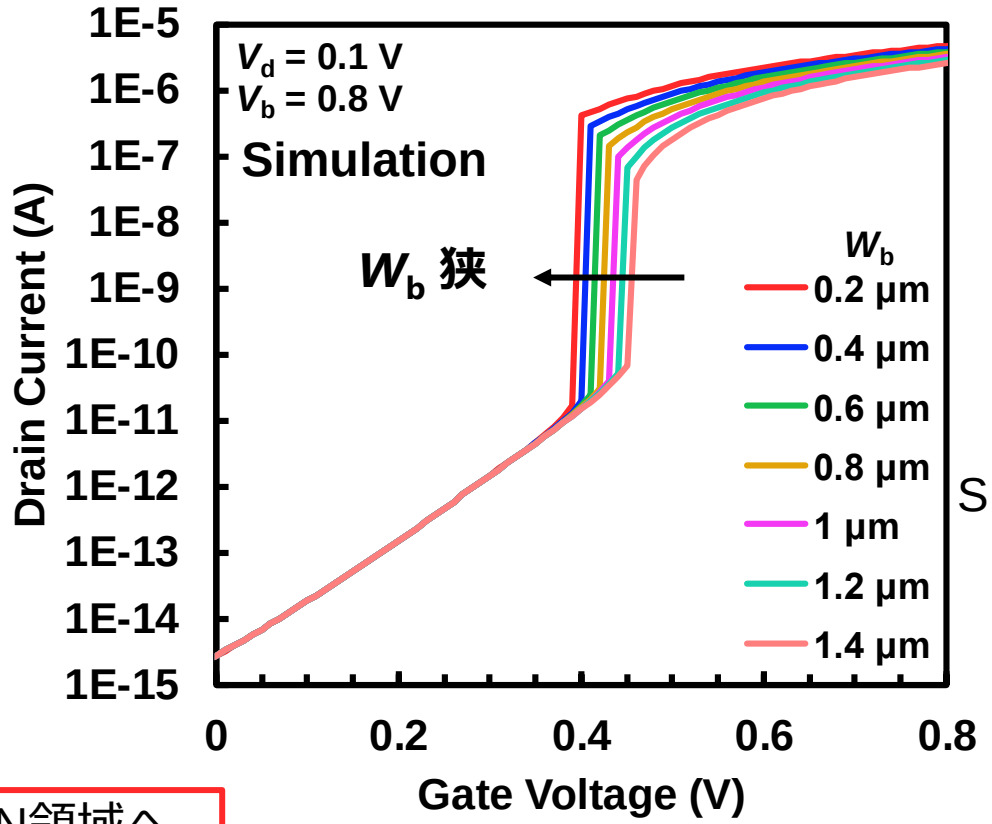
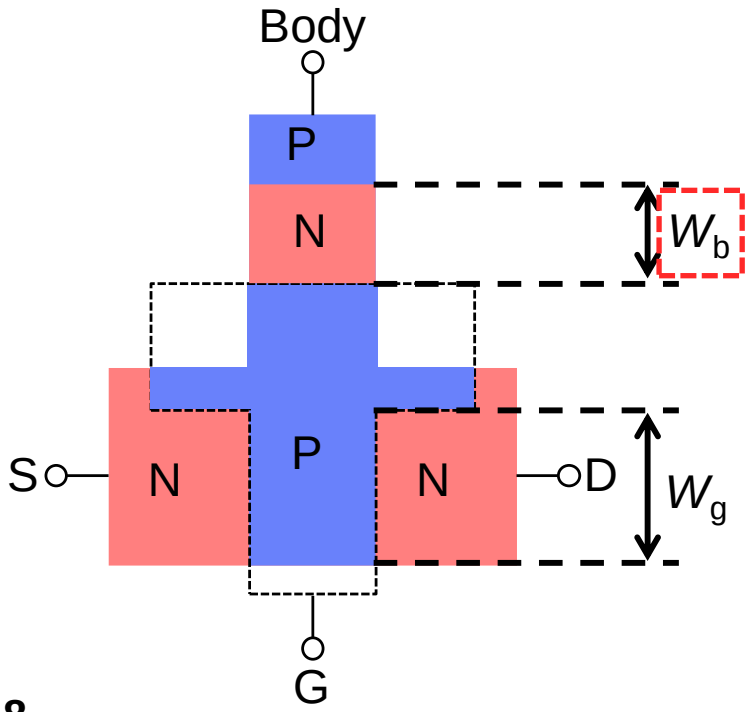
動作原理・デバイスパラメータ依存性の例







1. 電子がDrain及びBody方向に拡散しN領域へ
2. N領域の電子によってBody-channel間の電位障壁が減少、正孔がchannel下部へ
3. channel下部に蓄積した正孔がSource-Drain/Body間の電位障壁を下げる

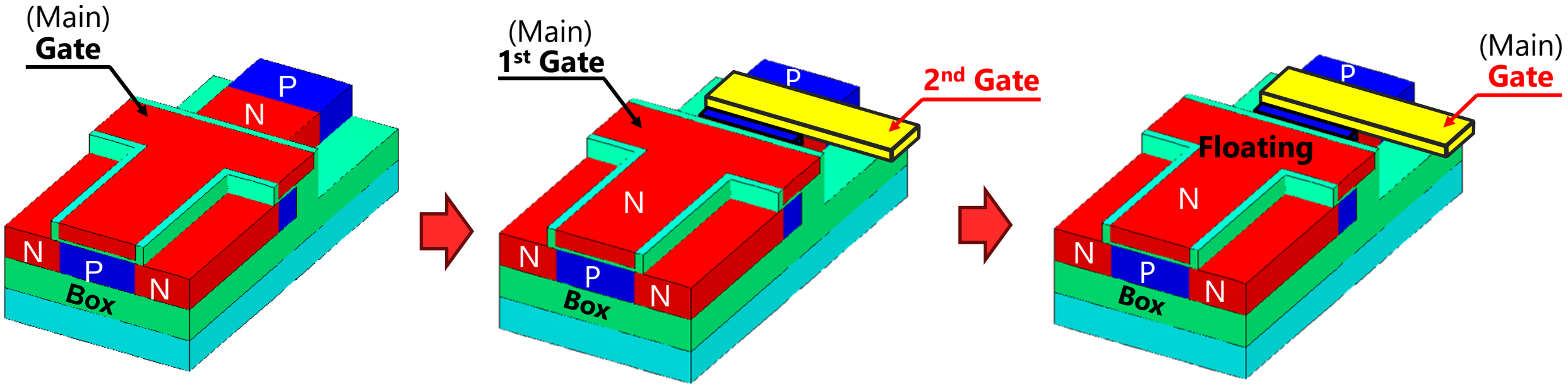
T. Mori *et al.*, *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1213–1219, Oct. 2018.

W_bが狭いほどI_{on}/I_{off}比増大かつ低いV_gで立ち上がる

T. Mori *et al.*, SSDM, pp. 839–840, Sep. 2018.

性能改善に向けたデバイス構造、動作原理解明について研究

PNBT SOI-FETの進歩



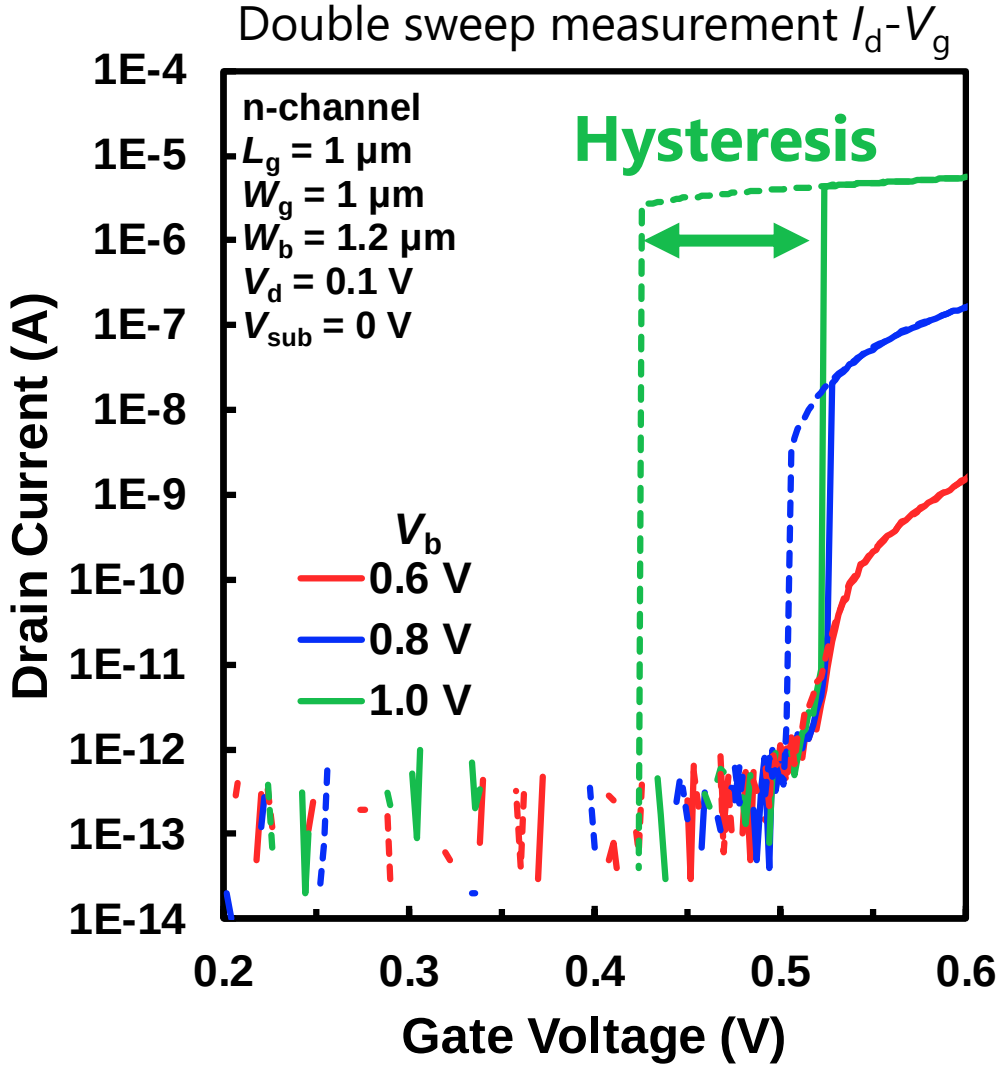
Single Gate PNBT SOI-FET (SG PNBT SOI-FET)

Dual Gate PNBT SOI-FET (DG PNBT SOI-FET)

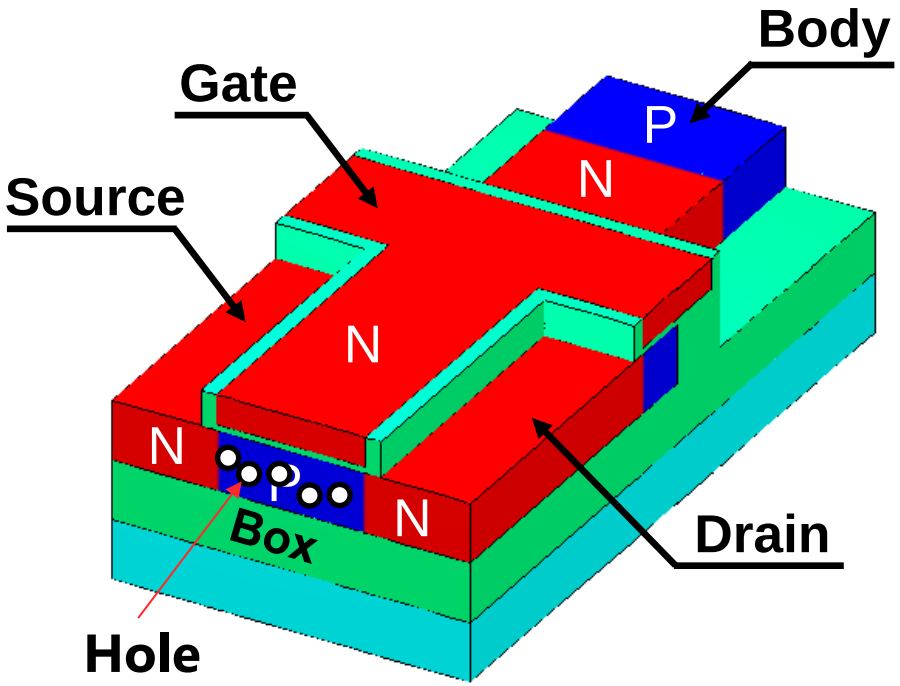
Gate-Controlled Carrier-Injection SOI-Tr (GCCI SOI-Tr)

SG・DG PNBT SOI-FETにおけるArイオン注入効果とGCCI SOI-Trについて紹介

Issue of PNBT SOI-FET | Hysteresis characteristics



Solid line : forward scan
Dotted line : backward scan



Channel potential is maintained by accumulated carriers.

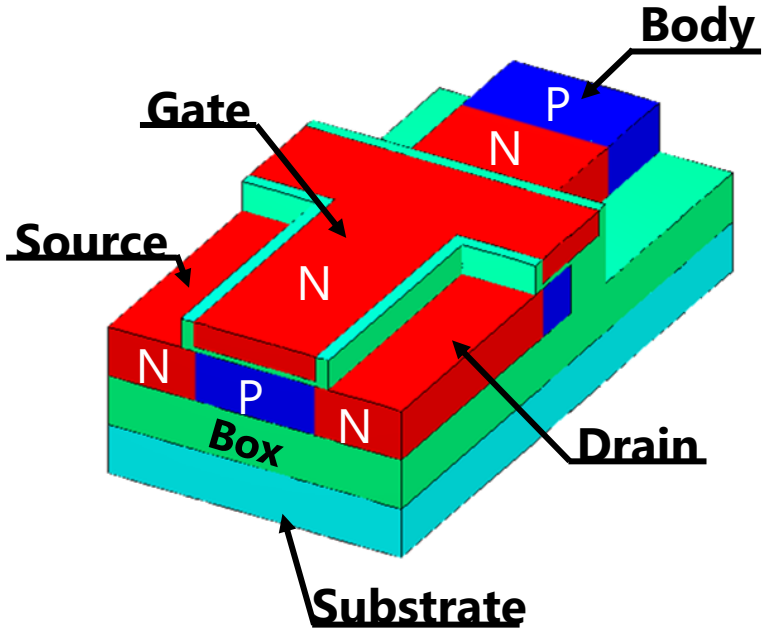
Hysteresis characteristics appear.

T. Mori and J. Ida, *IEEE J-EDS*, Oct. 2018.

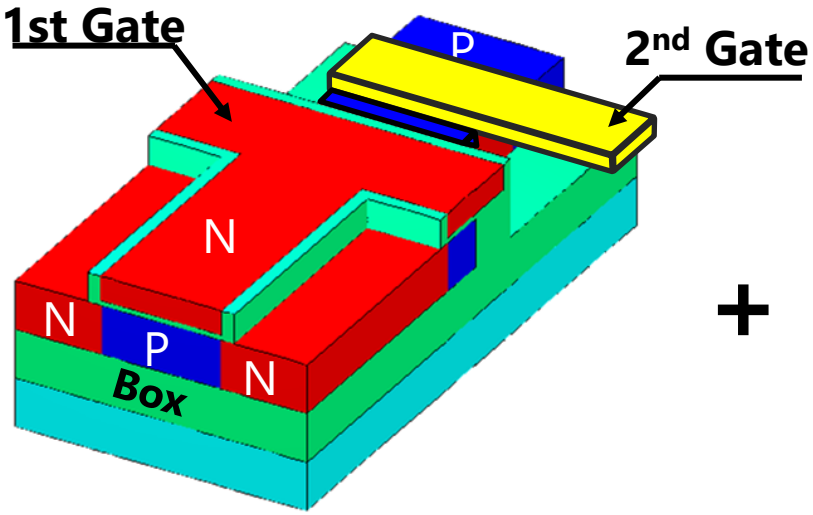
Arイオン注入によるヒステリシス制御

Decreasing (controlling) hysteresis characteristics is necessary.

show Ar-ion implantation effect on single-gate and dual-gate PNBT SOI-FETs.

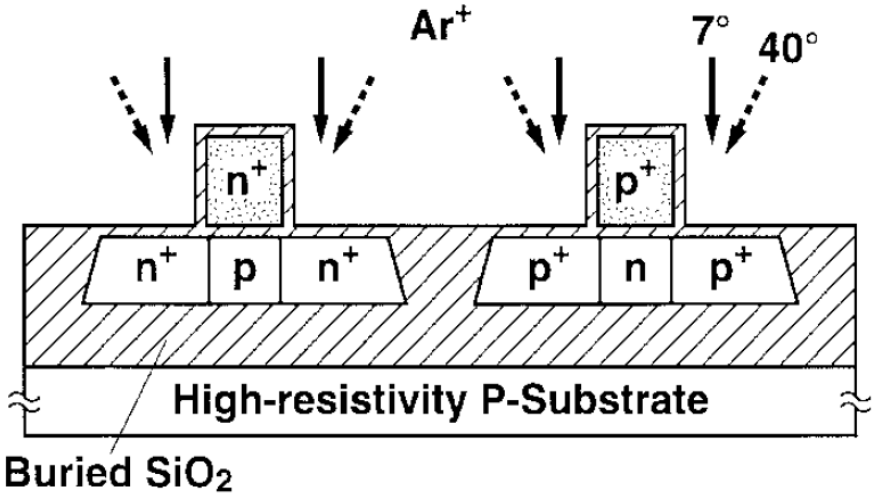


Single-gate



Dual-gate

+

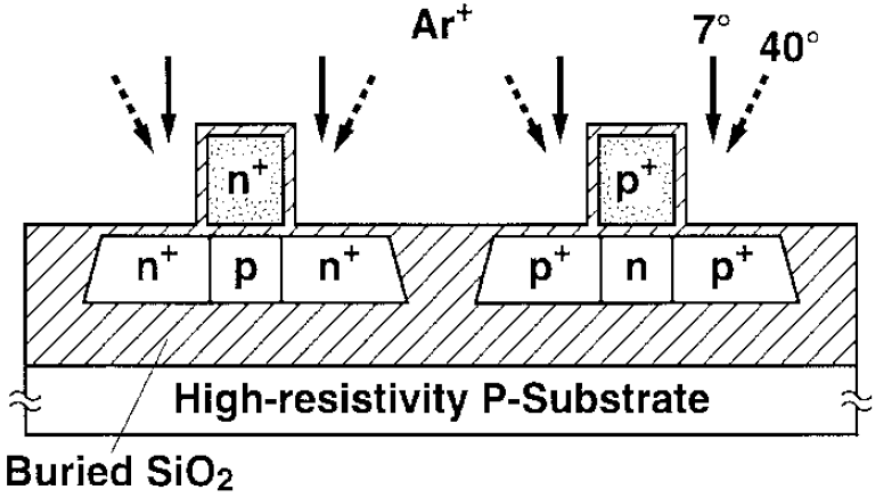


T. Ohno, *et al.*, *IEEE T-ED*, May 1998.
NTT

Ar-ion implantation

Arイオン注入の効果

To suppress floating body effect



T. Ohno, *et al.*, *IEEE T-ED*, May 1998.
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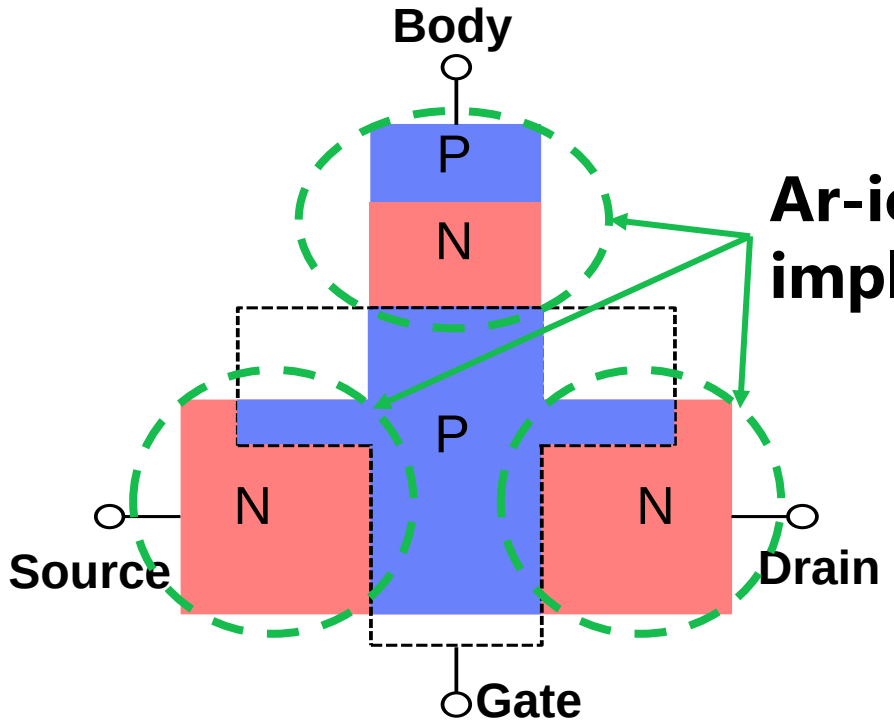
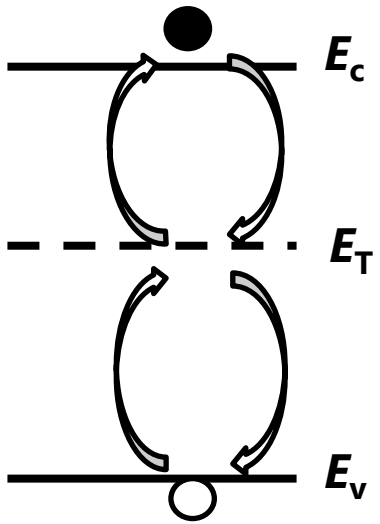


Ar-ion implantation creates recombination centers, which act as lifetime killers.



Ar-ions were implanted after gate formation to reduce hysteresis.
(Ar-ions were not implanted to gate region)

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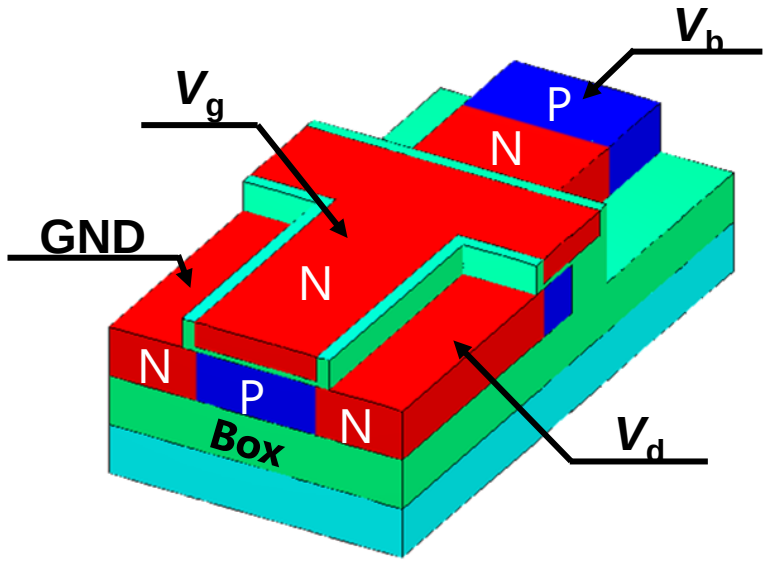
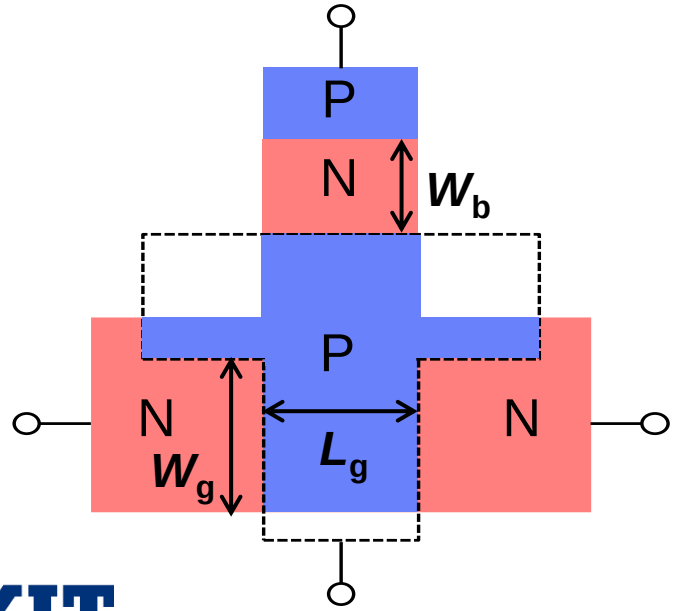
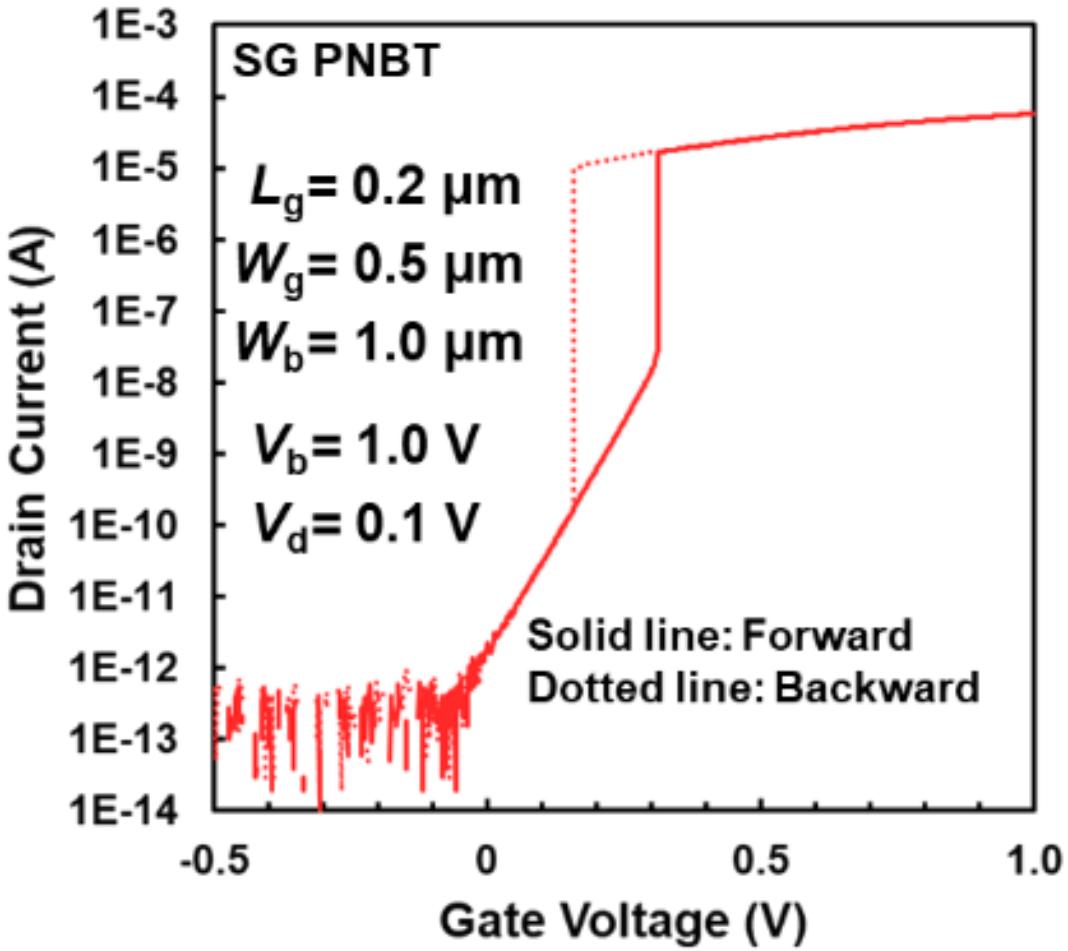
Single-gate PNBT SOI-FET | no dose



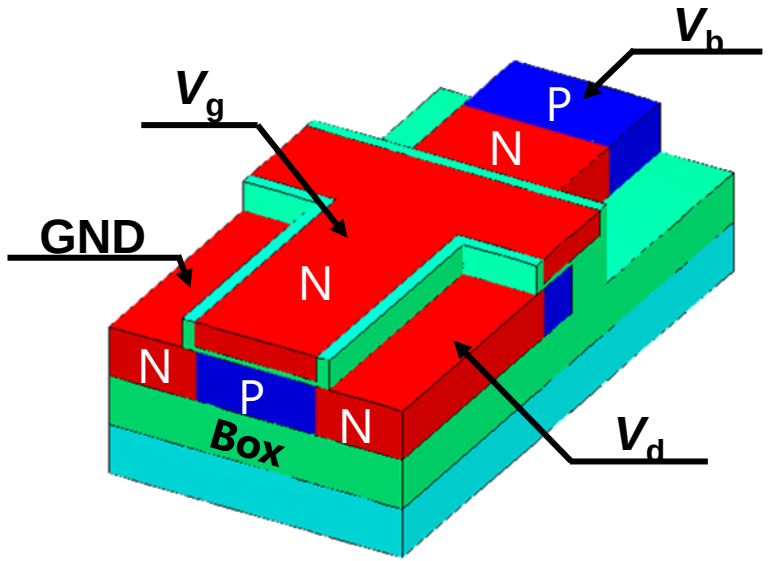


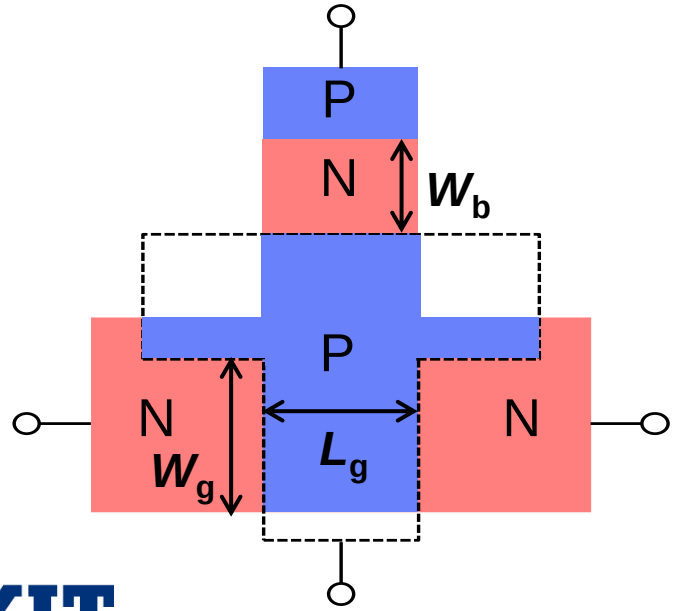


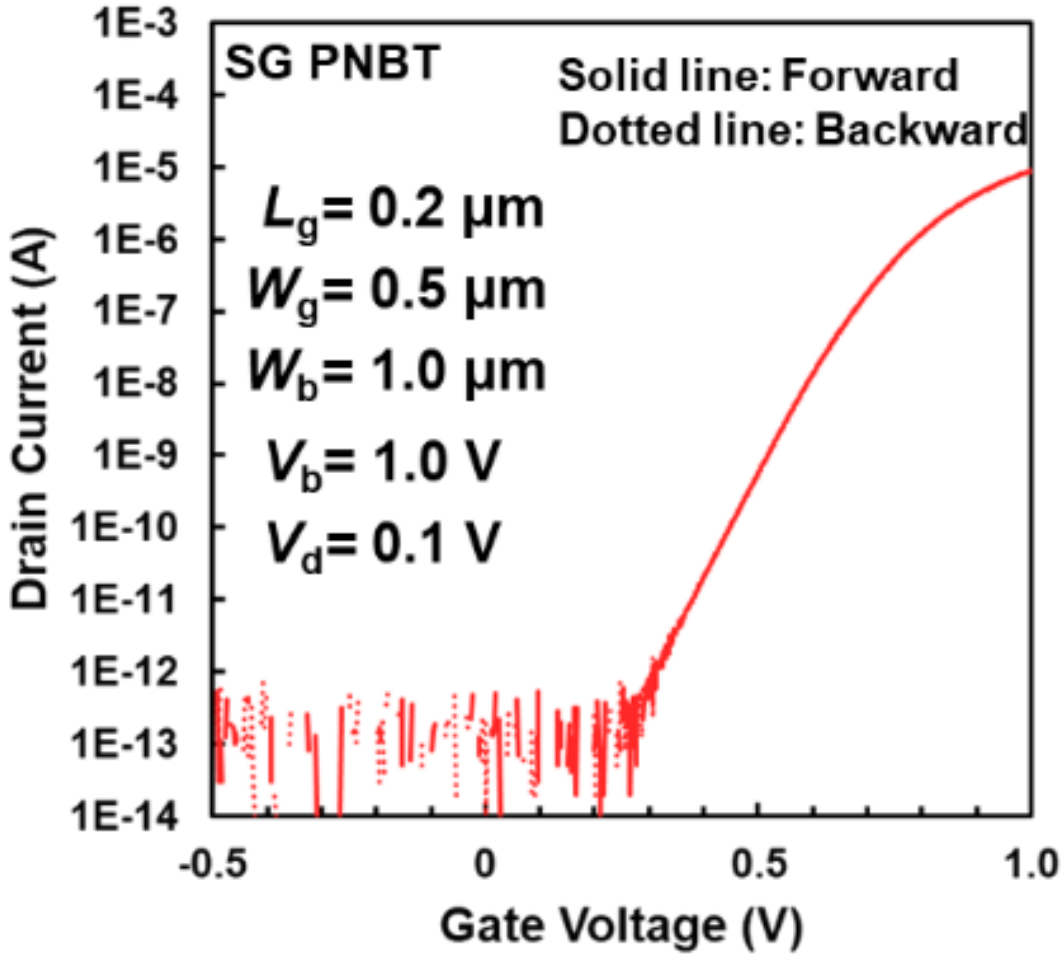
Steep SS and hysteresis occur.

Single-gate PNBT SOI-FET | with dose

R. Ito *et al.*, IIT 2024.



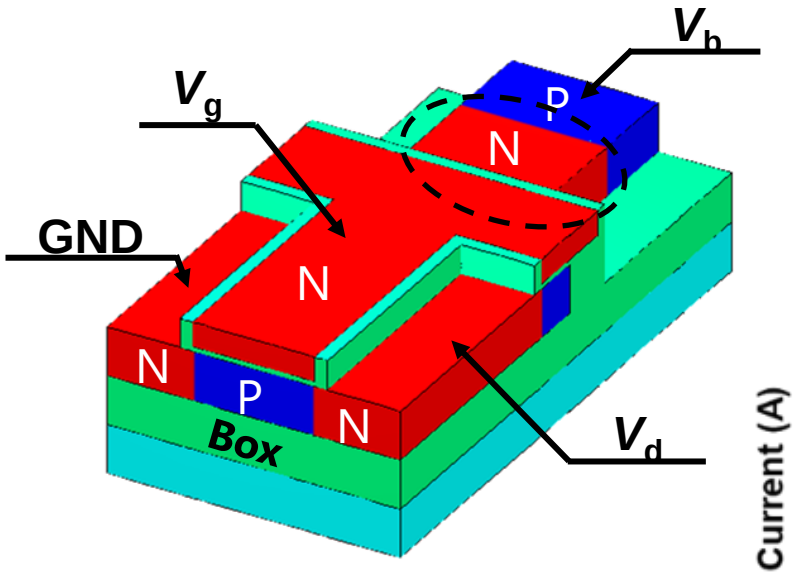


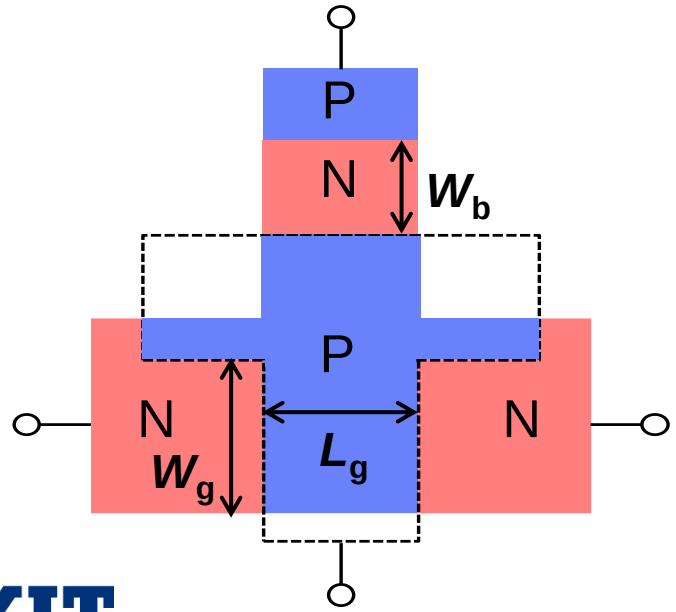


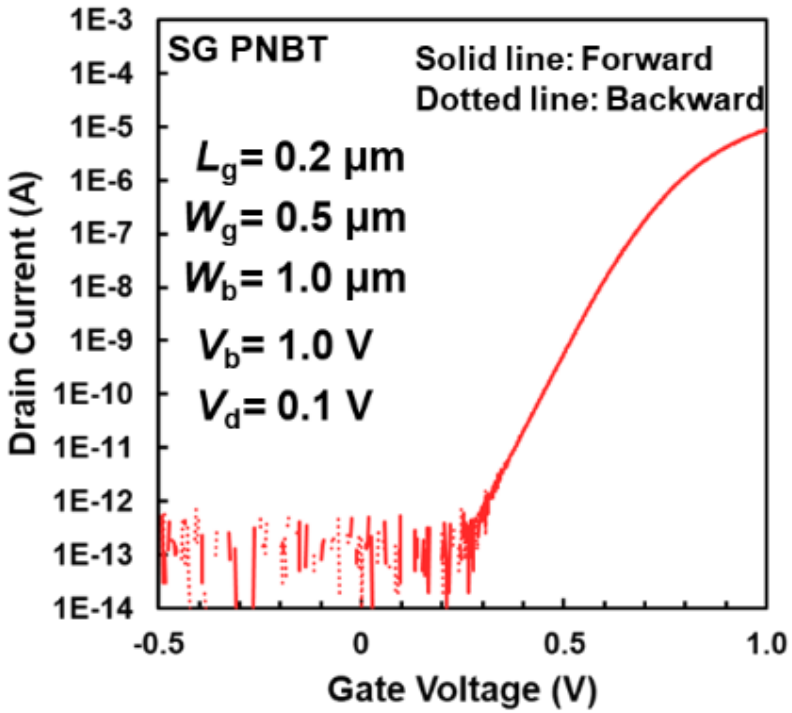
Hysteresis disappears but, steep SS also disappears.

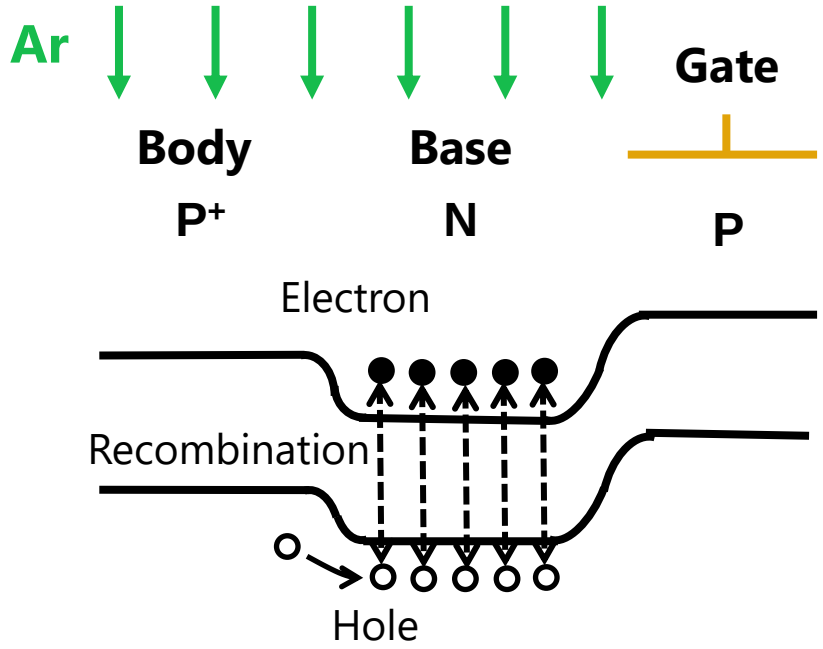
Single-gate PNBT SOI-FET | with dose

R. Ito *et al.*, IIT 2024.







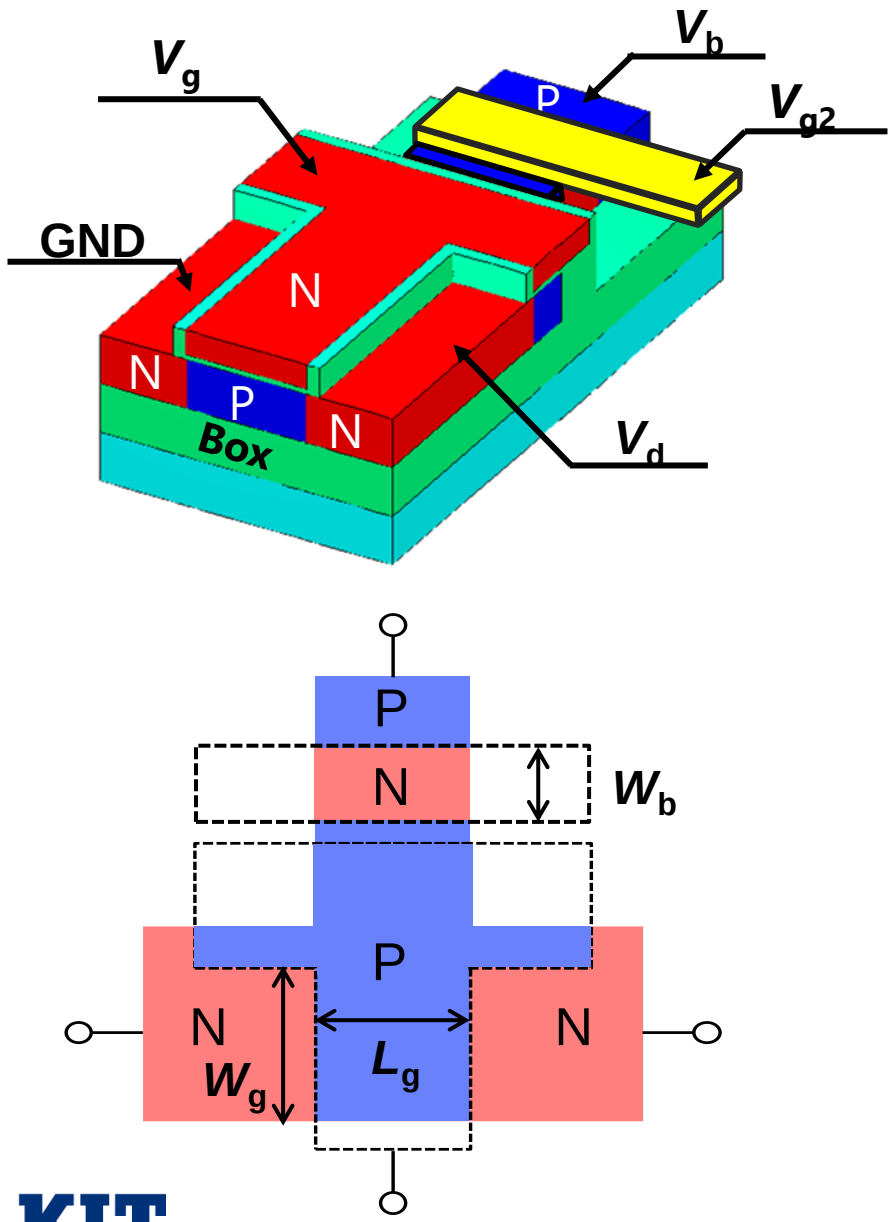


High Ar dose induces high recombination rate.

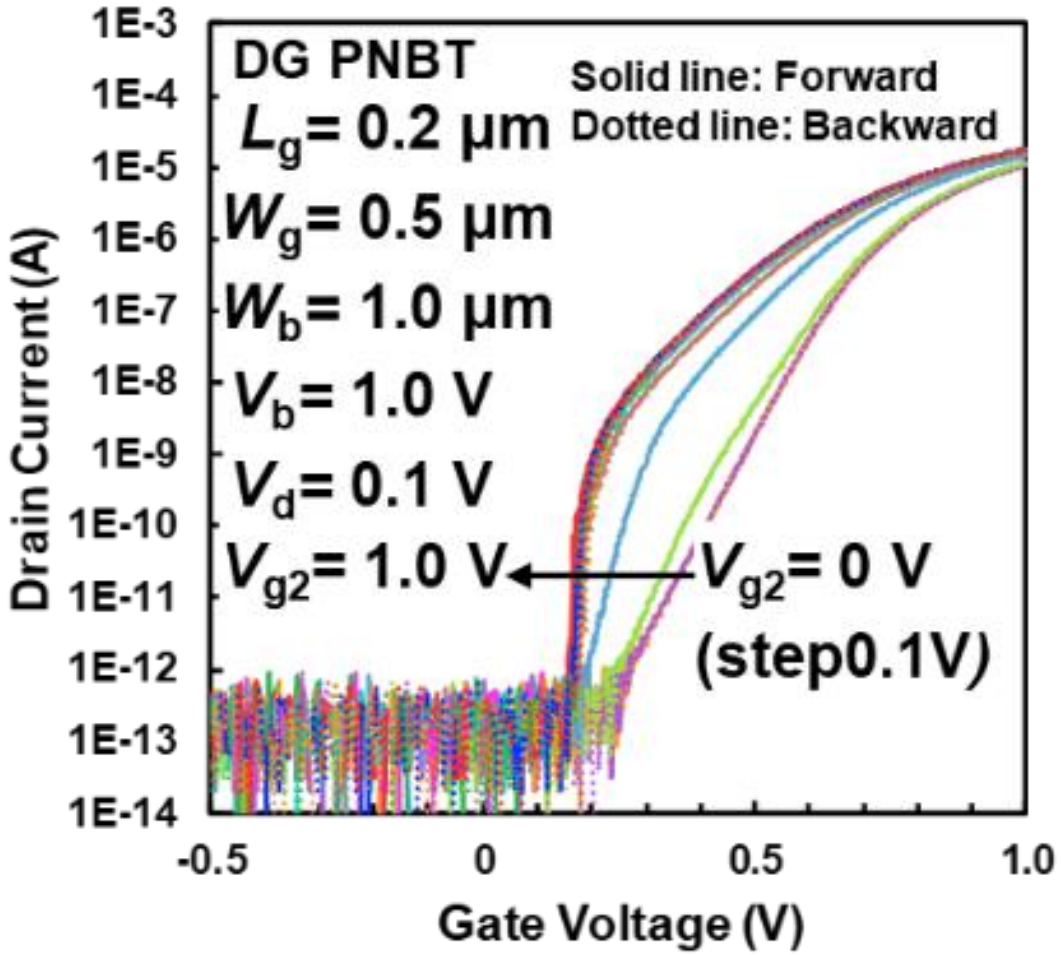
carrier injection efficiency decreases, and steep SS disappears.

Dual-gate PNBT SOI-FET | with dose

R. Ito *et al.*, IIT 2024.



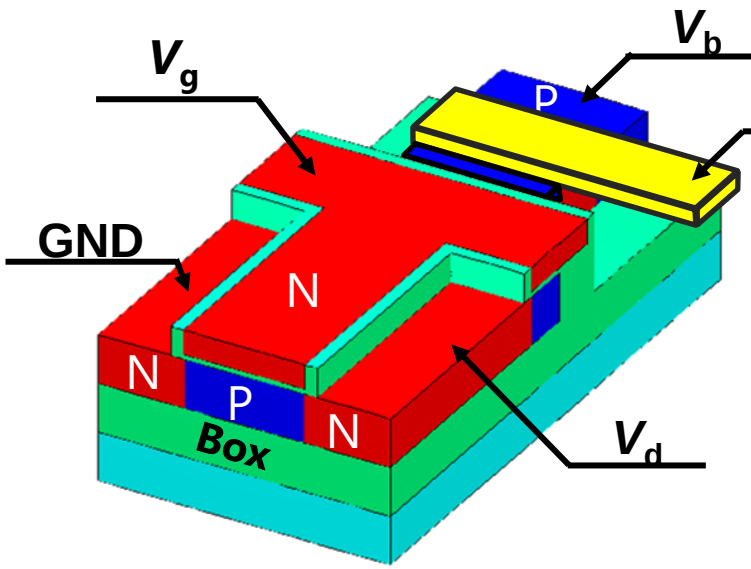
DG PNBT SOI-FET has an additional 2nd gate which can control potential of N-body region.

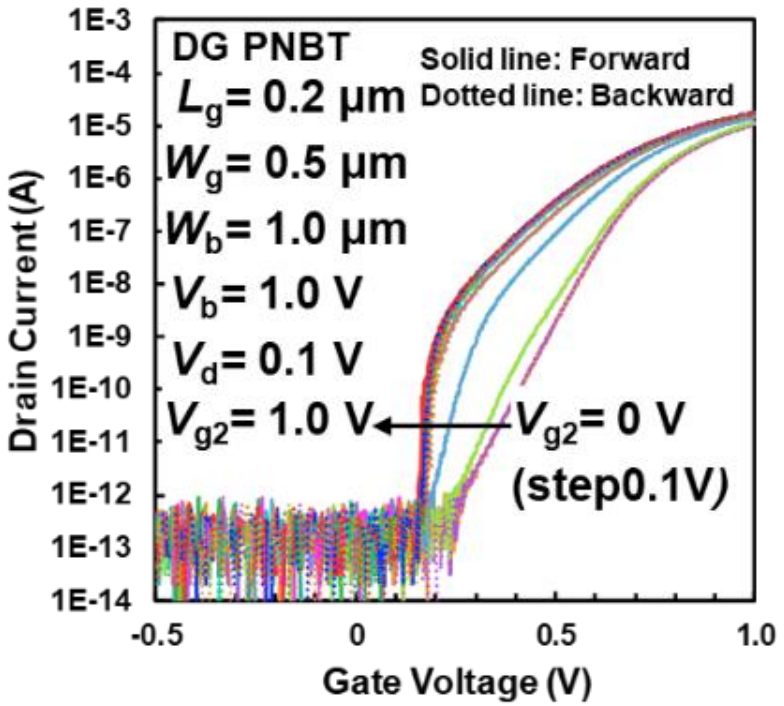


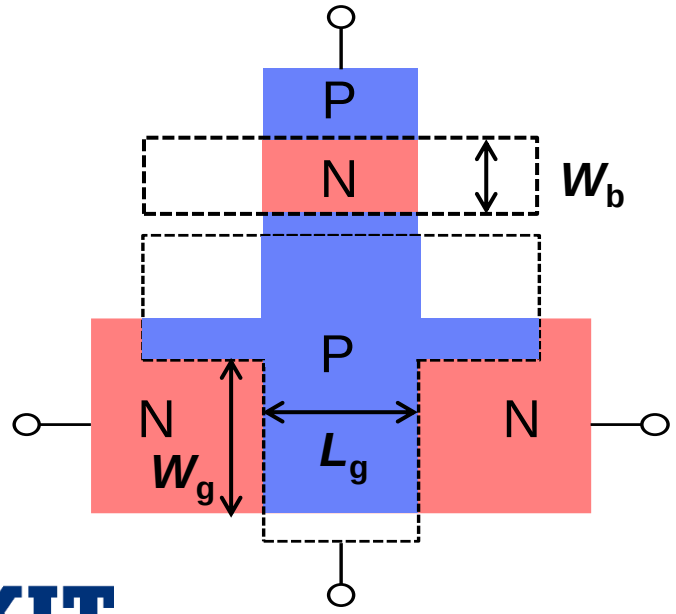
Steep SS occur without hysteresis !

Dual-gate PNBT SOI-FET | with dose

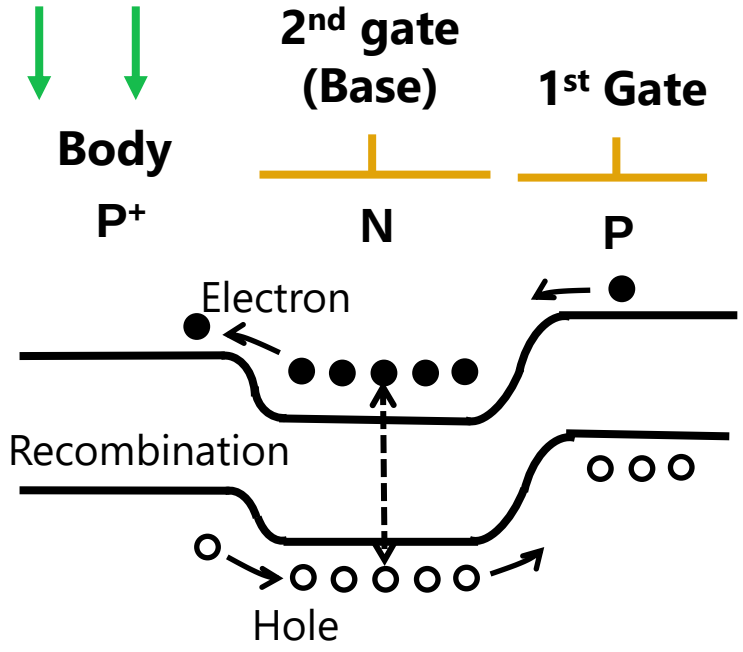
R. Ito *et al.*, IIT 2024.

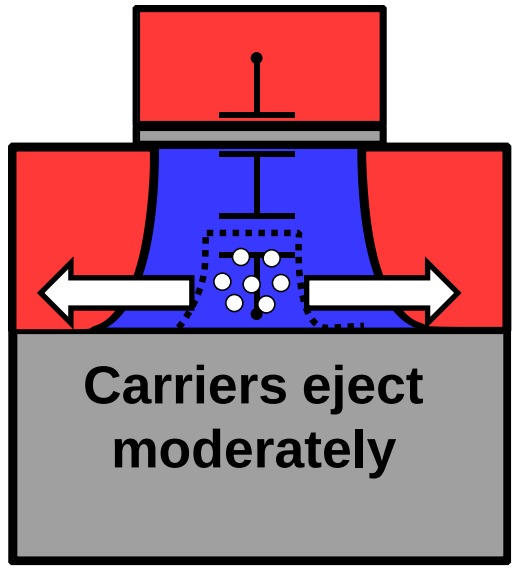






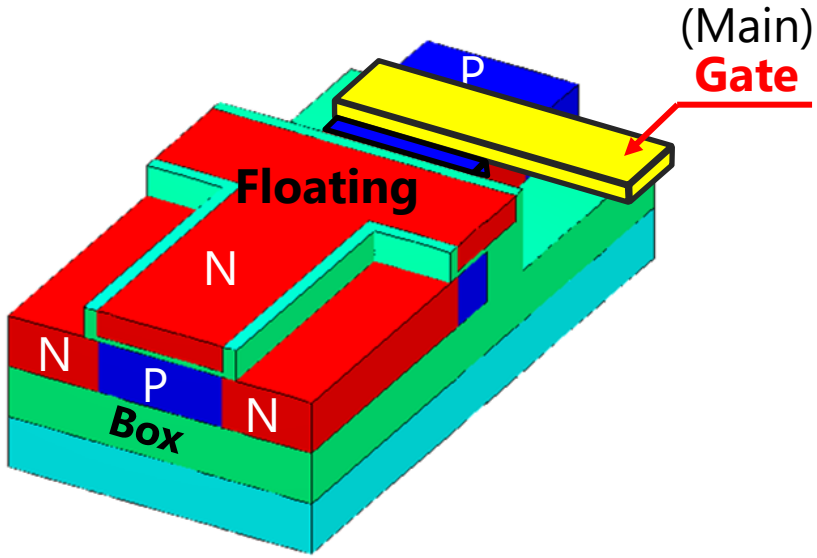
DG PNBT SOI-FET achieves moderately positive feedback.



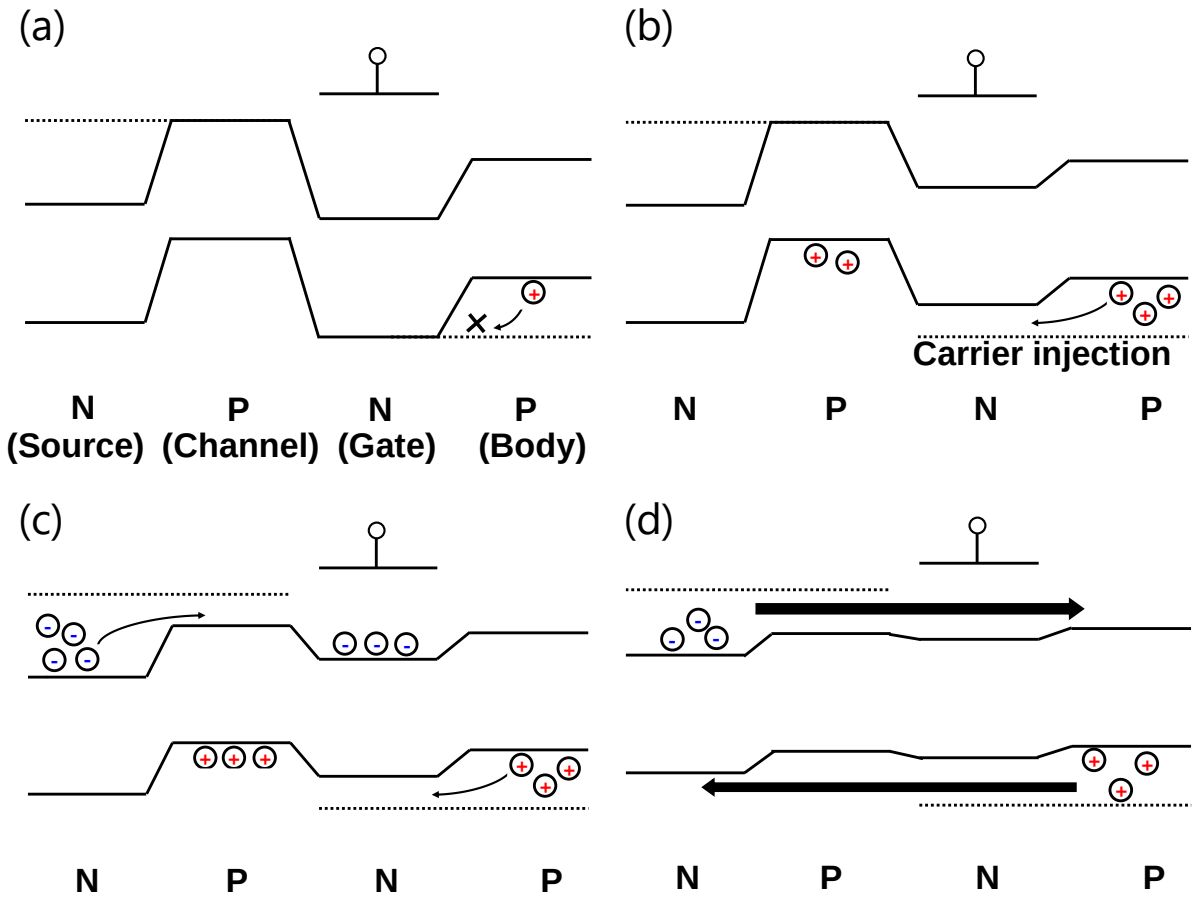


Gate-Controlled Carrier-Injection SOI-Tr

H. Yonezaki et al., EDTM 2024



Gate-Controlled Carrier-Injection SOI-Tr
(GCCI SOI-Tr)

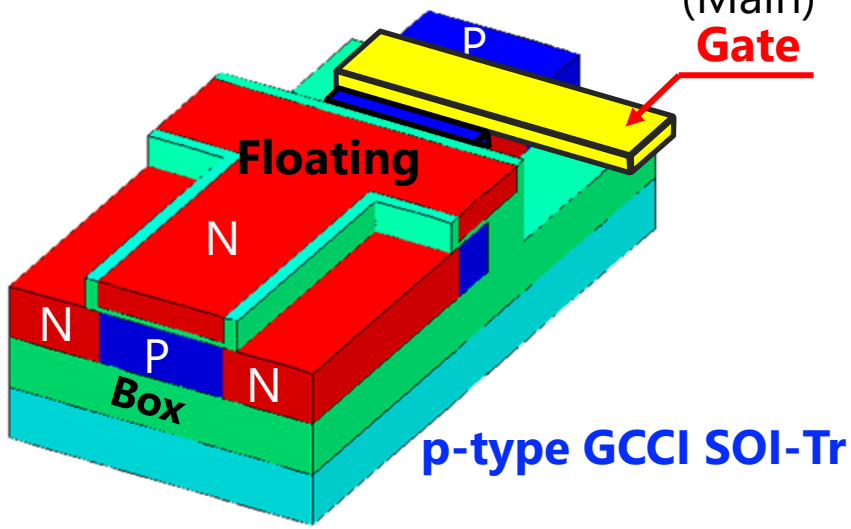


想定動作メカニズム

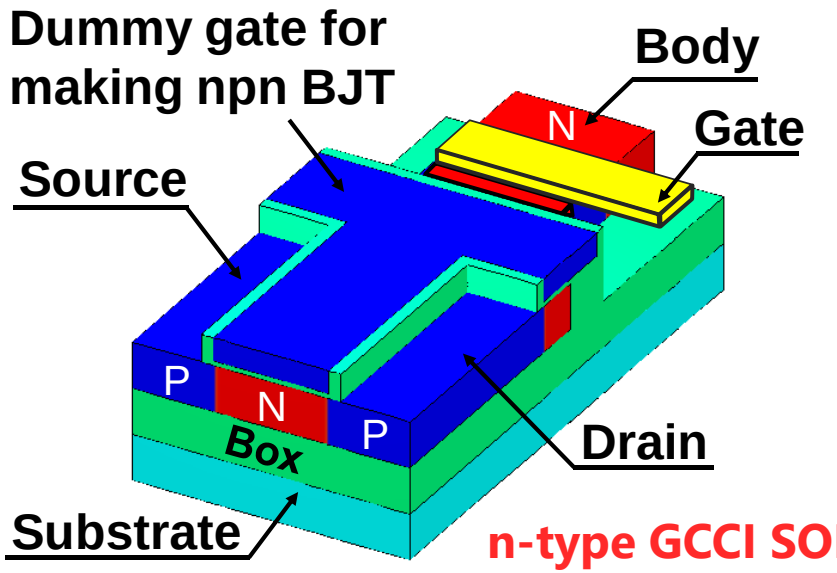
DG PNBT SOI-FETの2nd Gateをメインの Gateとして扱う（1st GateはFloating）
使用端子数減、制御の単純化が見込める

GCCI SOI-Tr 伝達特性

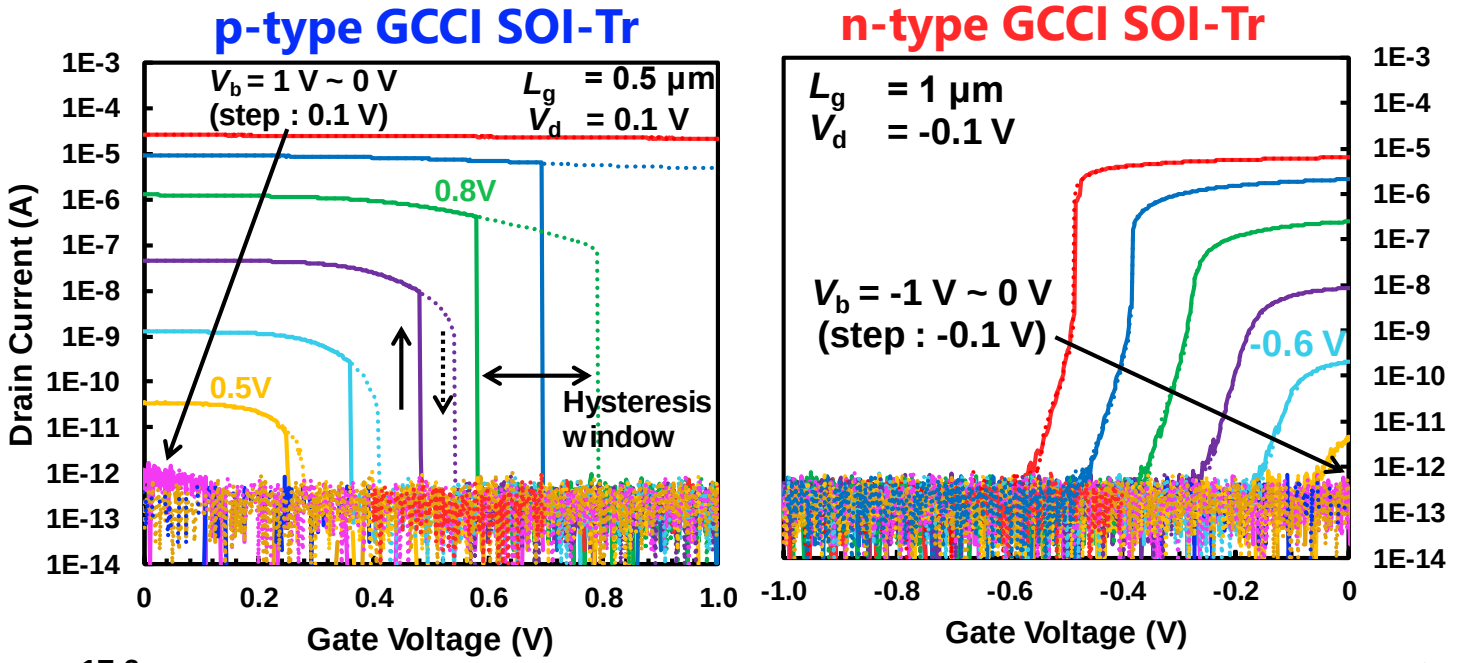
H. Yonezaki et al., SNW 2024

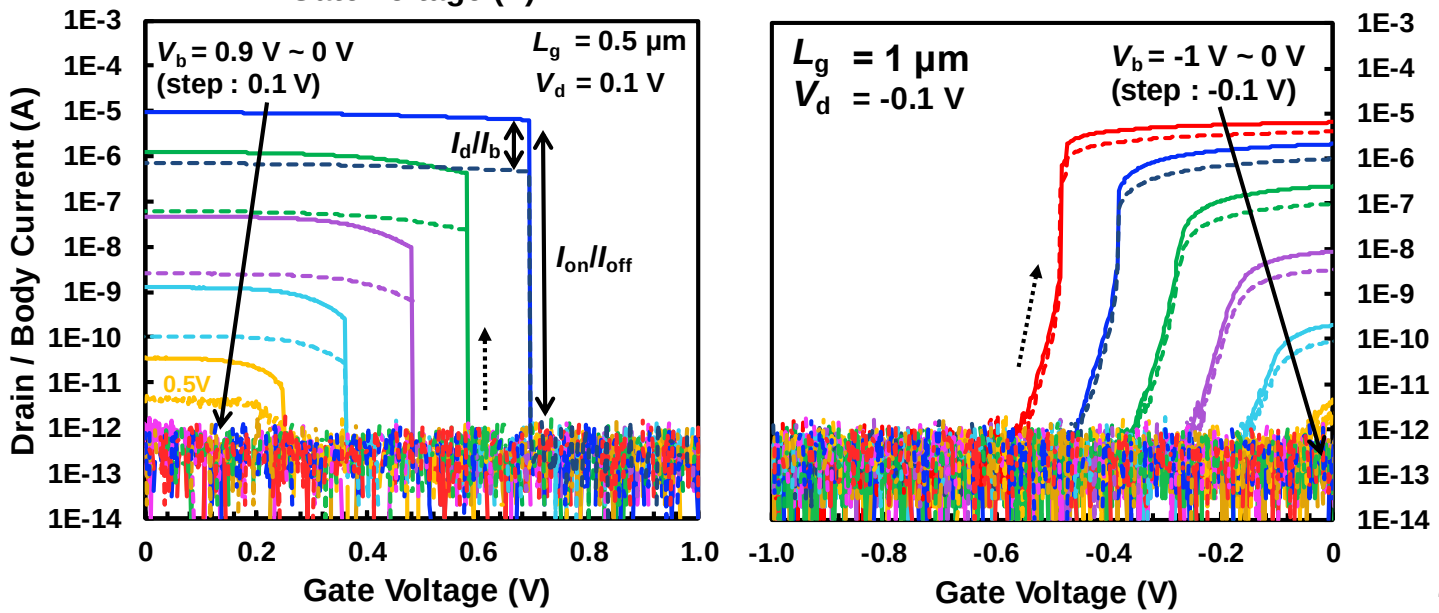


p-type GCCI SOI-Tr

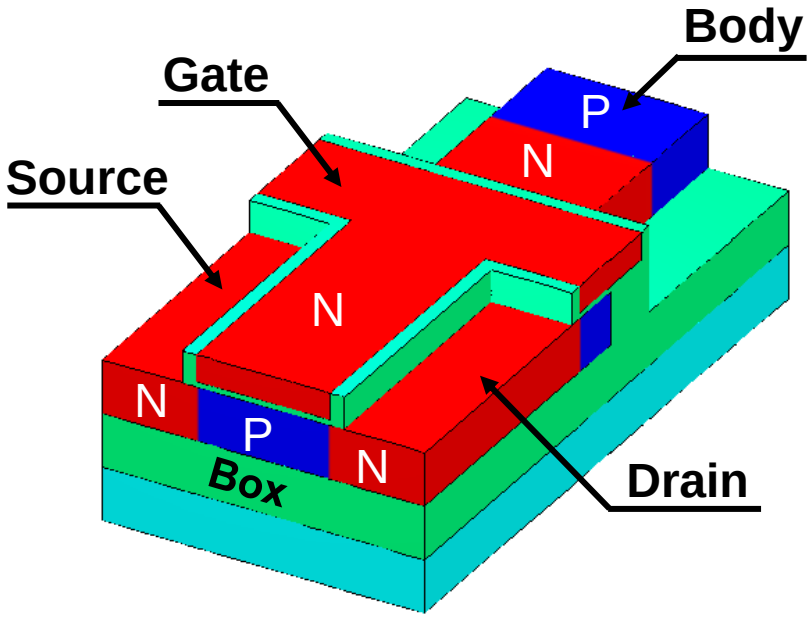


n-type GCCI SOI-Tr

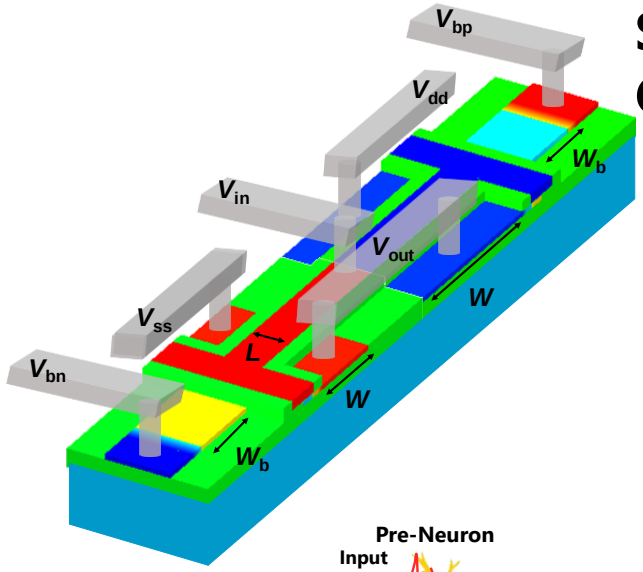




PNBT SOI-FETを用いた極低消費電力アプリケーション例

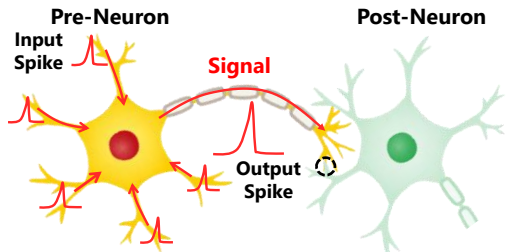


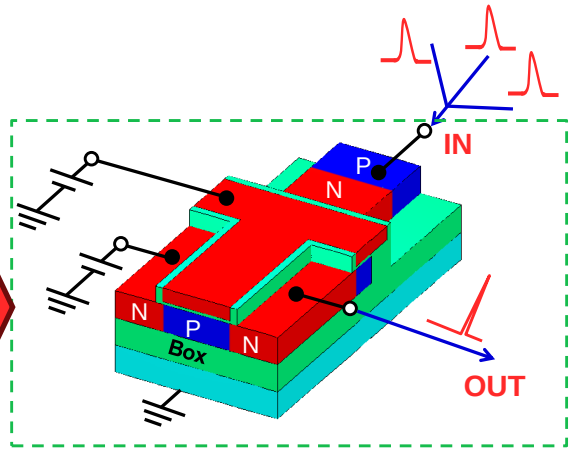
PNBT SOI-FET



Steep switching CMOS inverter

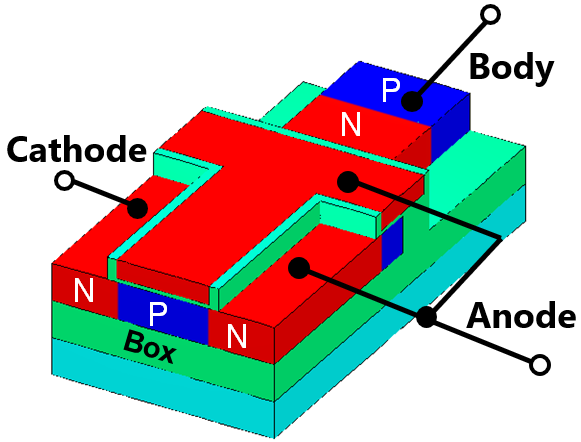
S. Ishiguro, *et al.*, *VLSI-TSA*, 2021.





Neuromorphic device

T. Sasaki, *et al.*, *EDTM*, 2022.



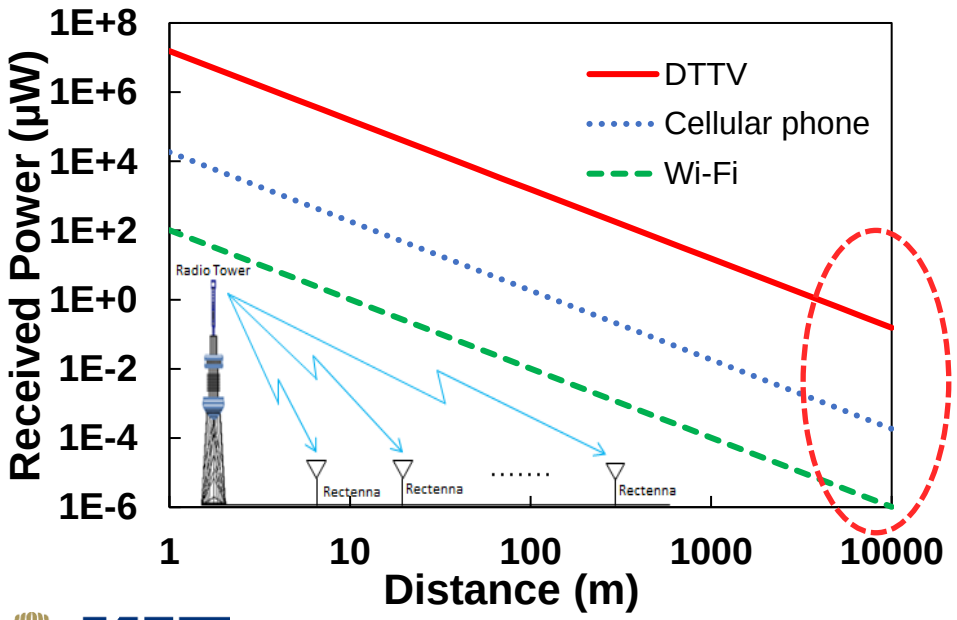
Steep switching diode for RF energy harvesting

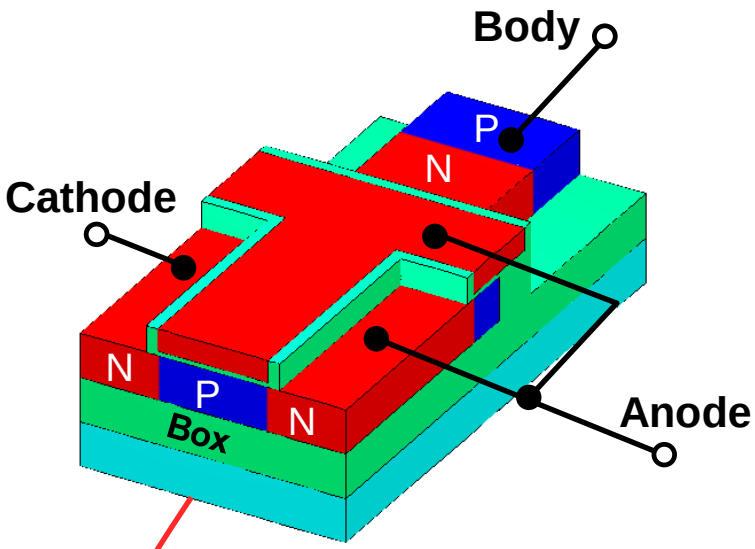
T. Mori, *et al.*, *IEEE J-EDS*, 2018.

環境発電用整流デバイスの研究

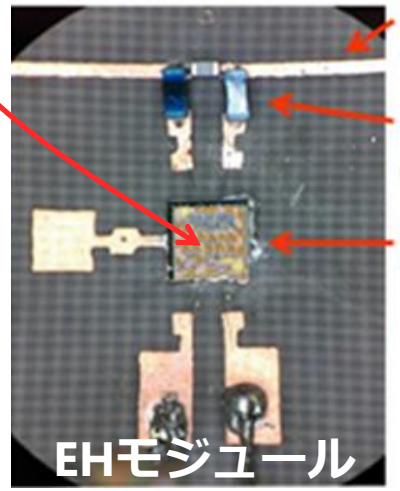
環境発電 (Energy Harvesting : EH)
環境中にある熱や振動などの
エネルギーを集めて発電する

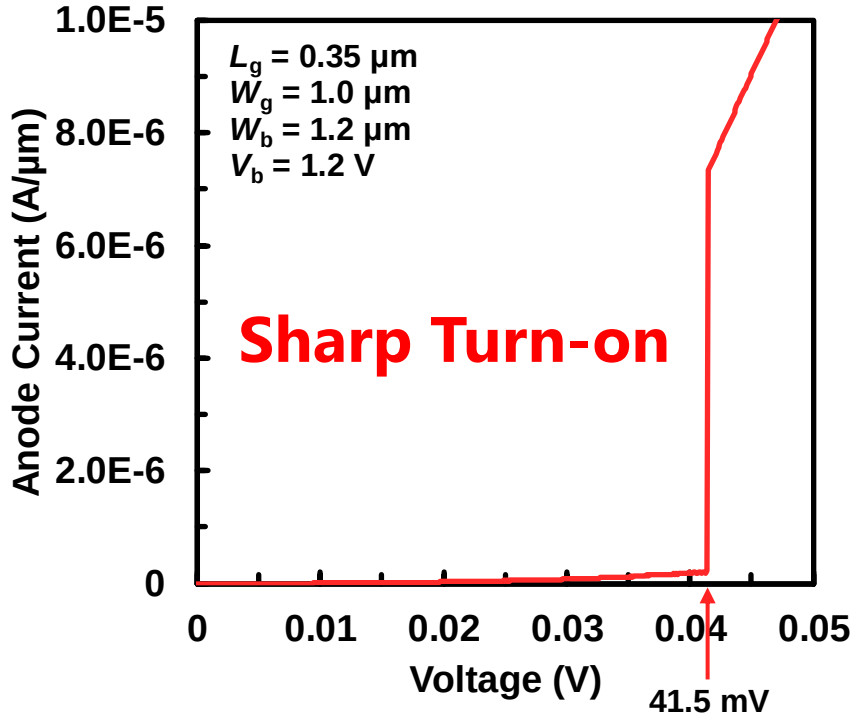
環境中に飛んでいる電波に着目！
しかし・・・
→微小な電波を整流する素子が必要





PNBT Diode

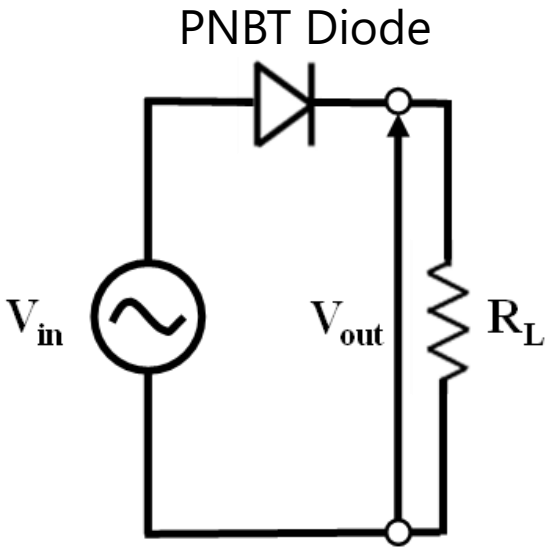


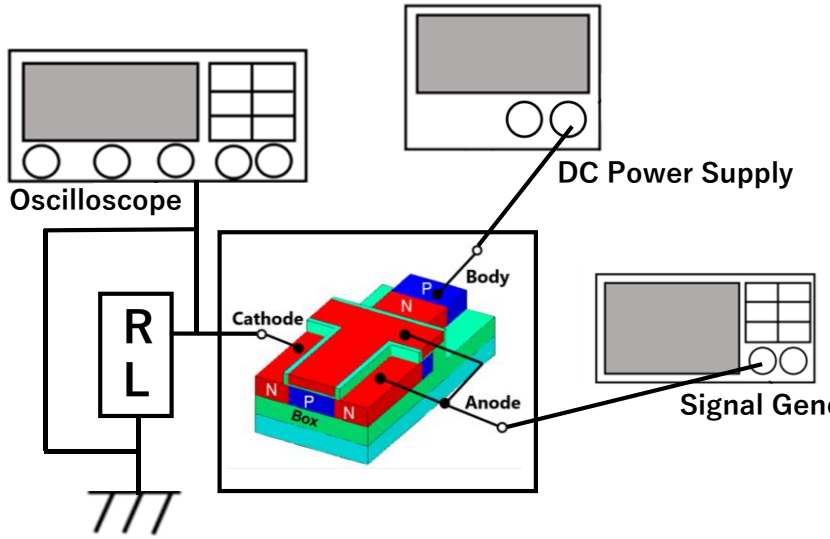


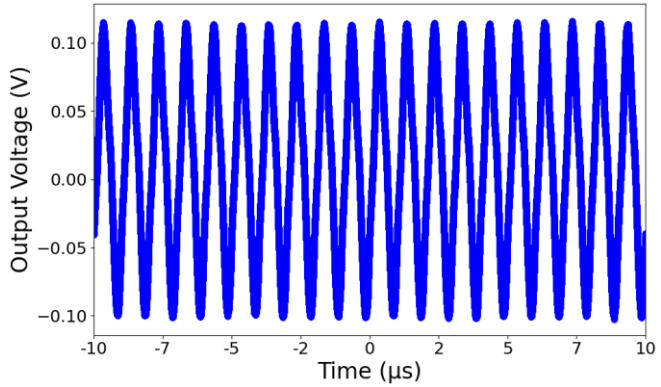
PNBT Diodeを使用した整流回路によって微小な電波からの発電を目指す

PNBT Diodeを用いた半波整流実験

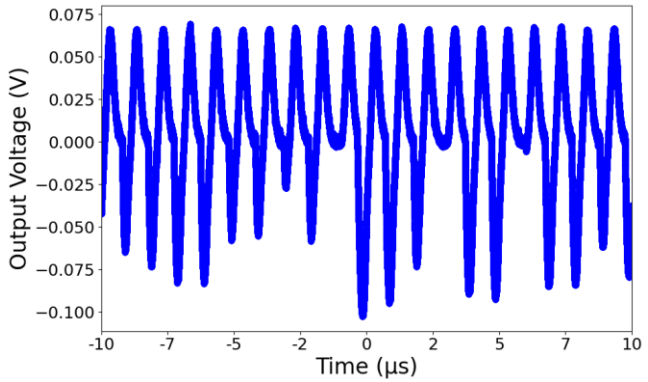
H. Matsushita *et al.*, TJMW 2024.



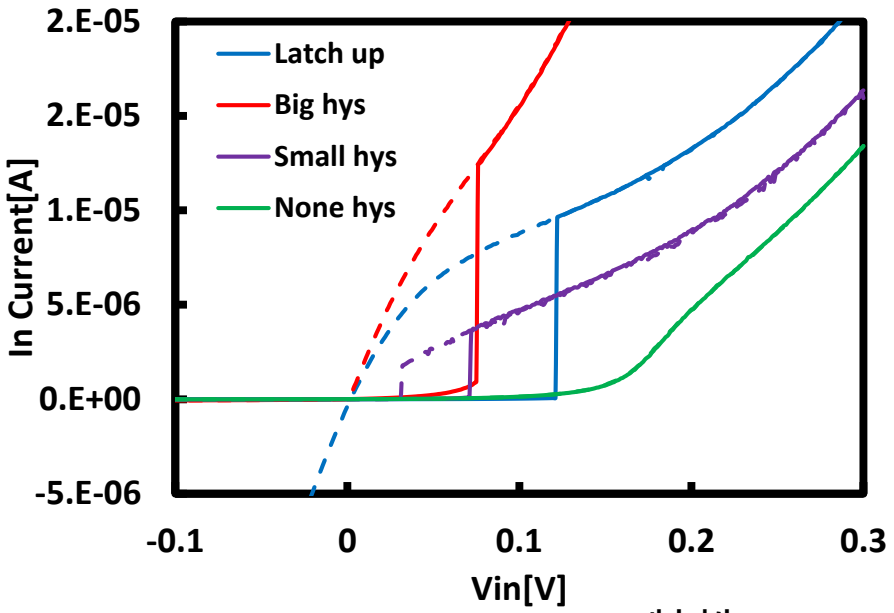




Latch upデバイス使用時の出力電圧



Small Hys. デバイス使用時の出力電圧



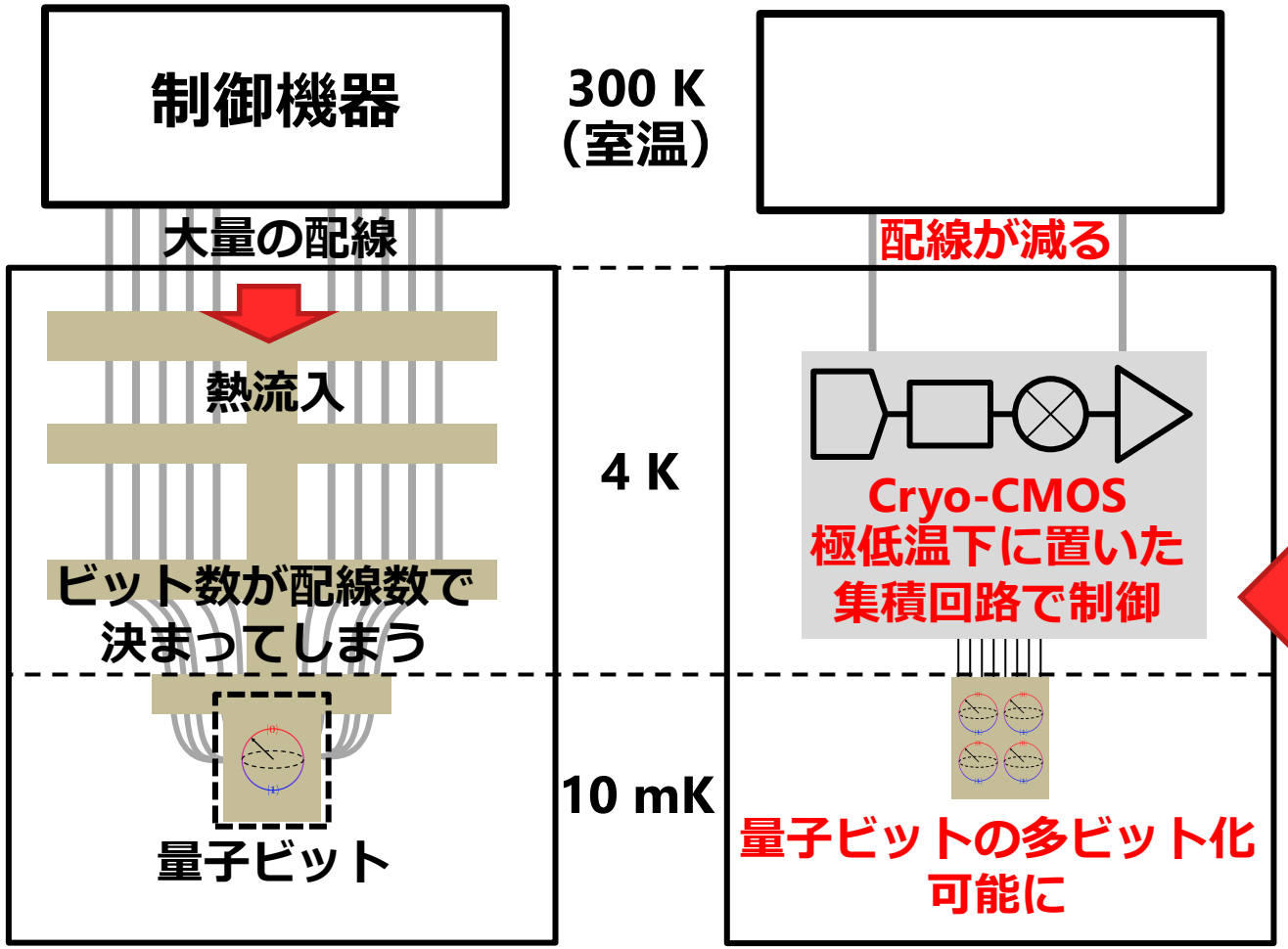
PNBT DiodeのI-V特性

Gate下やBase部にキャリアが残っていることで逆方向バイアス時も（過渡的には）完全なOFF状態にならない？
→Arイオン注入で制御できないか？

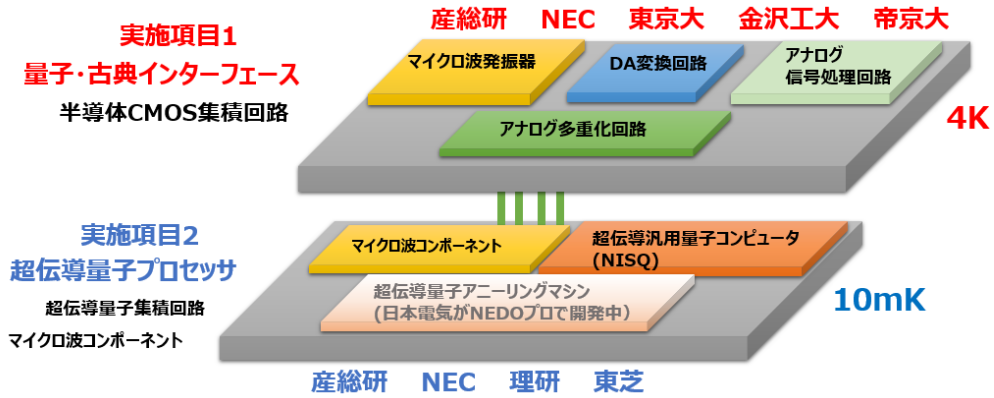
Cryo-CMOS

極低温CMOS回路用デバイスの研究

現在の計算機の性能を凌駕すると期待される
<量子コンピュータ>



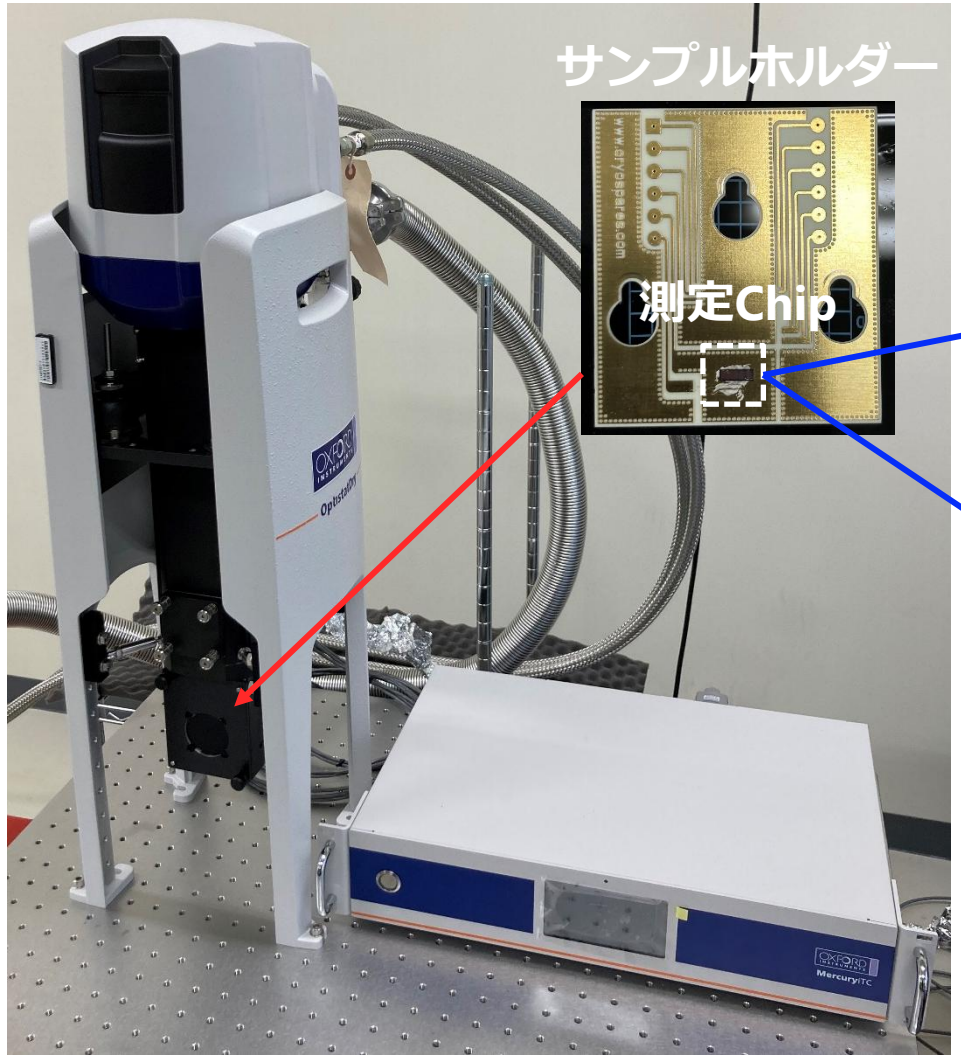
NEDO 委託で実施



極低温下で低消費電力な
デバイスが必要

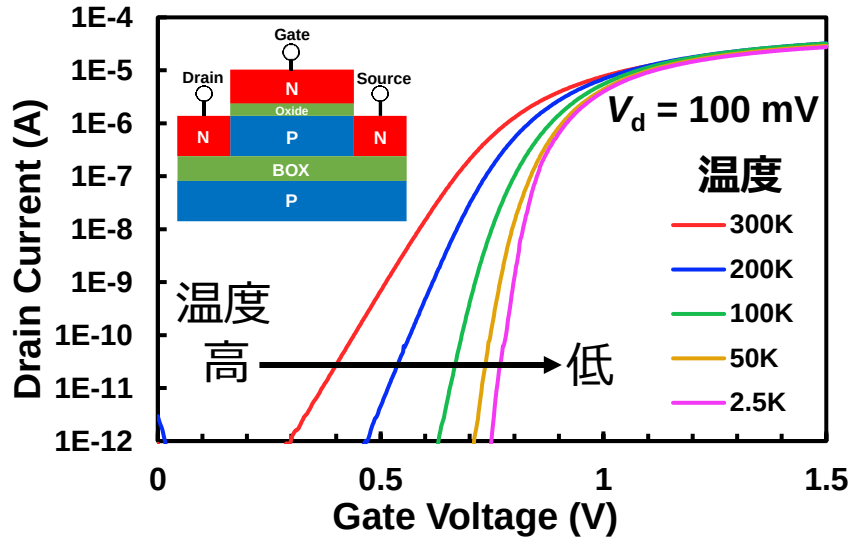
KIT

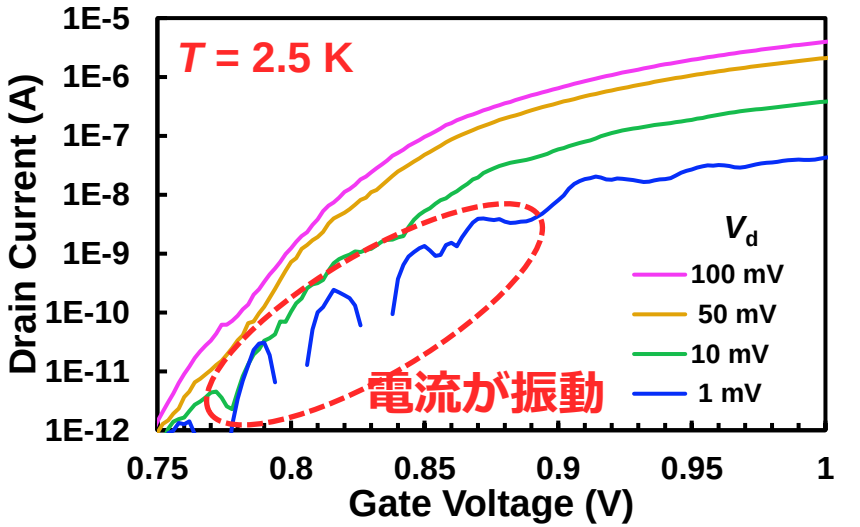
極低温CMOS回路用デバイスの研究



クライオスタット (産総研からの貸与)

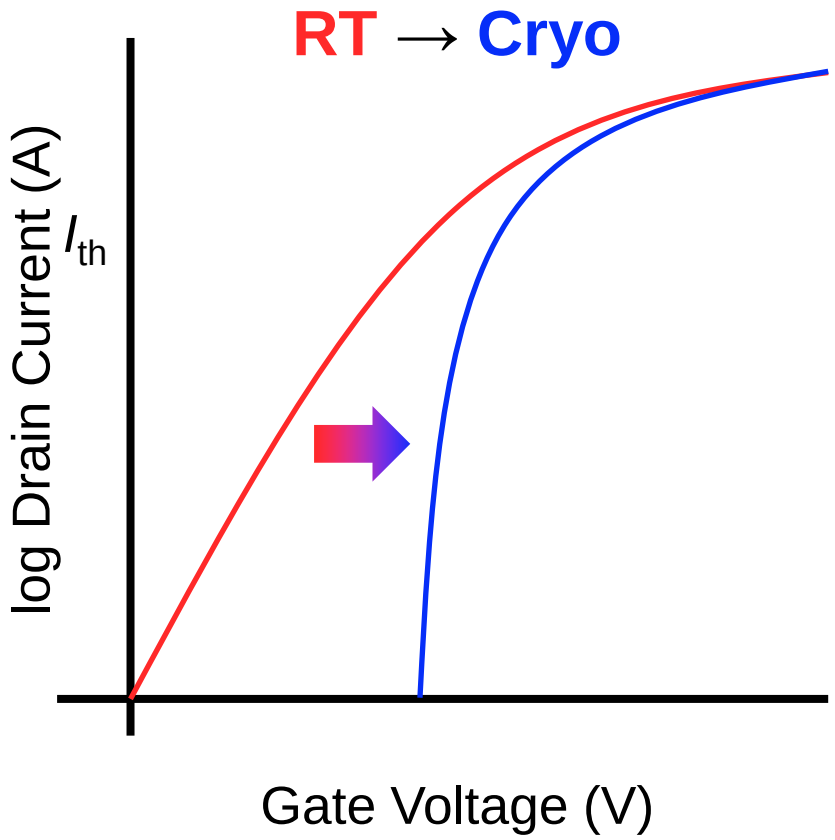
~2 Kの極低温下で測定が可能

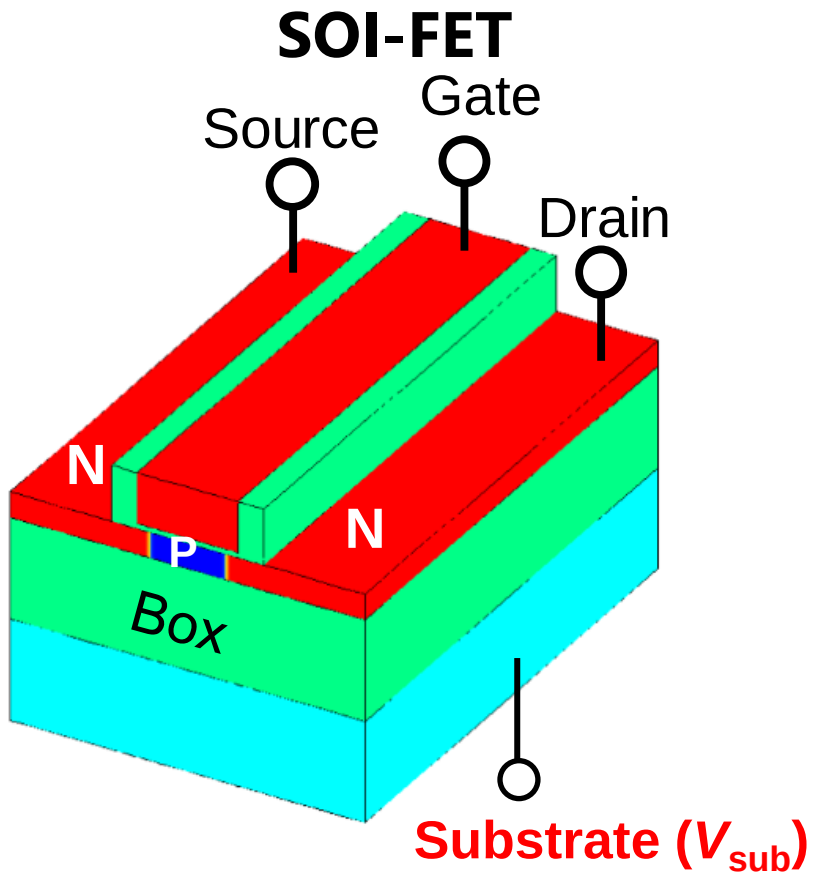




極低温下MOSFETの動作メカニズム解明が必要

SOI-FETへの期待 | 極低温下におけるしきい値の制御

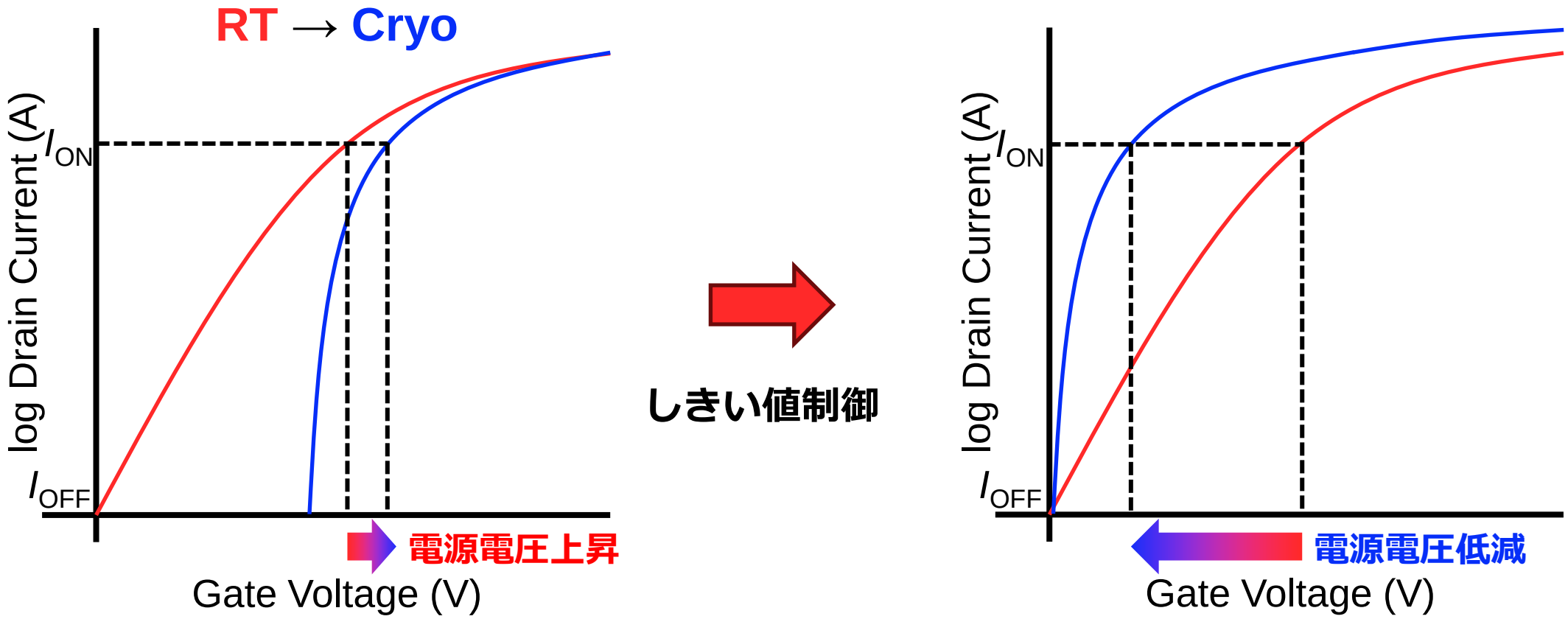




極低温環境下では電気的特性が変動

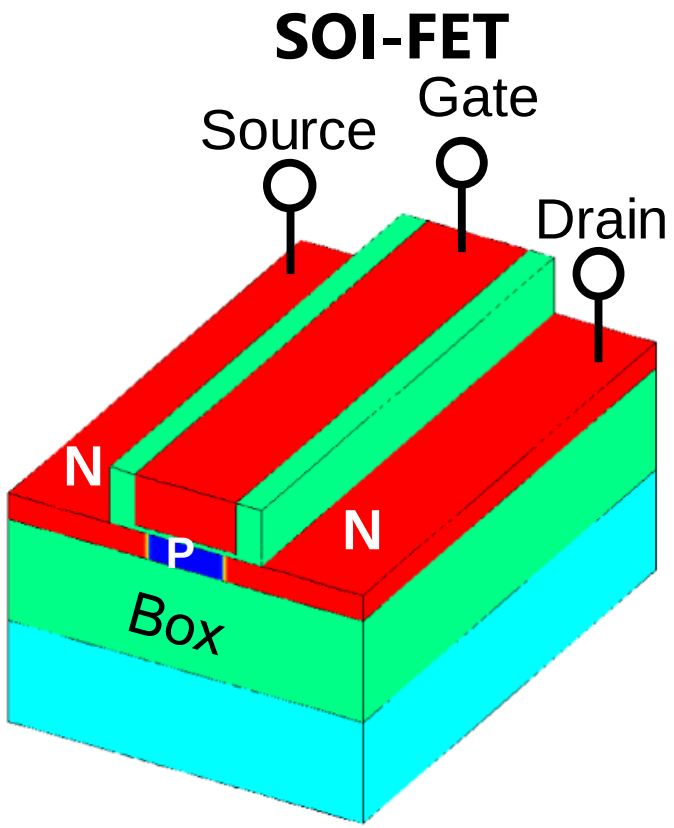
SOI-FETの基板バイアスによって制御

SOI-FETへの期待 | 極低温下におけるしきい値の制御



基板バイアスによりしきい値を制御することで電源電圧を低減し低消費電力化する

SOI-FETの懸念点



・フローティングボディ効果の影響
基板が浮いている（フローティングボディ）ためキャリアの蓄積やそれに付随した履歴効果が起こる

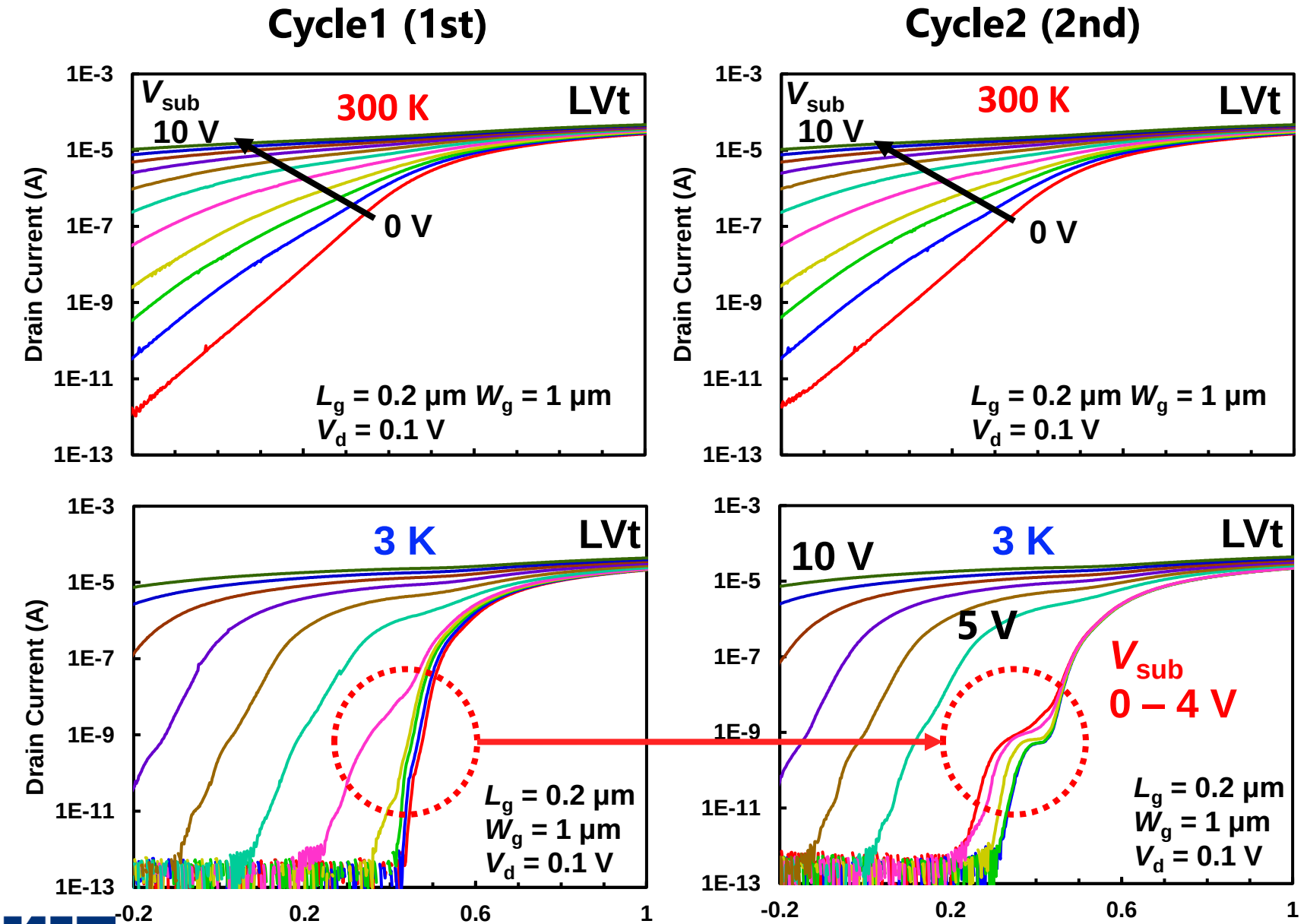
・Si/Box側界面の影響
Bulk MOSFETに対して埋め込み酸化膜(Box)側にも界面ができる

・熱の影響
SOI-FETでは放熱がBoxによって妨げられるため
自己加熱効果 (Self-Heating) の影響が大きくなる

上記の影響が極低温下ではどうなる？

正の基板バイアス依存性（履歴効果）

R. Ri *et al.*, *EuroSOI-ULIS*, pp. 1–2, May 2024.



〈 300 K 〉

V_{sub} 0 – 10 V
2cycles

Same results

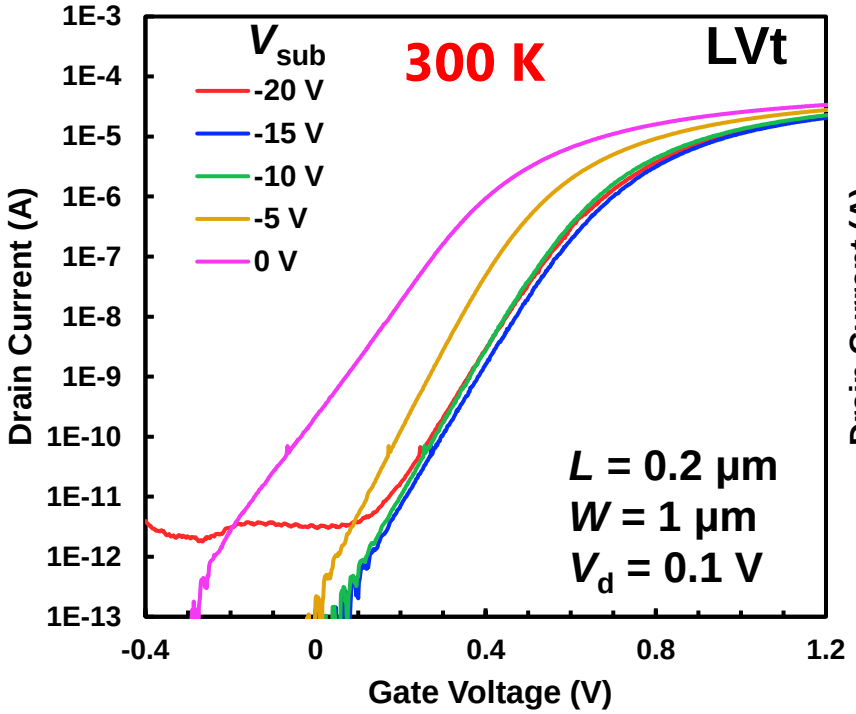
〈 3 K 〉

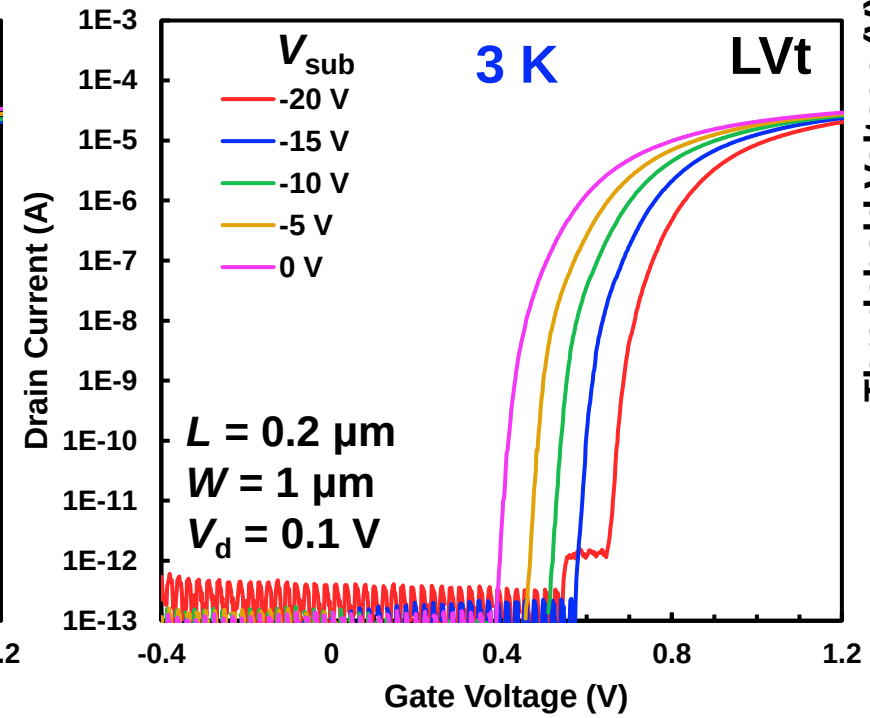
V_{sub} 0 – 10 V
2cycles

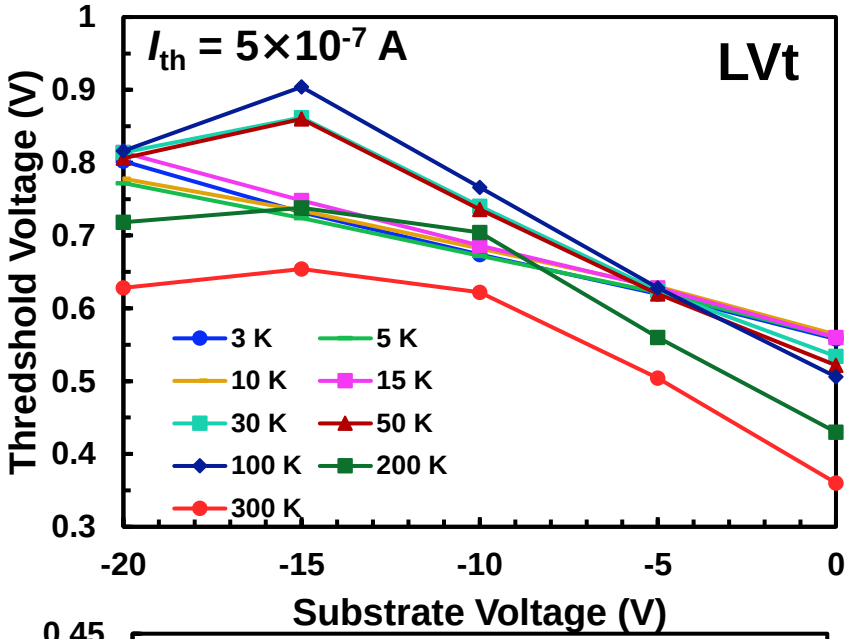
Shift
(at 2nd)

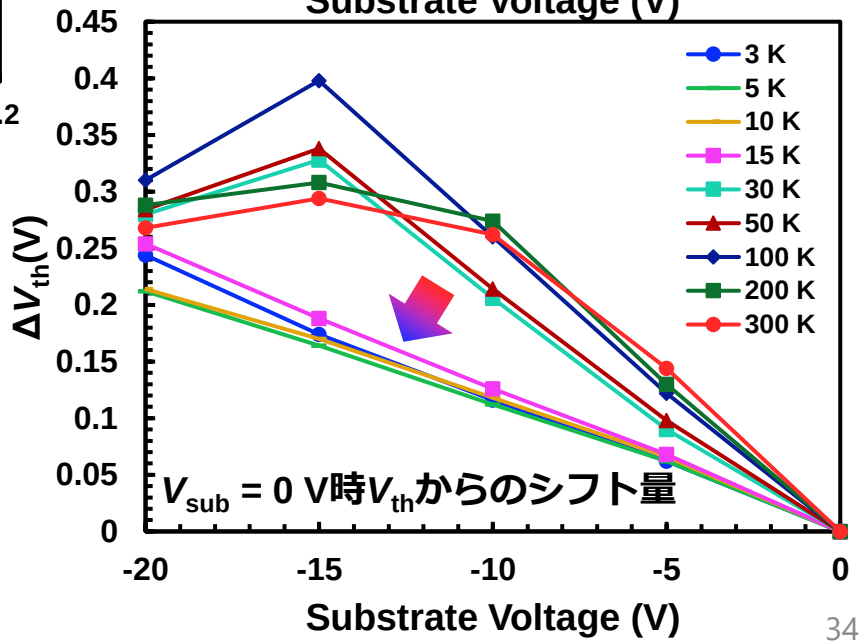
極低温下でのみ働くトラップが影響？

負の基板バイアス依存性





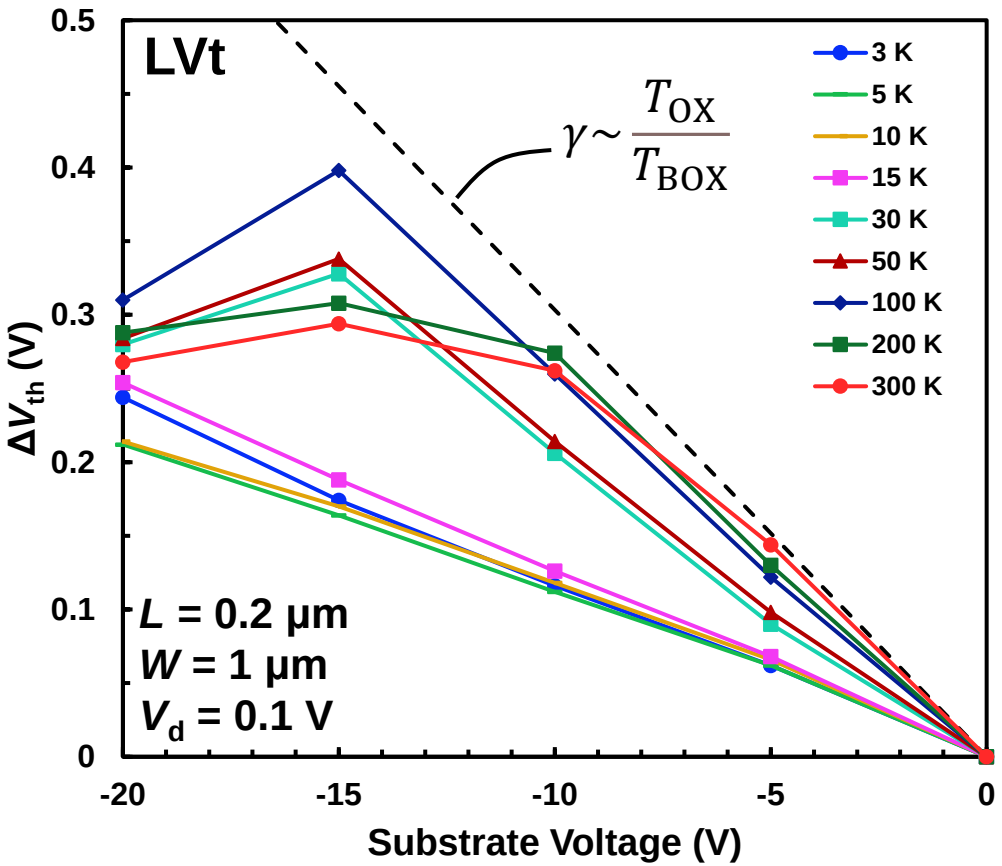


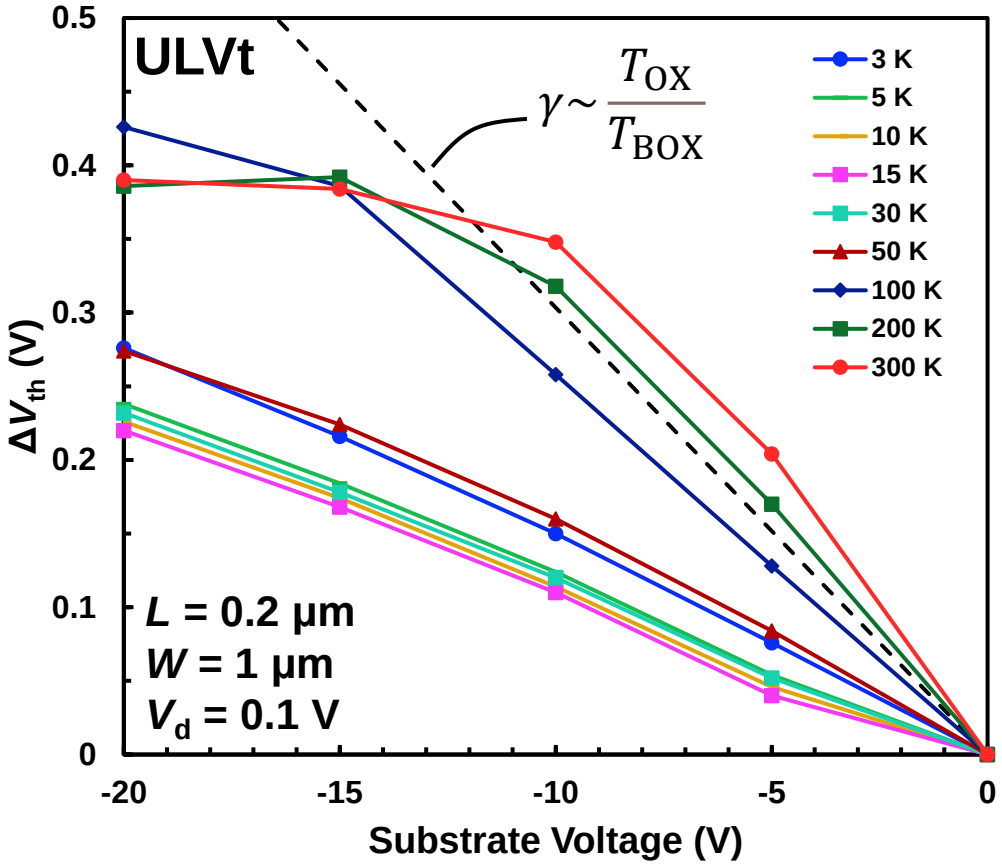


300 Kでは最初に大きく特性動き、V_{sub} = −10 Vで飽和
3 Kはほぼ一定間隔で特性シフト

しきい値シフト量は温度が下がると（15 K以下で）ほぼ一定に

チャネル不純物濃度依存性

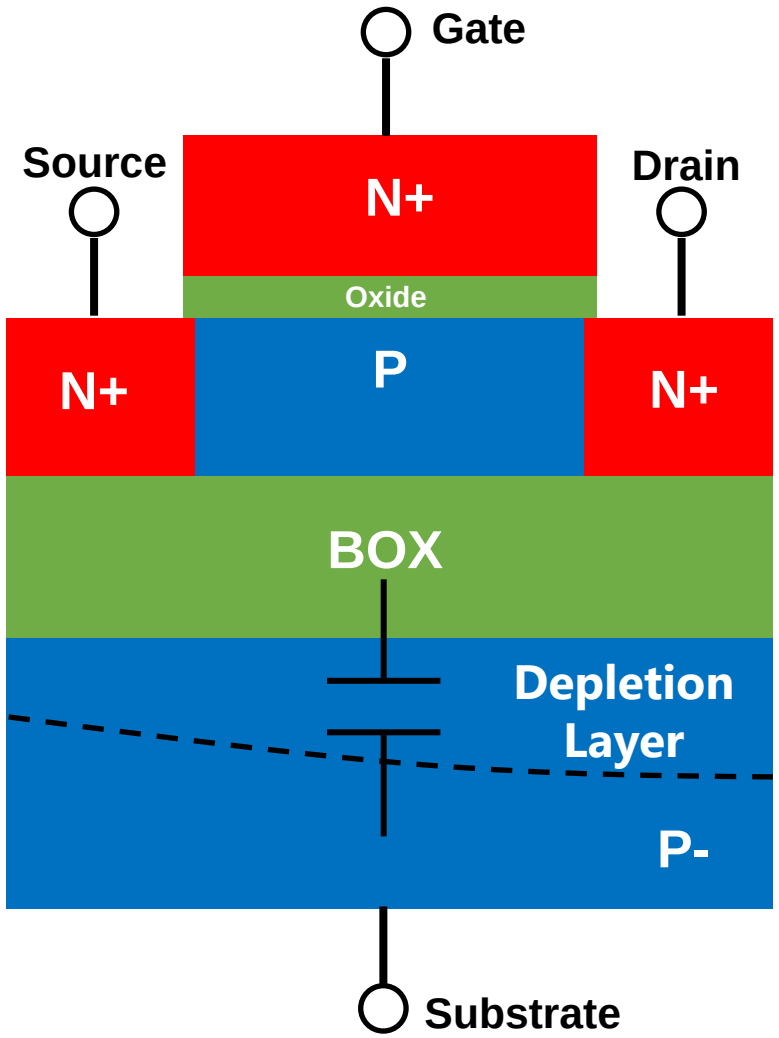




チャネル不純物濃度：LVt > ULVt

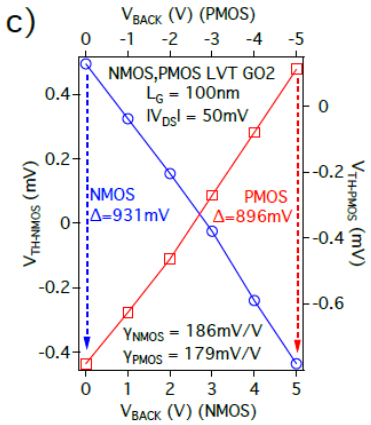
FD-SOIの理想的なボディ効果係数γと比較すると半分程度の傾き（シフト量）になっている
ULVt（LVtより完全空乏化しやすいはず）でも低温になると傾き悪くなりほぼ一定に

ボディ効果係数変動の想定原因



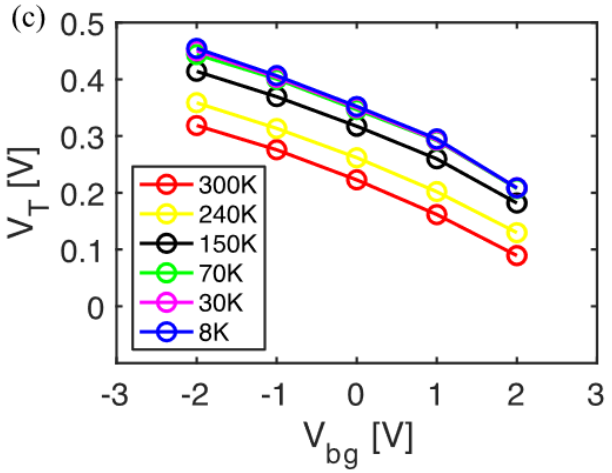
<想定要因>
フリーズアウト？によって
Box下の空乏層容量が変動→ボディ効果係数γが変動？

先行研究では温度によるγへの影響はほとんど無い
→プロセス依存？



"The measured GO2 body-factors at 4.3 K are close to the room temperature values: 183 and 178 mV/V for NMOS and PMOS, respectively."

H. Bohuslavskyi, Doctoral thesis, p. 77, Université Grenoble Alpes, 2019.



F. A. Mamun, *et al.*, *IEEE T-ED*, vol. 69, no. 10, pp. 5417-5423, Oct. 2022.

<先行研究との違い>
・Si膜厚、Box膜厚（先行研究はより薄い）
・裏面不純物ドープ（しきい値制御用のドープ有？）

まとめ

PN-Body Tied SOI-FETとCryo-CMOSの研究進捗について紹介

<PNBT SOI-FET>
・Arイオン注入によるヒステリシス制御
→DG PNBT SOI-FETにおいて、ヒステリシスを抑えつつsteep SSを実現
・PNBT Diodeの整流特性
→逆方向バイアス時にも過渡的に電流が流れてしまう現象について解析

<Cryo-CMOS>
・極低温下における基板バイアス時の挙動
→正バイアス時は履歴効果、負バイアス時は基板バイアス効果係数の変動が発生