Muon-induced Soft Errors in FinFET and Planar SRAMs

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Kakenhi Kiban(S) project (2019-2024)

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JAEA	**Shinichiro Abe**
Osaka Inst. Tech.	**Yoshinari Kamakura**

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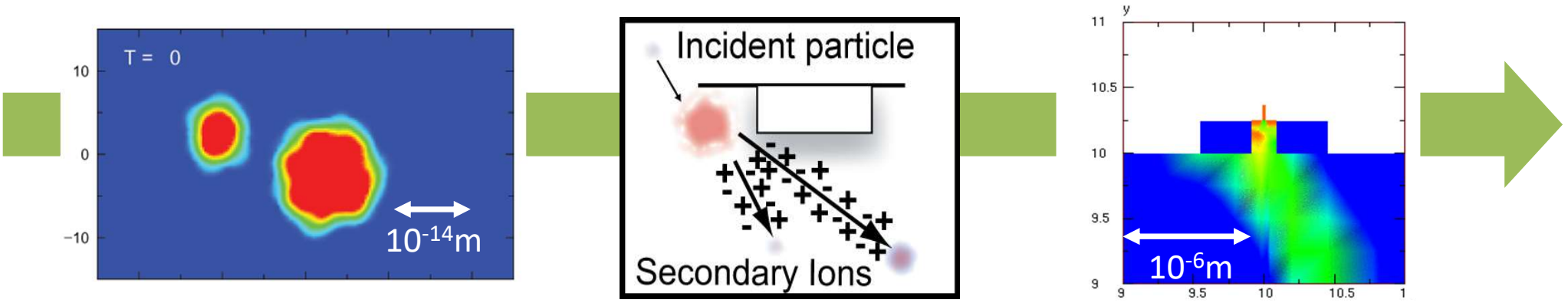
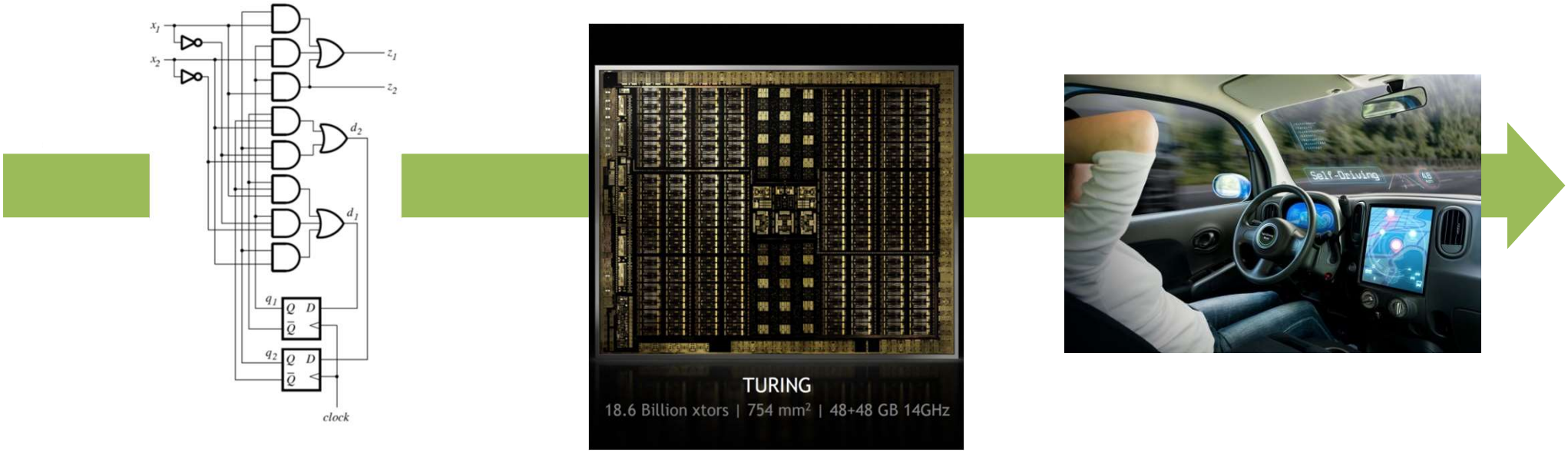
Soft error: occurrence and propagation





Muon: potential source of soft error

Muon accounts for 70% of secondary particles on earth

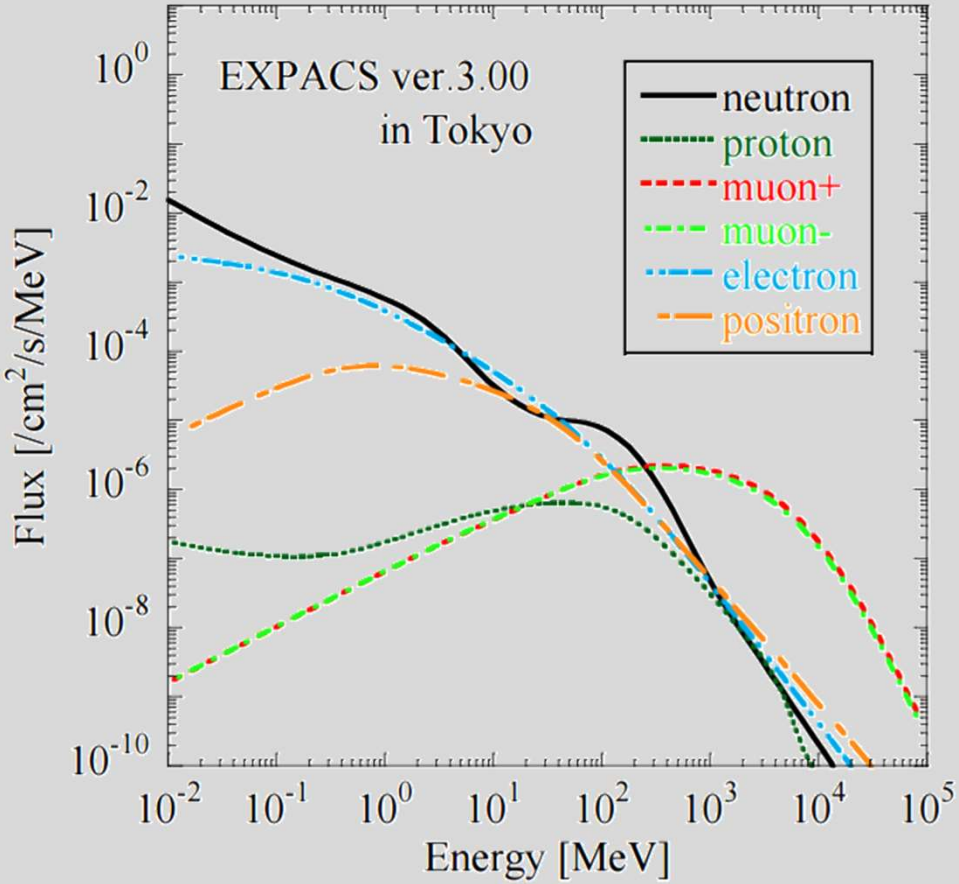
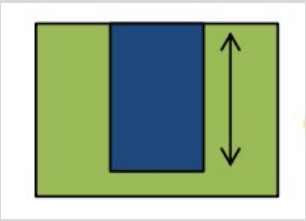


Fig. Flux spectra from EXPACS: T. Sato et al., EXPACS, *Radia. Res.*, 166, 544-555, 2006

Decrease in critical charge

Deposited charge can exceed critical charge of modern devices!

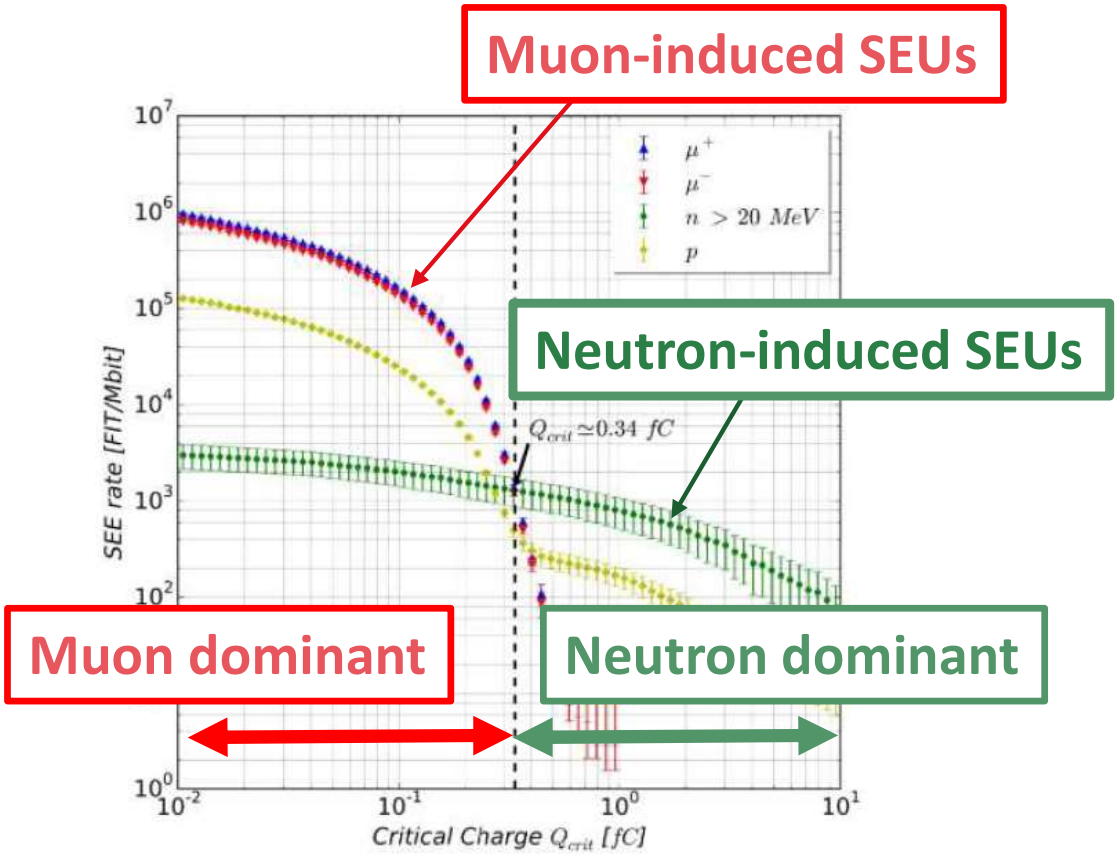


Sensitive volume depth 0.5μm

Energy	dE/dx	Deposited Charge in 0.5μm
1GeV	0.47keV/μm	0.02fC
40KeV	73keV/μm	**1.80fC**

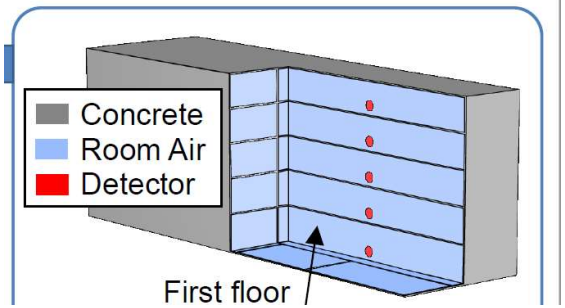
Increasing trend of muon impact

As Qc decreases, there is a possibility that muons will become dominant [2]

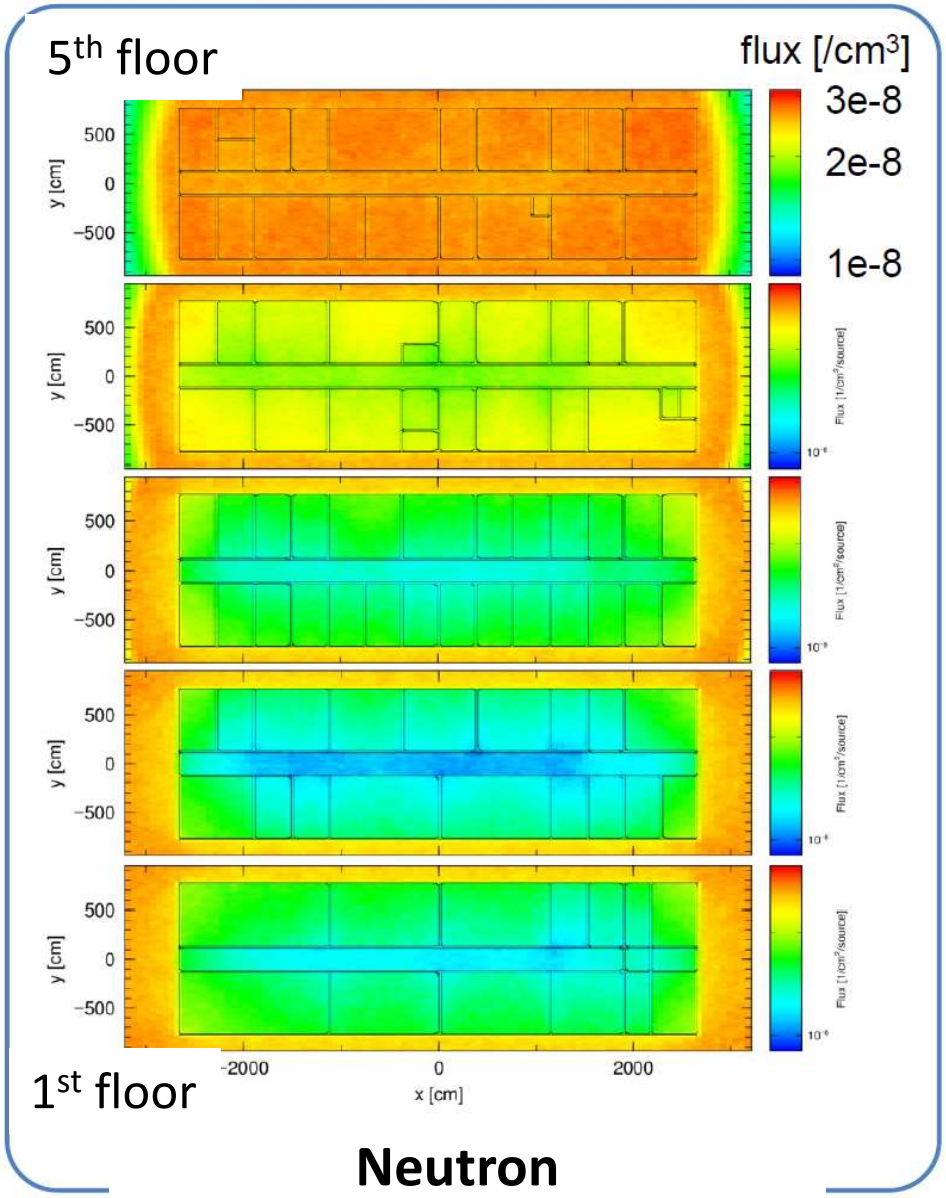


[2]: A. Infantino: TNS, 2017.

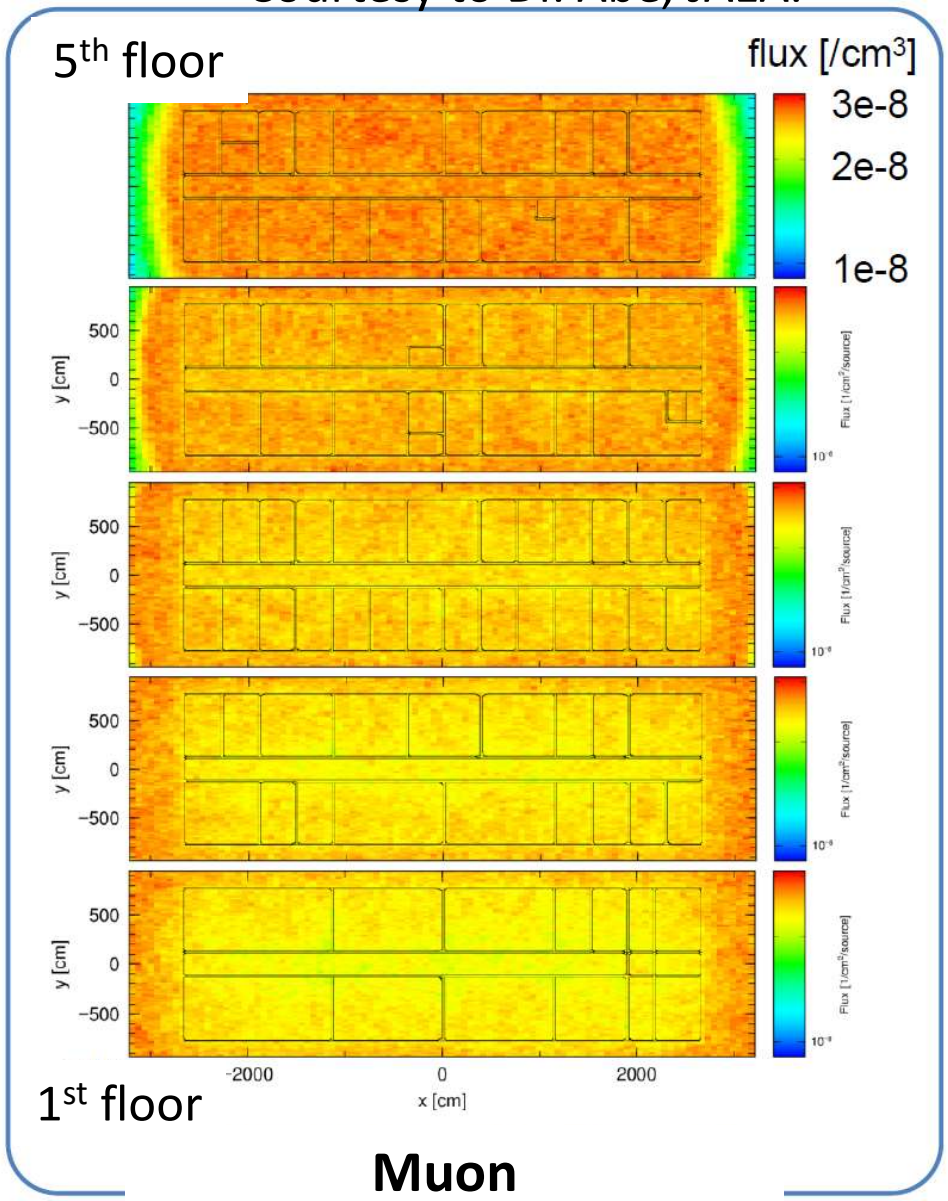
Neutron and muon in a concrete building



Courtesy to Dr. Abe, JAEA.



Neutron



Muon

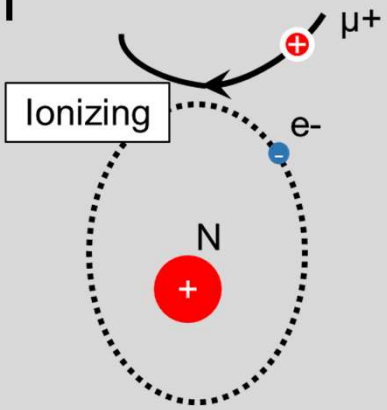
Previous works: muon-induced SEU

Positive muon:

- Experiments [1-4]
  - 14nm,22nm, etc.
- Simulation [2,4]

Charge Generation

- Ionization



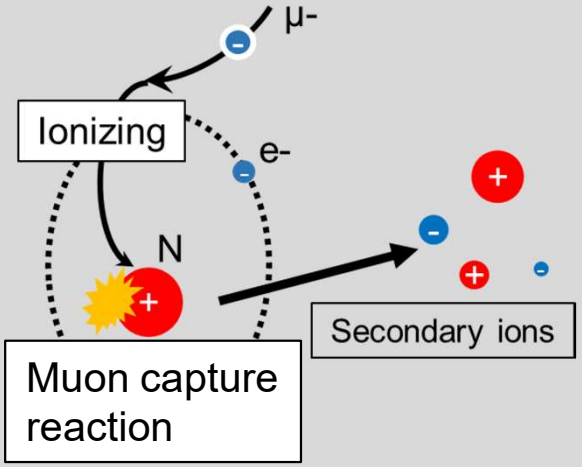
Negative muon:

- Experiments [5]
  - Only in 1980s
- Simulation [2,4]

Charge Generation

- Ionization
- Muon capture

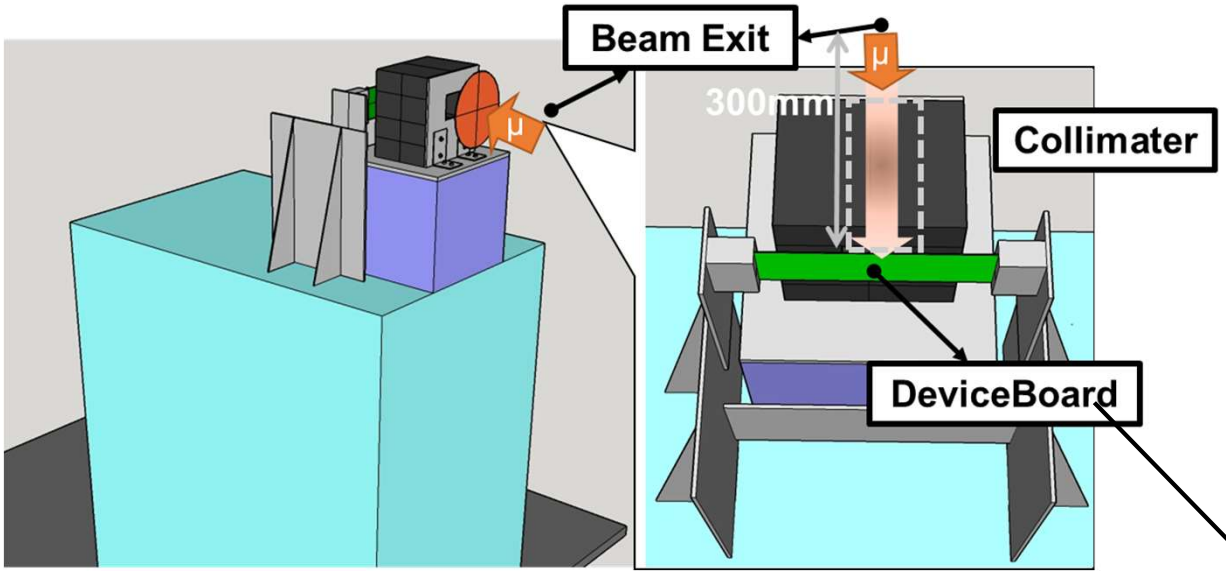
Secondary ions can deposit large charge



Impact of negative muon capture had not been studied in experiments.

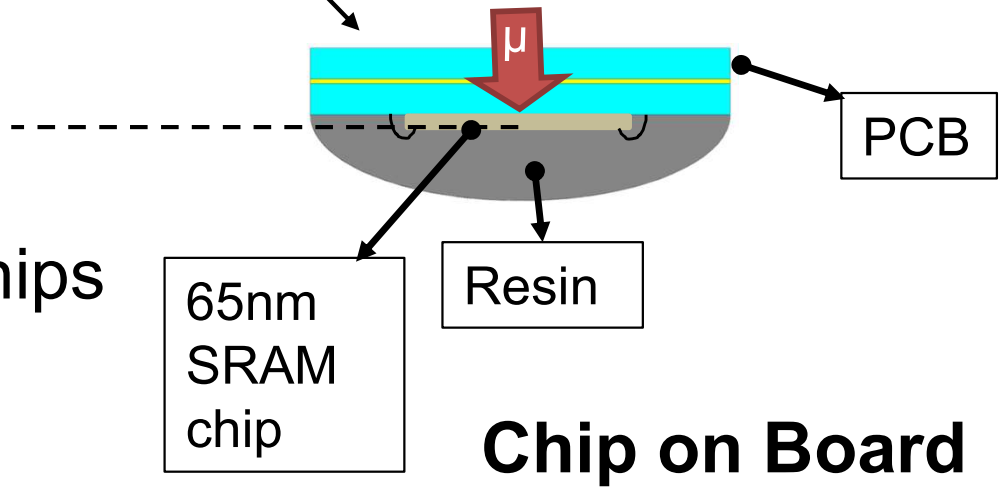
[1],[2]: Sierawski et al., *TNS*, 2010 & *IRPS*, 2014,
[3]:Seifert: *IRPS*, 2015 [4]: S.Serre, *RADECS*, 2012 [5] :J. Dicello, *Nucl. Inst. MPR*,1987

Experimental setup



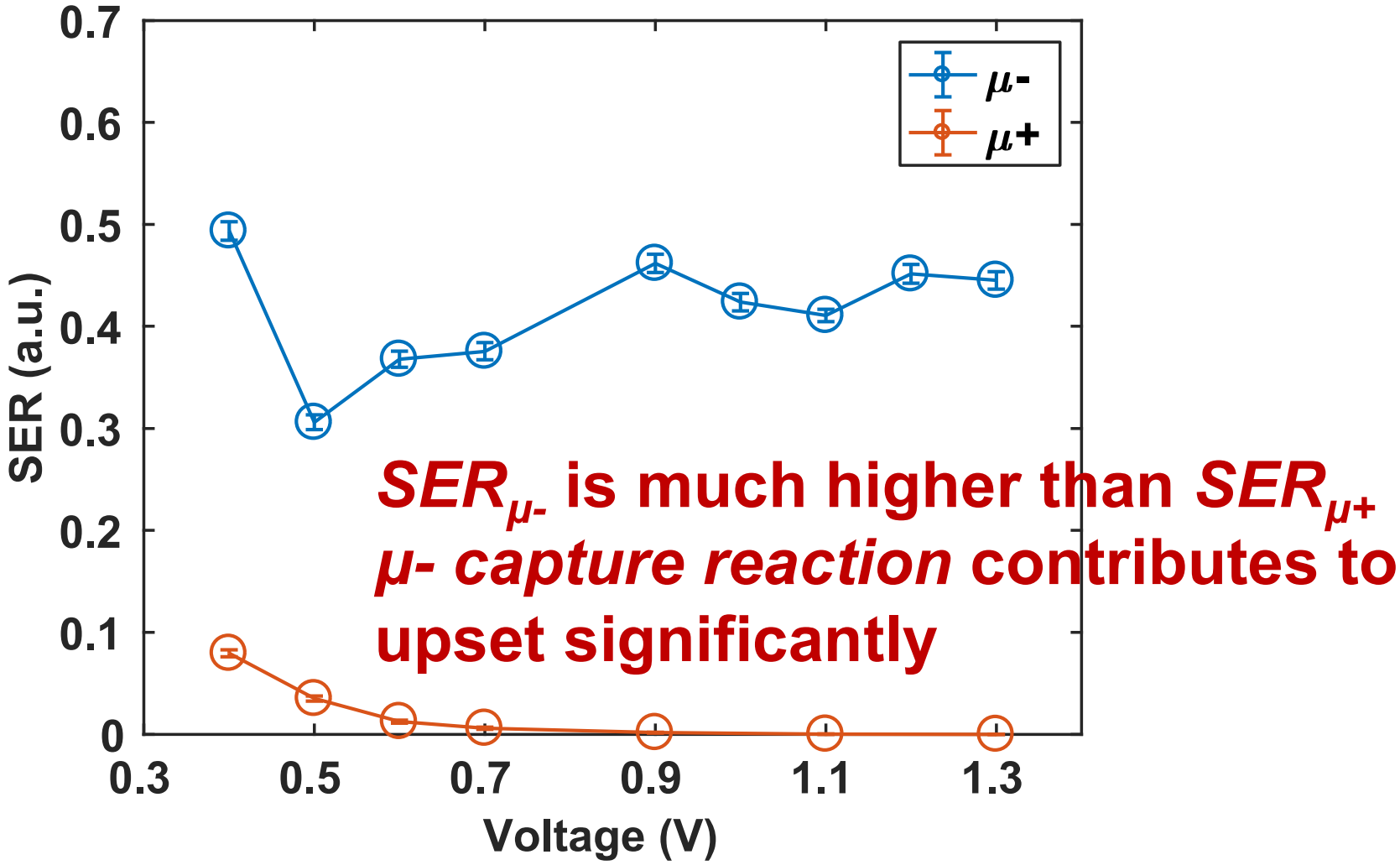
Beam facility:
MUSE
(muon science facility)
of MLF, J-PARC

Control momentum of muon
(@38MeV/c)
for making muons stop inside chips
near transistors



Chip on Board

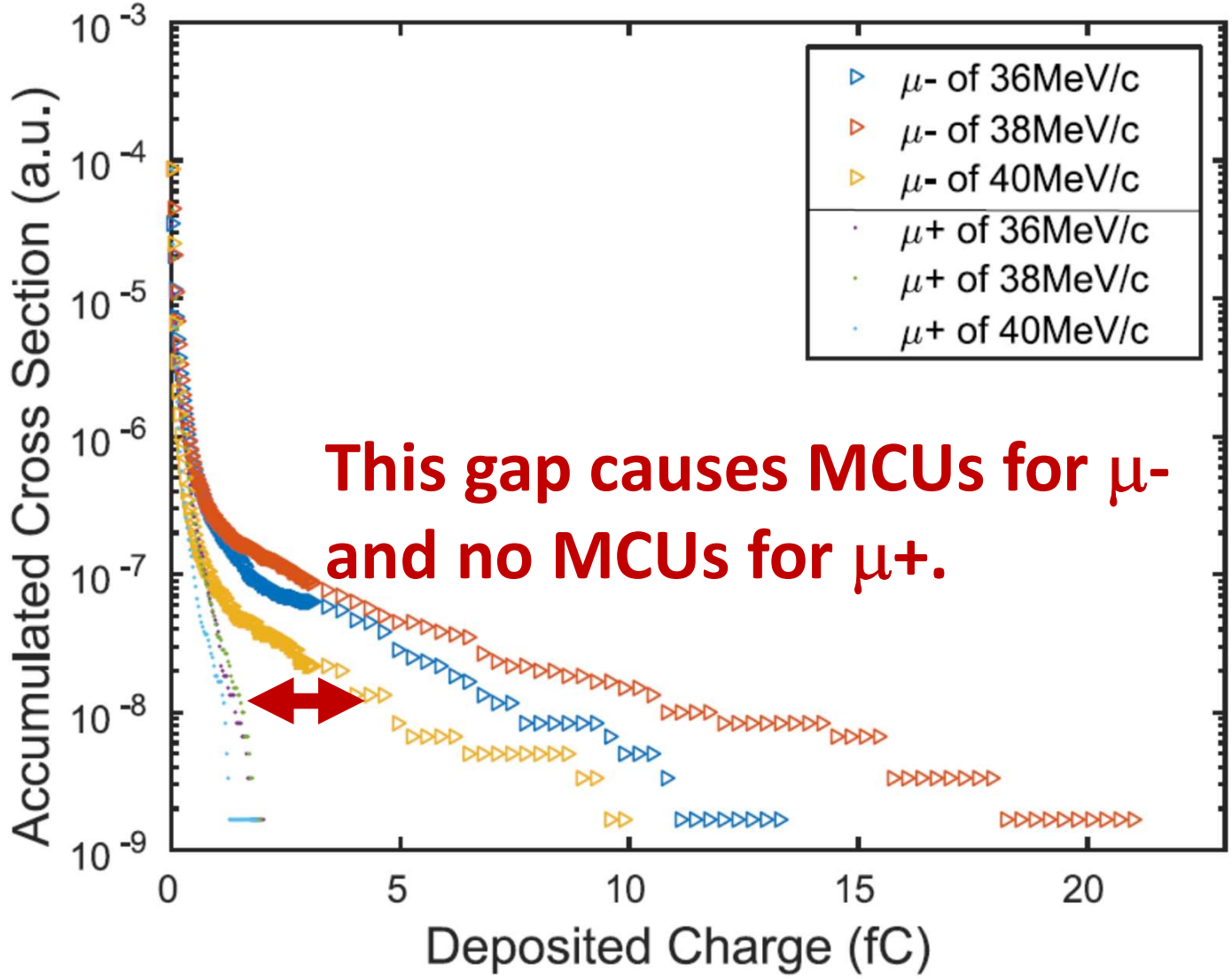
Positive vs. negative muons in bulk



W. Liao, et al., "Measurement and Mechanism Investigation of Negative and Positive Muon-Induced Upsets in 65nm Bulk SRAMs," *IEEE Trans. Nuclear Science*, August 2018.

Charge amount induced by positive and negative muons

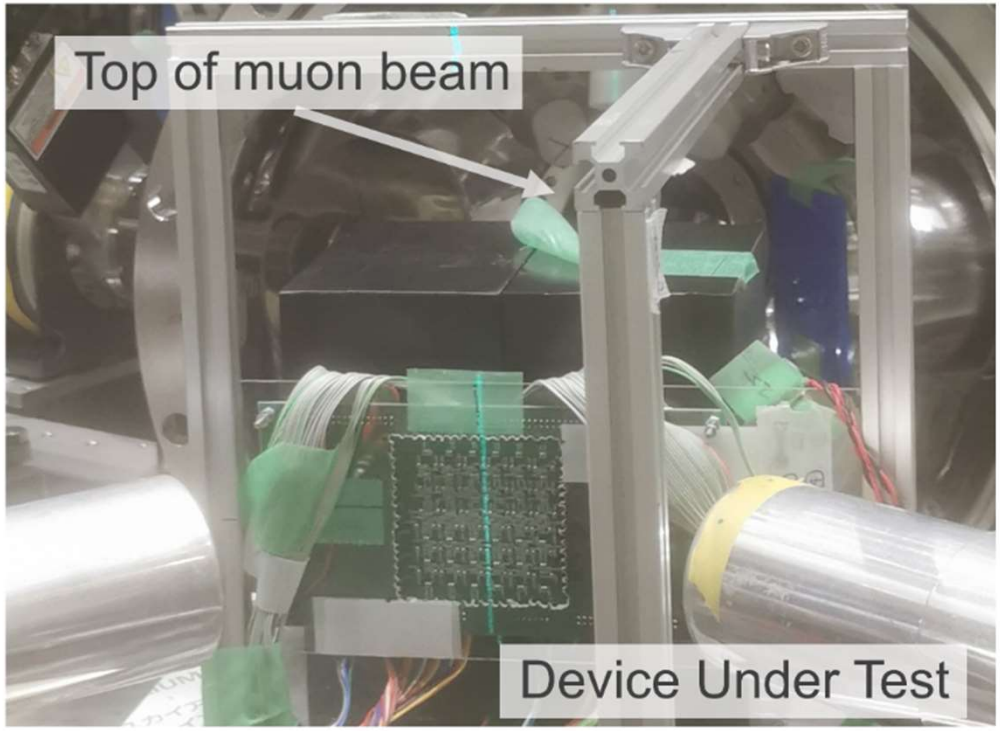
PHITS simulation



W. Liao, et al., "Measurement and Mechanism Investigation of Negative and Positive Muon-Induced Upsets in 65nm Bulk SRAMs," *IEEE Trans. Nuclear Science*, August 2018.

Recent experiment for FinFET SRAMs

[Gomi, RADECS 2023]



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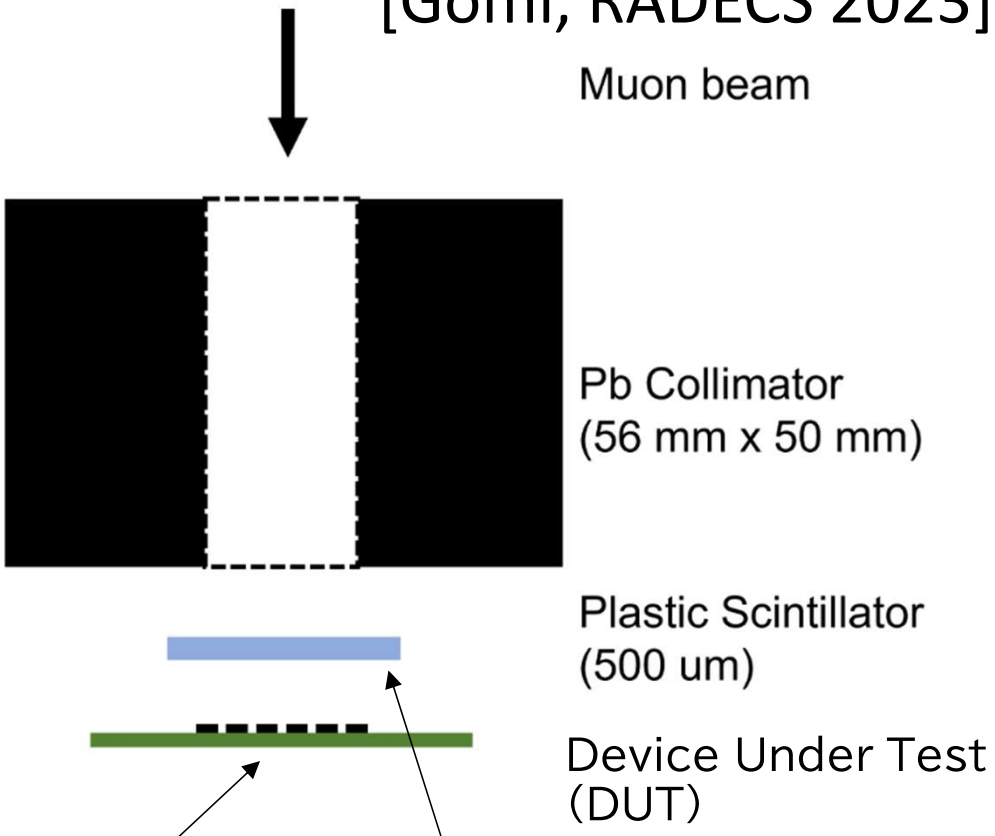
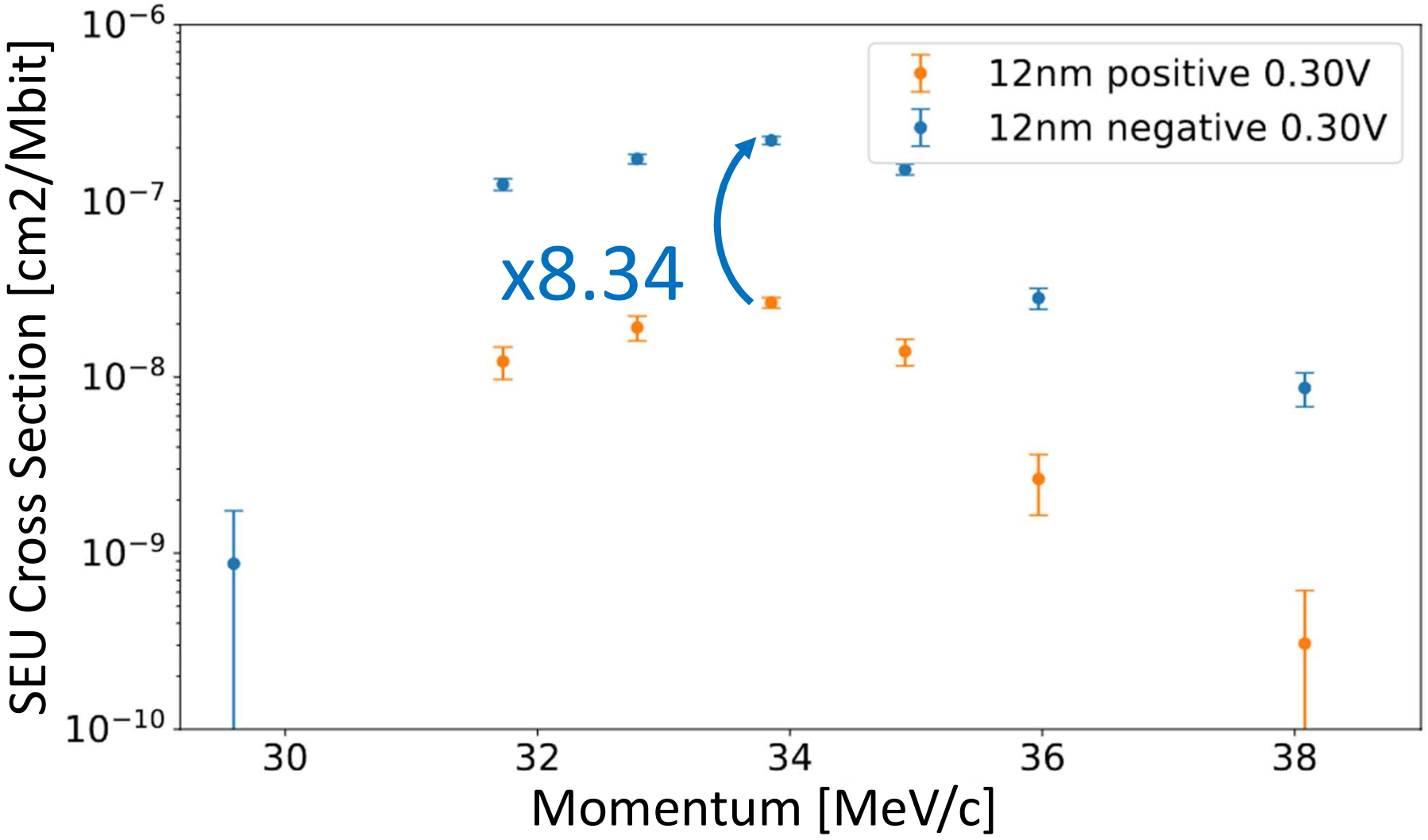


12-nm FinFETs or 28-nm SRAMs

Plastic scintillator counts # of muons

Dependence of SEU cross section on muon momentum

[Gomi, RADECS 2023]

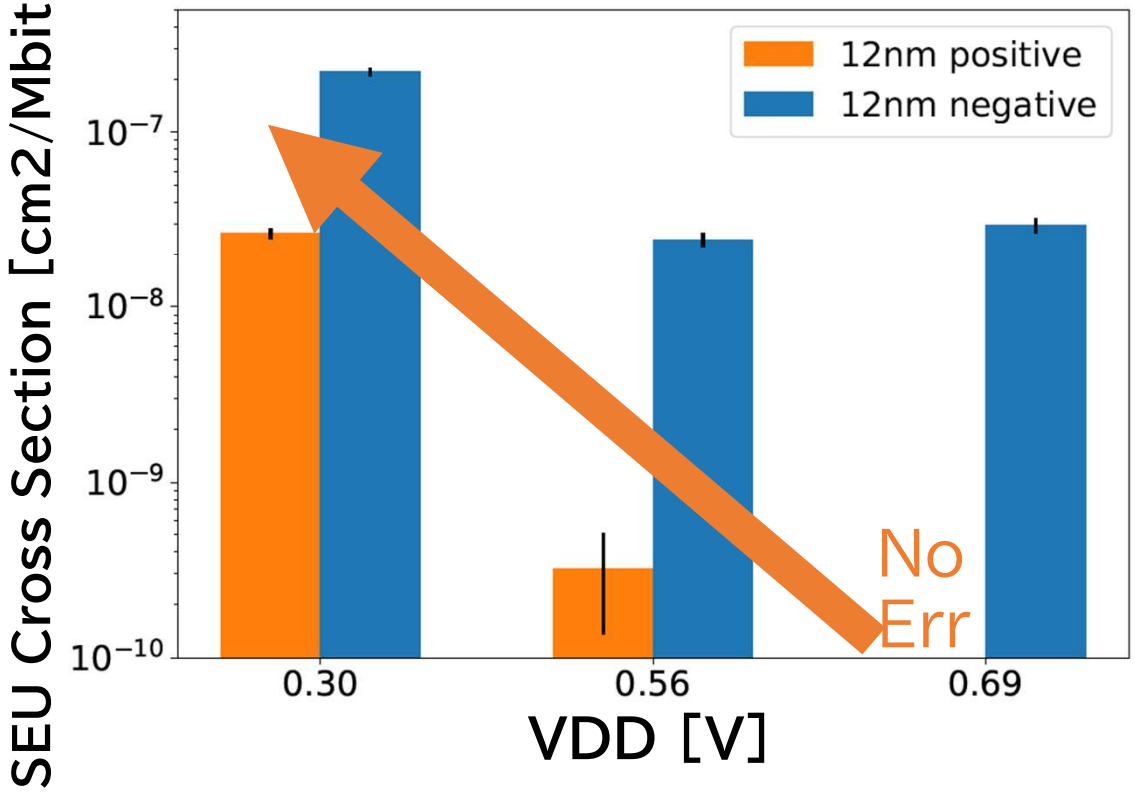


Dependence of SEU cross section on supply voltage [Gomi, RADECS 2023]

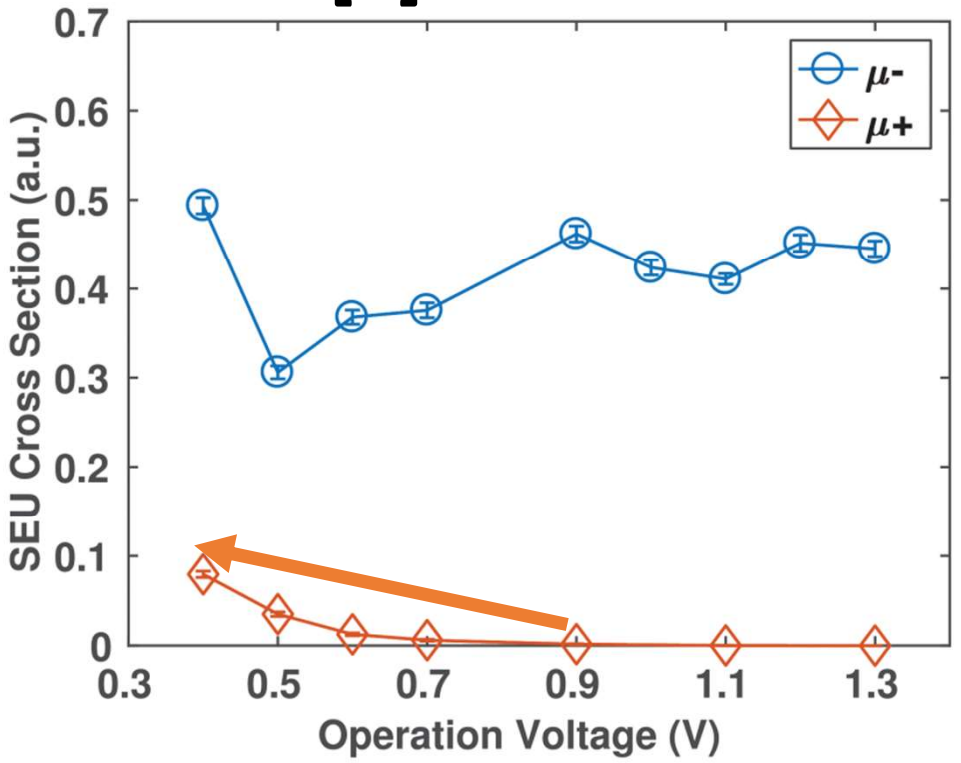
Positive muon-induced SEU cross section increases rapidly in 12nm SRAM.

- **Direct ionization might be dominant in the near future.**

12nm



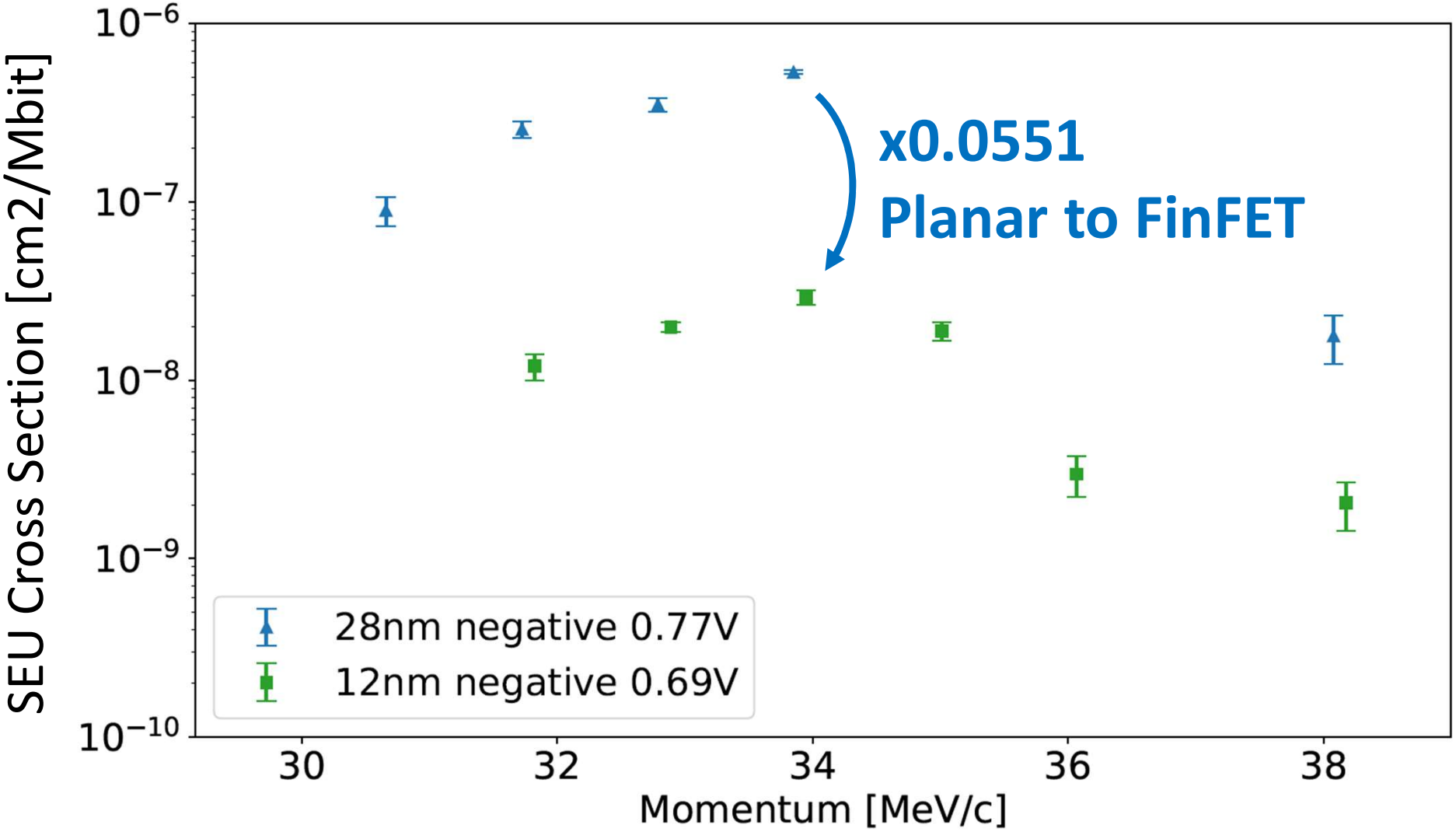
65nm[4]



[4] W. Liao et al, TNS, 2018.

Comparison b/w 12nm FinFET and 28nm planar

[Gomi, RADECS 2023]

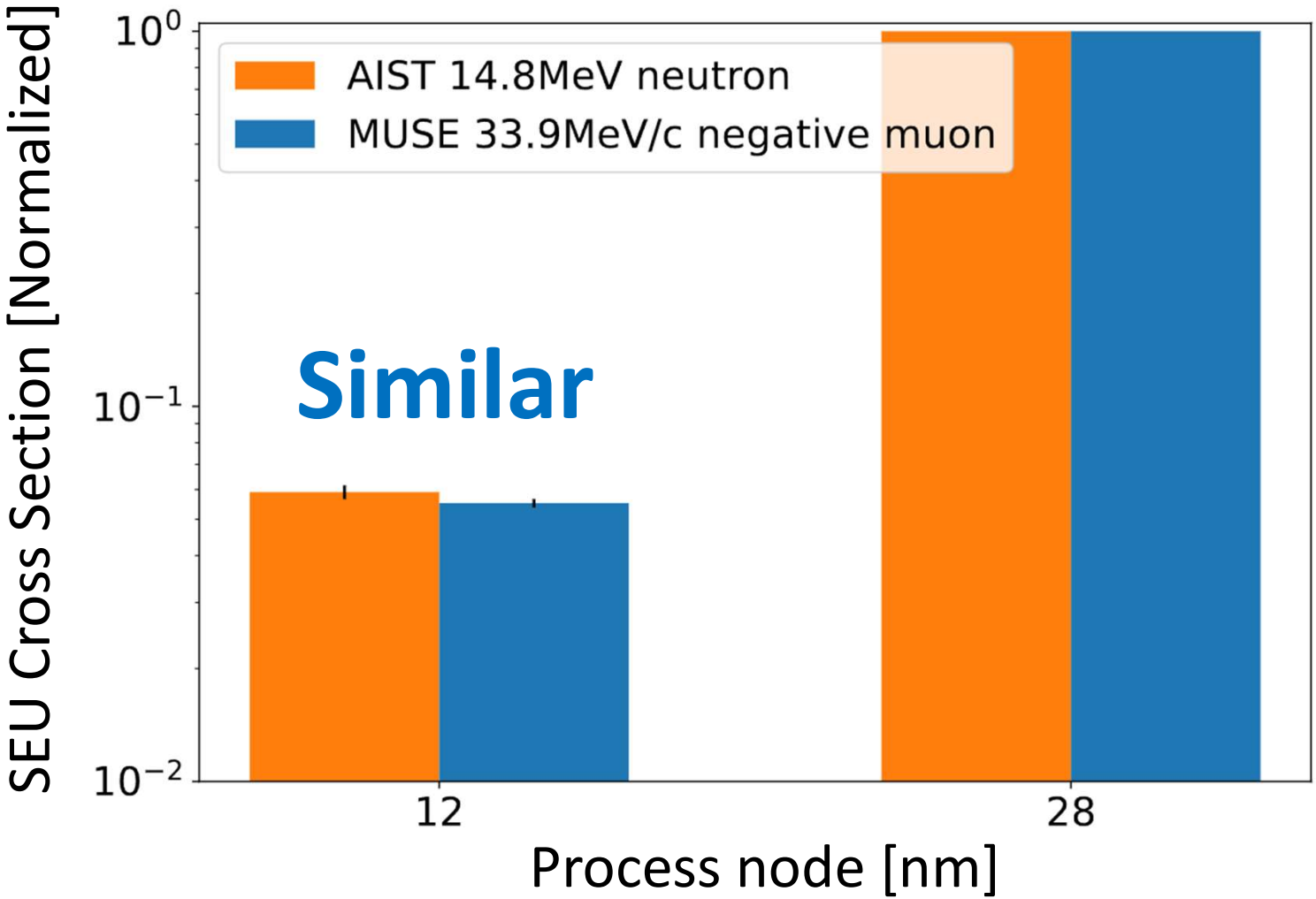


Comparison b/w μ^- and neutron

[Gomi, RADECS 2023]

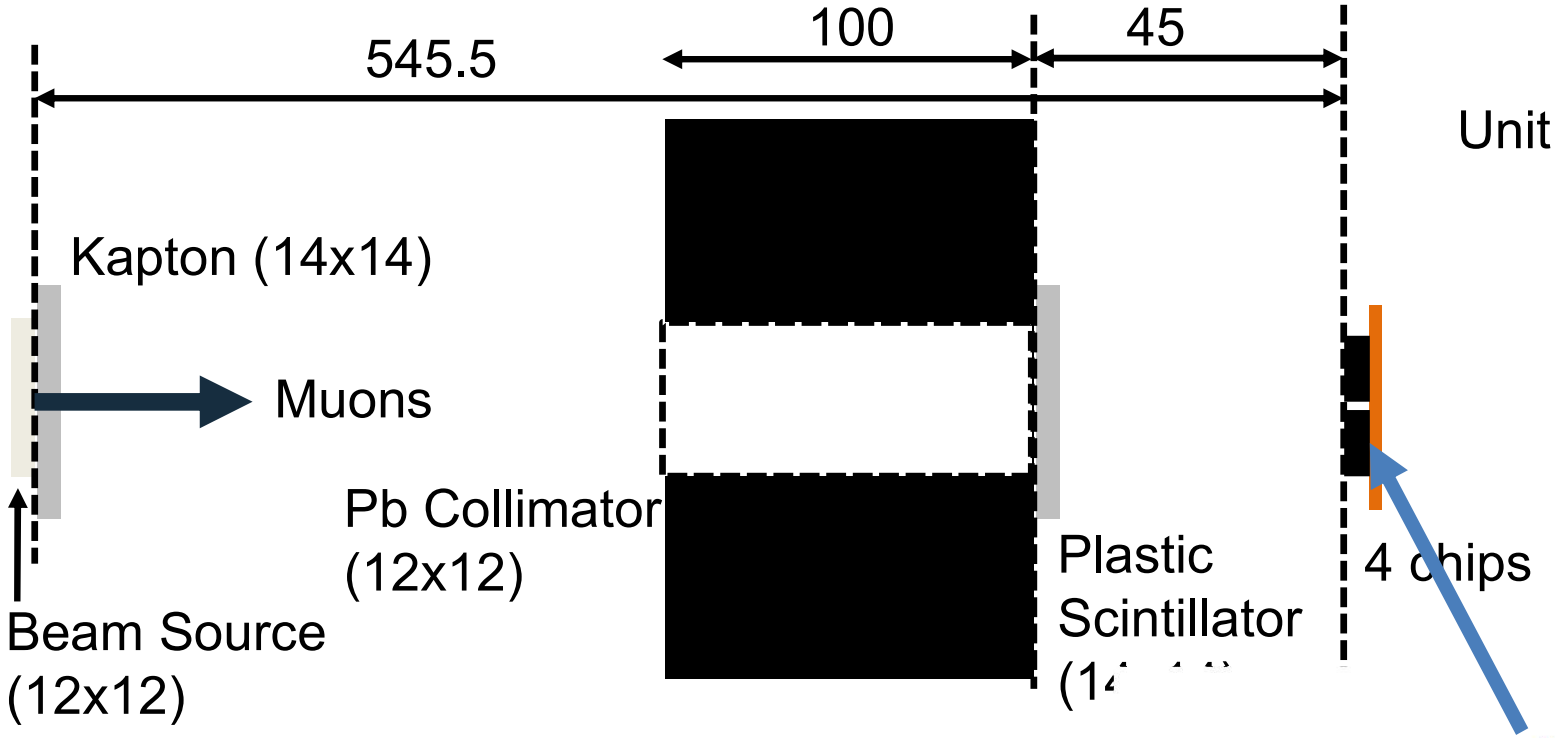
Similar reduction ratio from 28nm to 12nm

- **Similar secondary ions are causing SEUs**

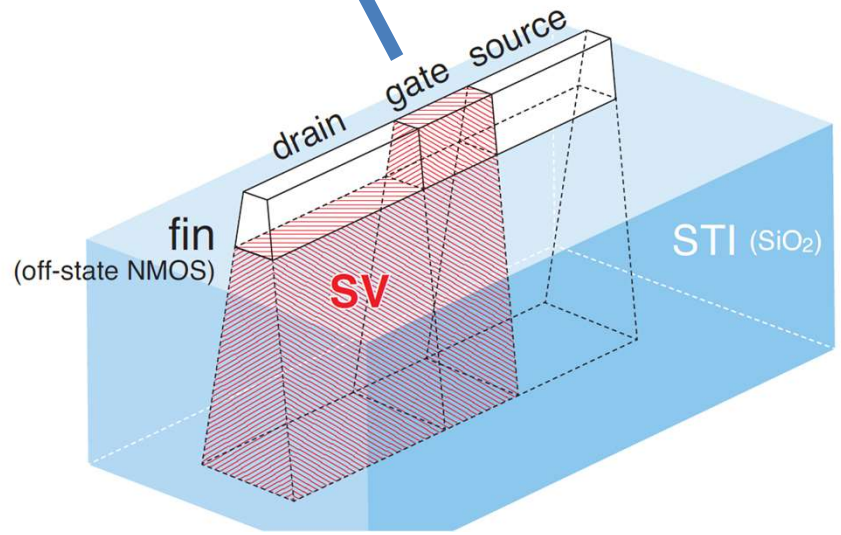


Simulation setup

- SEU cross sections were simulated using PHITS and single sensitive volume (SV) method.



Locate SV for each memory bit.



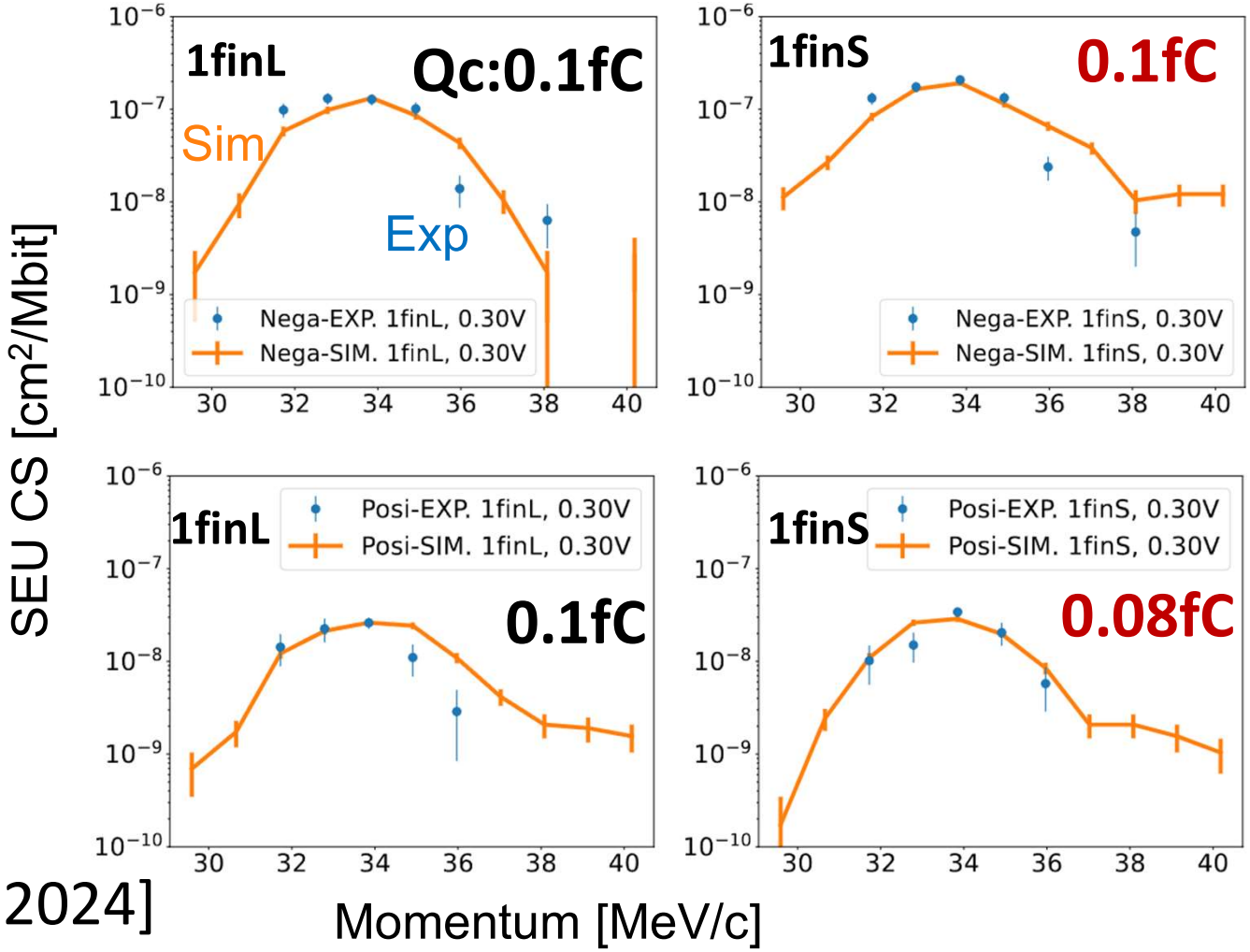
[Gomi, RADECS 2024]

Simulated SEU cross sections

- Experimental results were mostly reproduced.
- However, different Qc values for positive and negative muons. -> Further investigation is necessary.

Positive Muons

Negative Muons

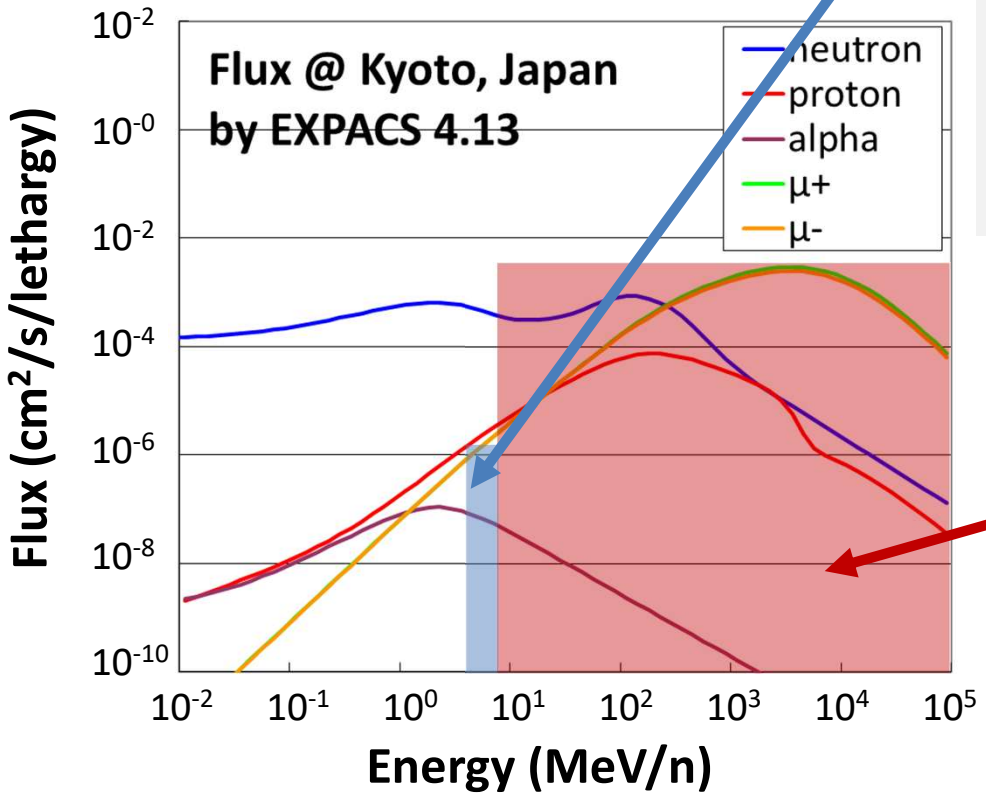


[Gomi, RADECS 2024]

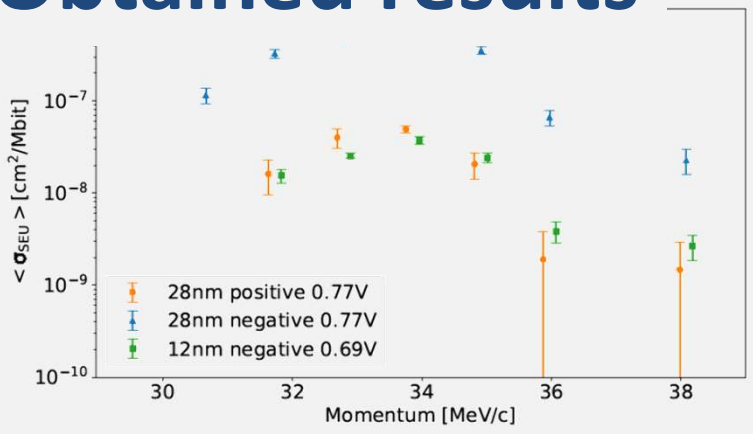
Conclusion and future direction

- Muons stopping near transistors cause SEUs.
- No increase to 12nm FinFET similar to neutrons

Need to know muon-induced SEU cross section across all energy range



Obtained results



No evaluation despite abundant muons (even e^- can induce SEUs)