

# **QUP Workshop**

## **Development of Cryo CMOS ASICs for Qubit Controller**

**Apr/9/2025**

**QUP, IPNS ITDC E-sys, KEK**

**Masaya Miyahara**

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# Contents

- **Project Overview**
- **Development status of Cryo CMOS ASICs**
  - ✓ Ring Oscillator
  - ✓ Analog to Digital Converter (ADC)
  - ✓ Digital to Analog Converter (DAC)
- **Conclusion & Future Works**

# Development of Scalable Highly Integrated Quantum Bit Error Correction System

Project Manager: Kazutoshi Kobayashi

Kyoto Institute of Technology (KIT), Japan



Search "QUBECS"

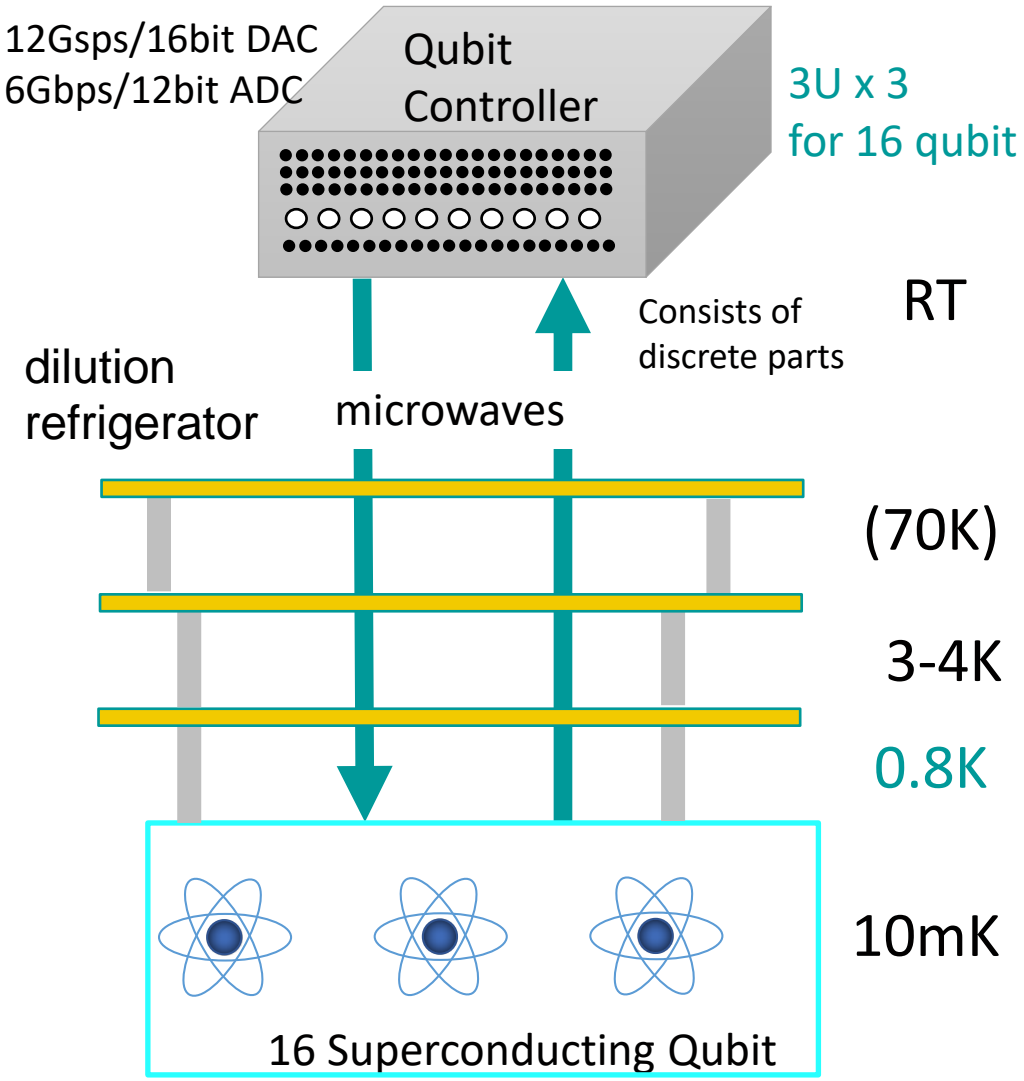
<https://www.greenlab.kit.ac.jp/qubecs/>

Project started from Oct./2022

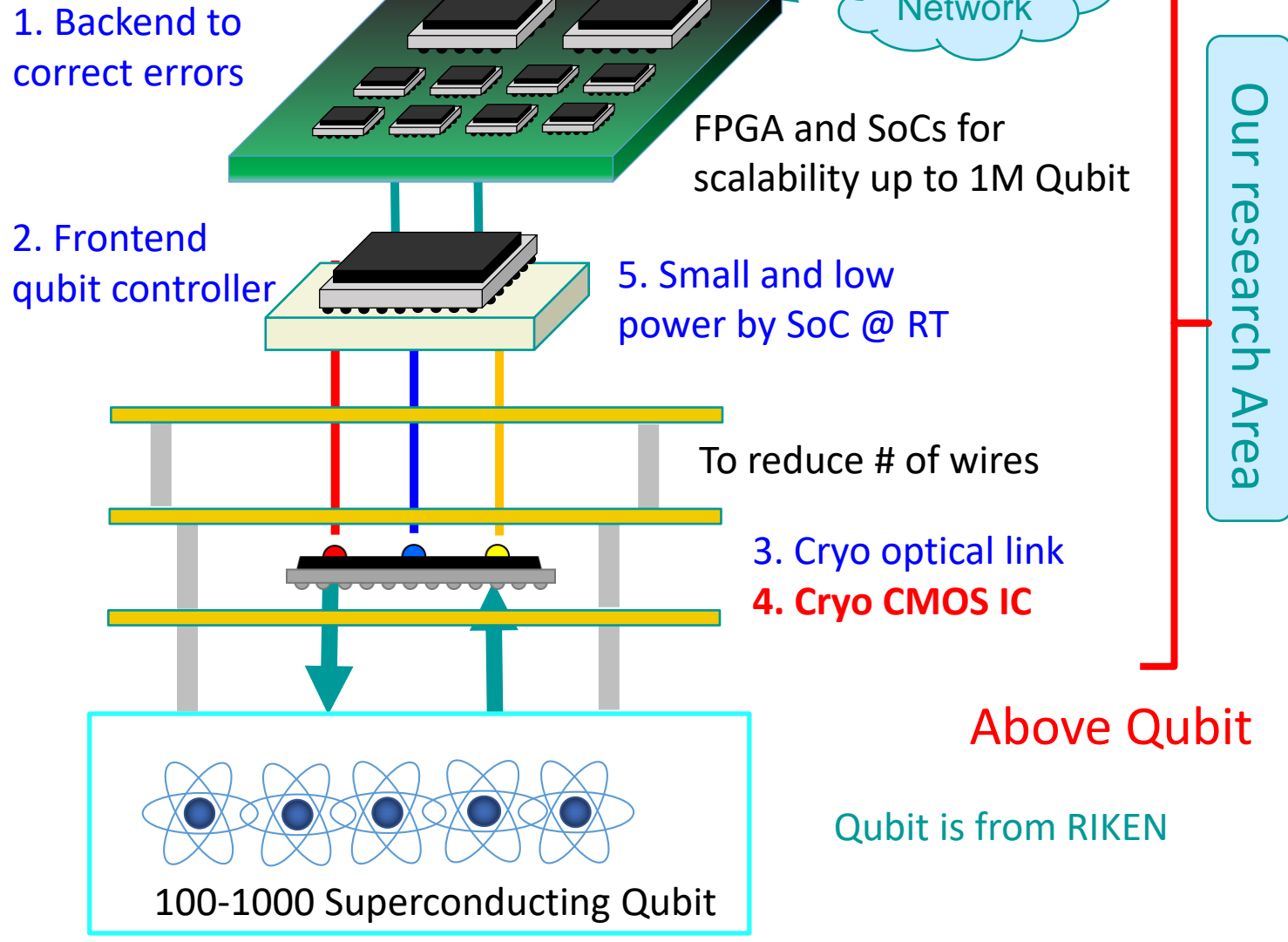
# Outline

## From NISQ to FTQC

NISQ=Noisy Intermediate-Scale Quantum, FTQC=Fault Tolerant Quantum Computer



Current small-size QC

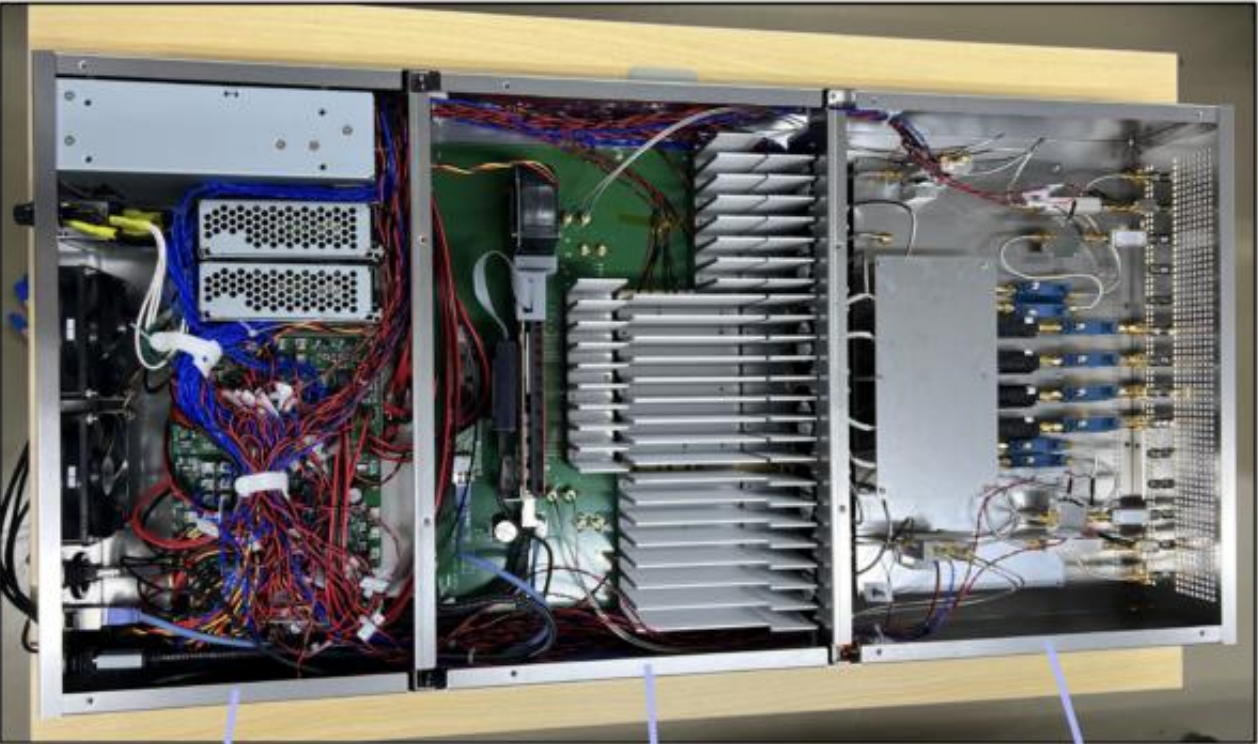


Our targeted scalable QC

Our research Area

# Qubit Controller: QuEL-1

<https://quel-inc.com/product/>



Board for DC supply and temperature control

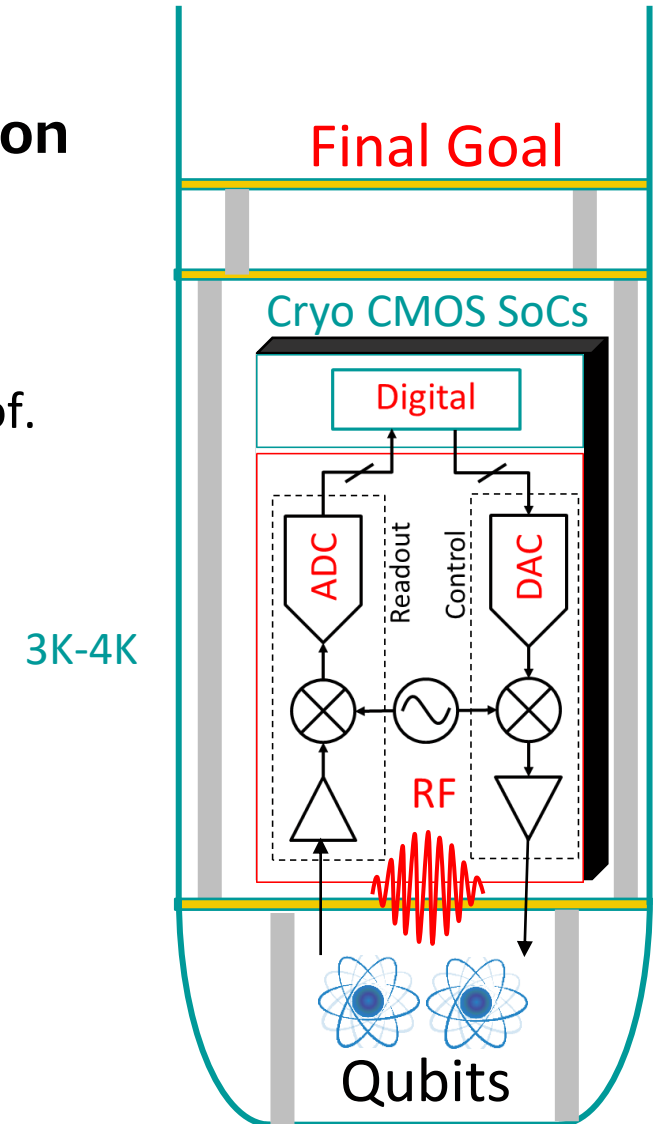
System board  
FPGA  
ADC/DAC  
Mixer + LO

Residual MW components  
Bandpass filters  
Multipliers (option)  
Combiners, etc.

Transmitter	8 channels Resolution : 16 bit Sampling rate : 12 GSPS Bandwidth: 500 MHz – 2.0 GHz Frequency: 7-11 GHz (19-22 GHz with multiplier option)
Receiver	4 channels Resolution : 12 bit Sampling rate : 6 GSPS Bandwidth: 500 MHz – 2.0 GHz Frequency: 7-11 GHz
Interface	10GbE x4 (for data transport) GbE x1 (for control) HDMI x1 (for reference clock)
Size	W 440mm x H 124mm x L 900mm 3U (can be installed in a 19-inch rack)

# Subject 4 : Cryo CMOS ASICs for Frontend/Backend

- **Goal: Implementing ASICs operating at a cryogenic temperature to control qubits (Frontend) and error correction (Backend)**
- **Research items**
  - ✓ **Digital** circuit implementation and reliability enhancement techniques (Prof. Kobayashi, KIT, Japan)
  - ✓ **RF** frontend circuit (Prof. Tsuchiya, Shiga Pref. Univ., Japan)
  - ✓ High-speed **DAC** for frontend (Prof. Takai, KIT, Japan)
  - ✓ **High speed ADC for front end (Prof. Miyahara, KEK, Japan)**



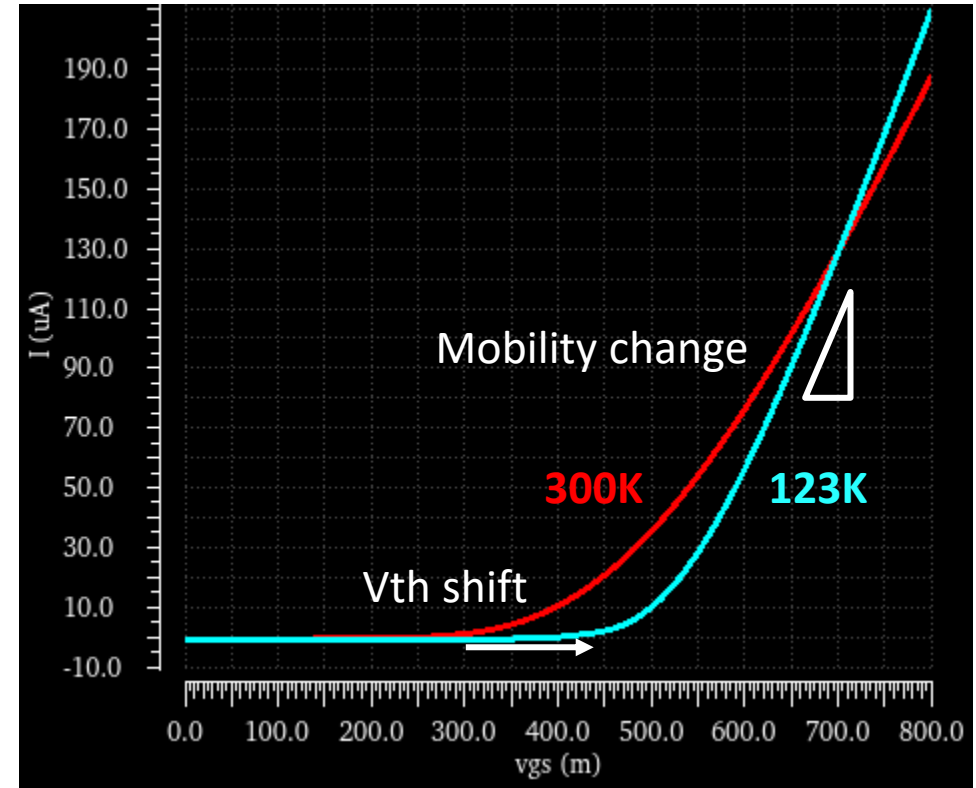
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# Design Challenge of Cryogenic CMOS ASIC

- 22nm planer bulk CMOS process
- No Process Design Kit (PDK) @ 4K
  - ✓ General PDK supports down to -40°C (233K)
    - Although it is not official, it can simulate temperatures down to about -150°C (123K).
    - Another PI is trying to make device model @4K
      - ❑ It will take time to make an accurate simulation model, I decided to make circuit using current PDK.
- Characteristics of devices
  - ✓ Transistor
    - Increasing threshold voltage → decreasing current
    - Increasing carrier mobility → increasing current
  - ✓ Passive components (resistor, capacitor, inductor)
    - Temperature coefficient

$$I_D = \frac{\mu C_{ox} W}{2} \frac{V_{GS} - V_{th}}{L}^2 (1 + \lambda V_{DS})$$



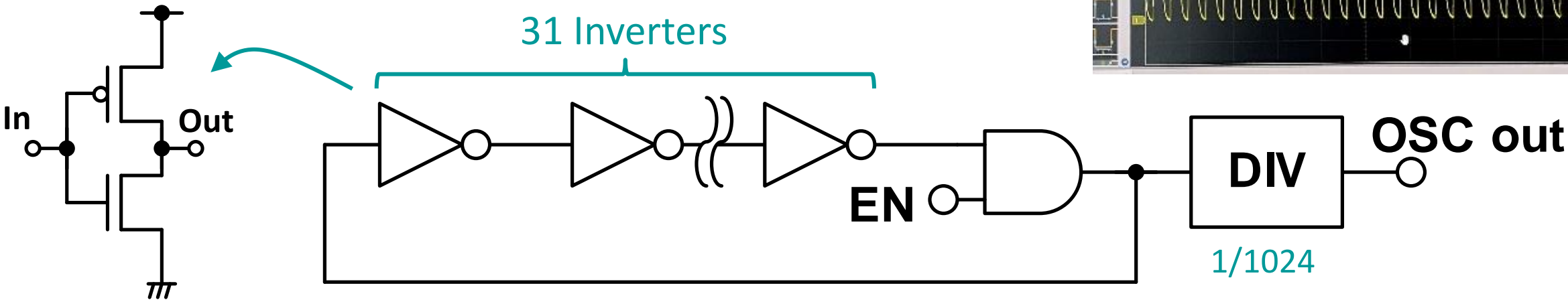
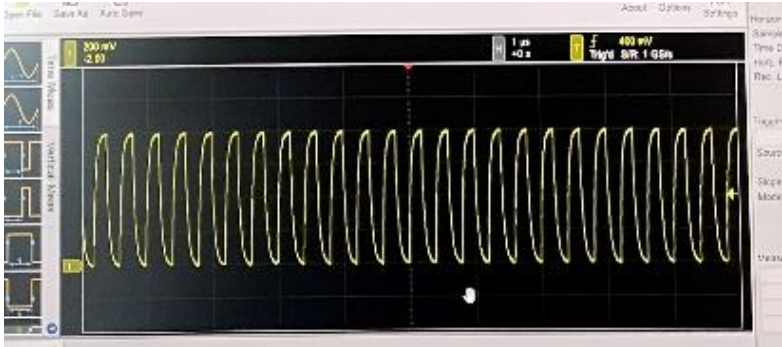
NMOS Transistor I-V curve

# Cryogenic Ring Oscillator

- **Ring OSC. (31 INV+1 AND with 1/1024 divider)**

- ✓ Digital standard cell-based design for checking the operating speed of digital circuits.
  - Oscillation frequency is proportional to operating speed
- ✓ 3 types of threshold voltage
  - Ultra Low Vth (ULVT)
  - Low Vth (LVT)
  - Regular Vth (RVT)

Higher frequency is expected



# Measurement setup

4K test environment was developed by supporting from Cryogenic group in ITDC.



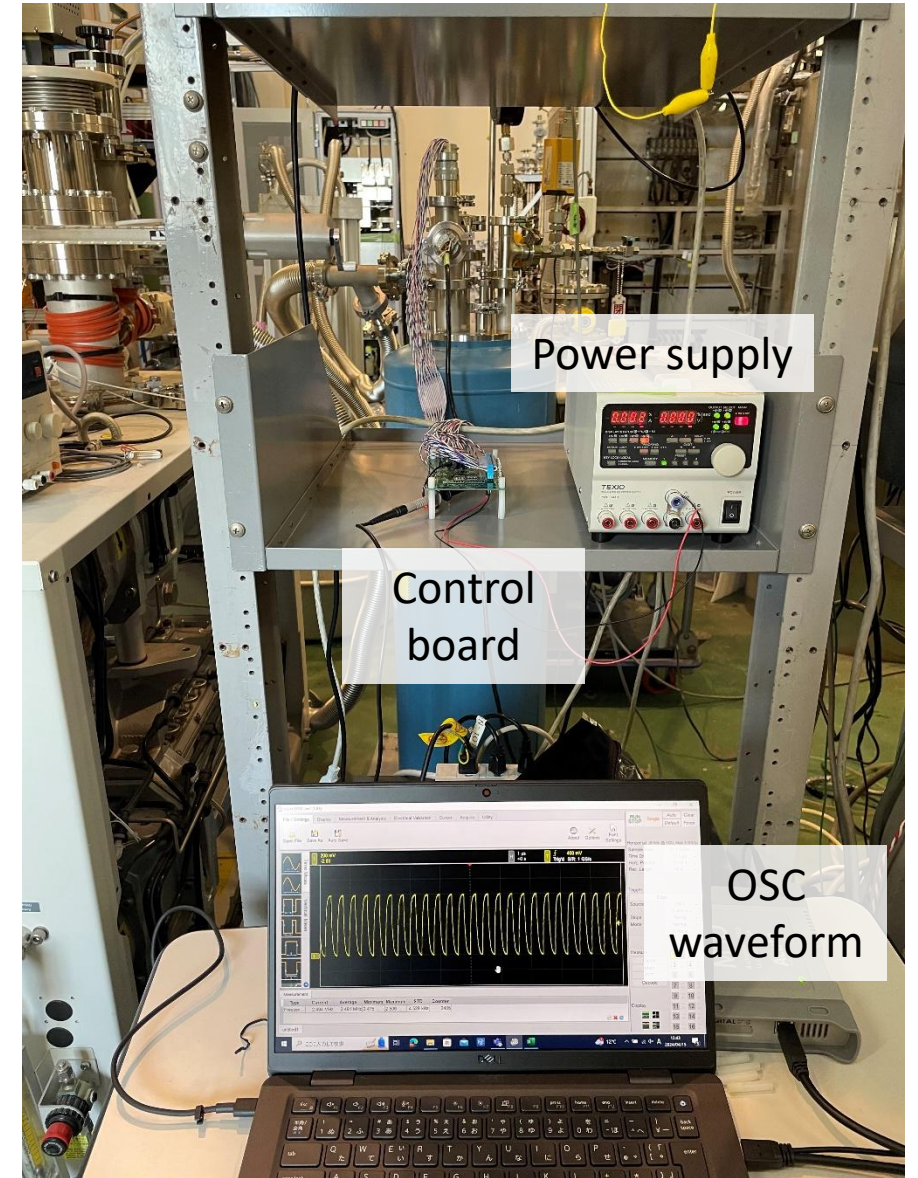
Dewar



Insert

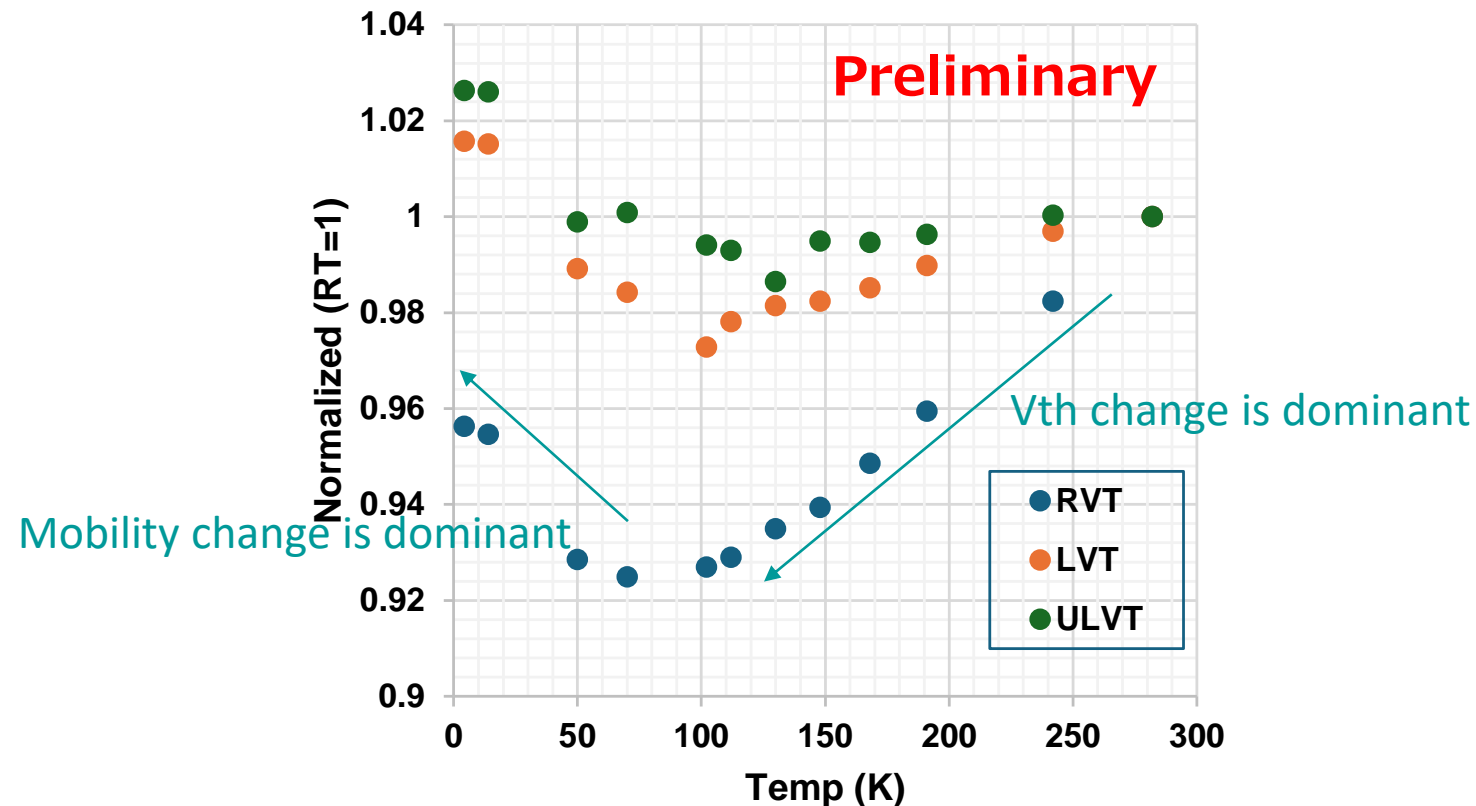
Coaxial Cable  
8  
Std. Cable  
96

Typical  
Board size  
12 x 12 cm<sup>2</sup>



# Ring oscillator measurement result

- Oscillation frequency is fluctuated by changing threshold voltage and mobility.
  - ✓ The higher the threshold voltage, the larger the effect of frequency decrease.
  - ✓ LVT and ULVT are within  $\pm 2\%$   $\rightarrow$  small effect on operating speed of digital circuits.



## Frequency variation of ring OSCs

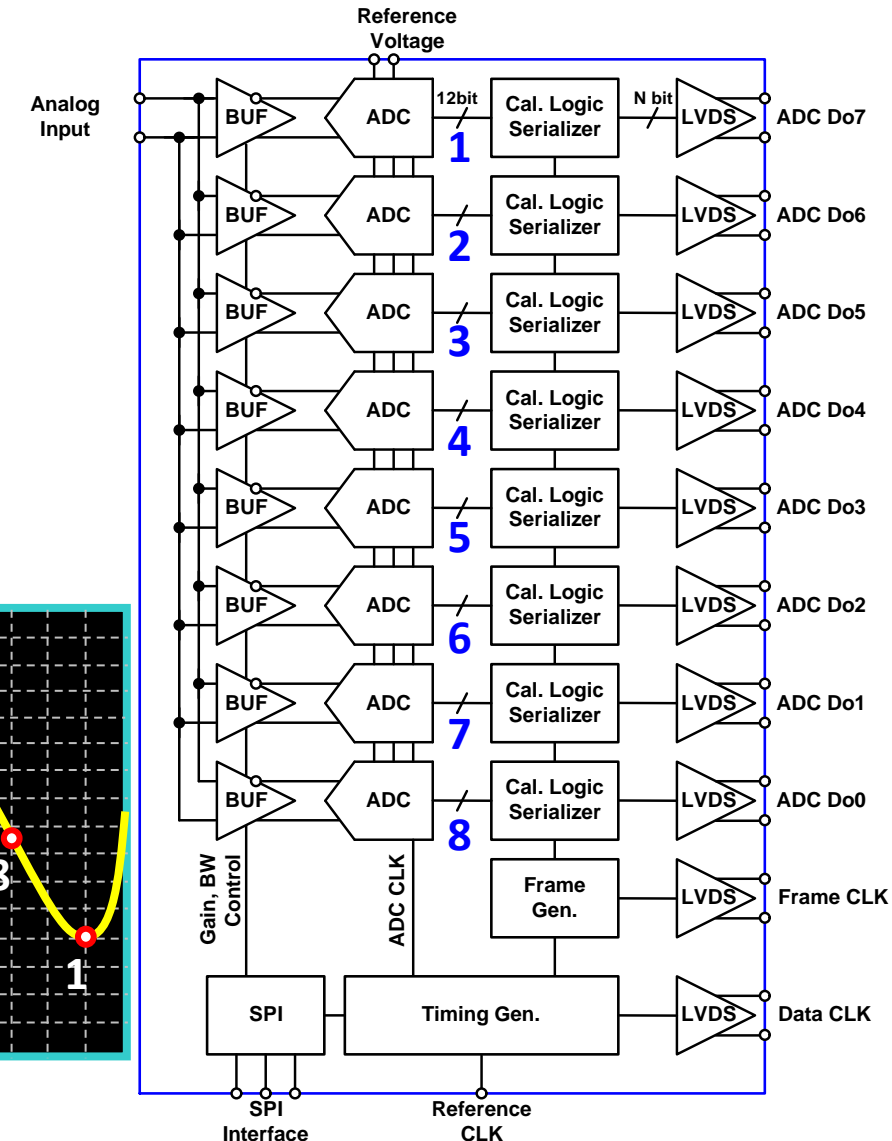
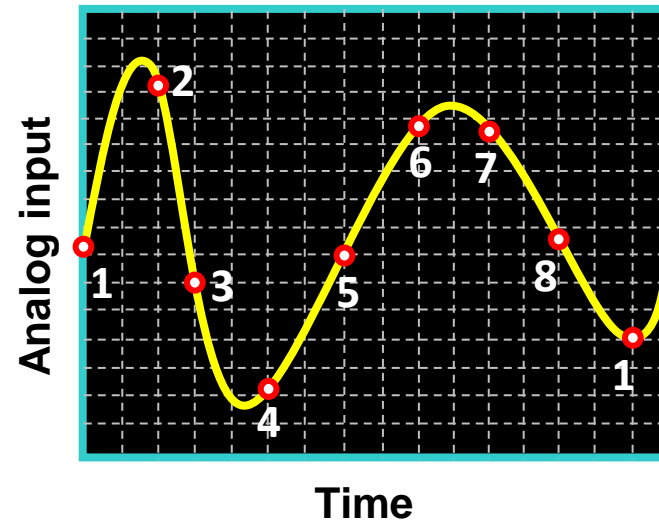
# Target of Cryo ADC Development

## ● Target specification

- ✓ Resolution: 8~12bit
- ✓ Sampling rate: 1~6GS/s
- ✓ Temperature: 300~4K
  - The target performance will be changed based on cooling capacity and Qubit observability.

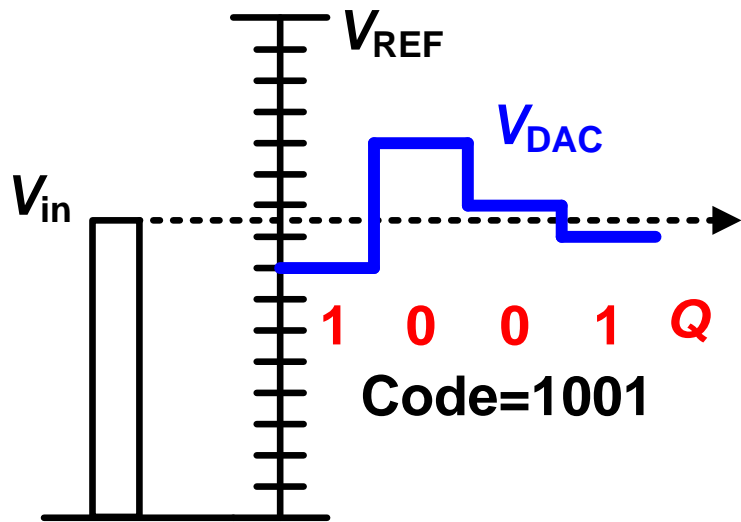
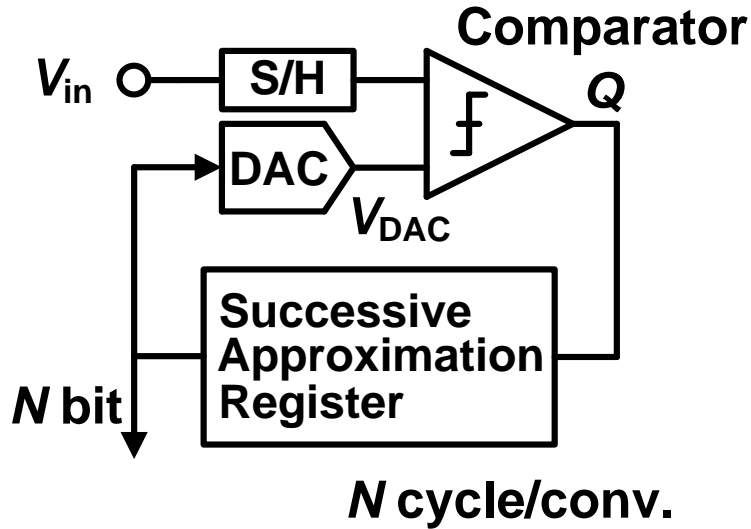
## ● Challenges

- ✓ Development of scalable ADC architecture suitable for interleaved operation
- ✓ Development of calibration techniques for channel-to-channel mismatches with flexibility

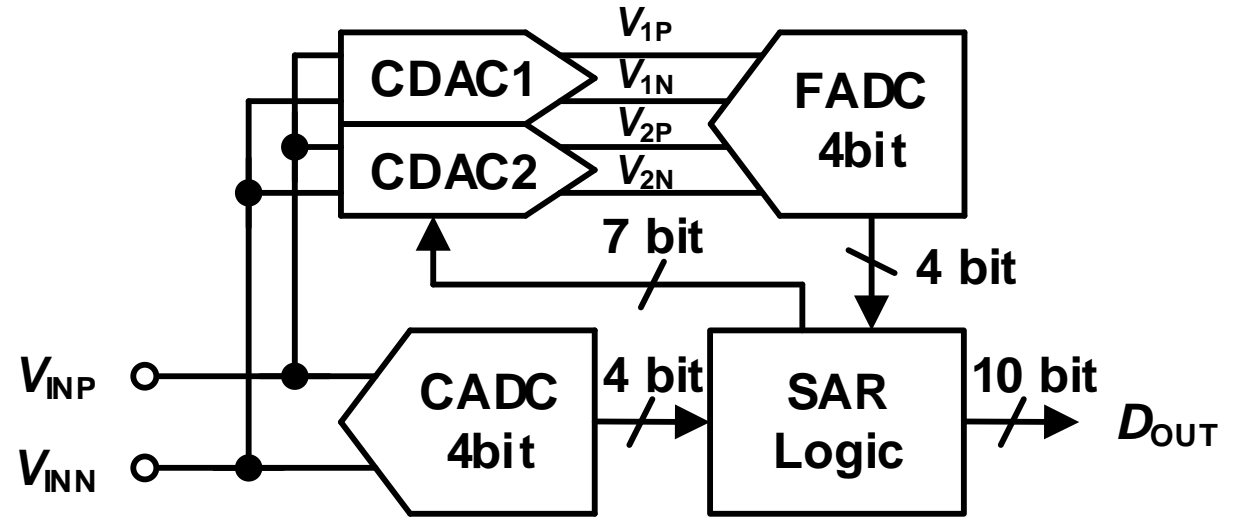


Time-interleaved ADC (8x)

# Proposed ADC Architecture



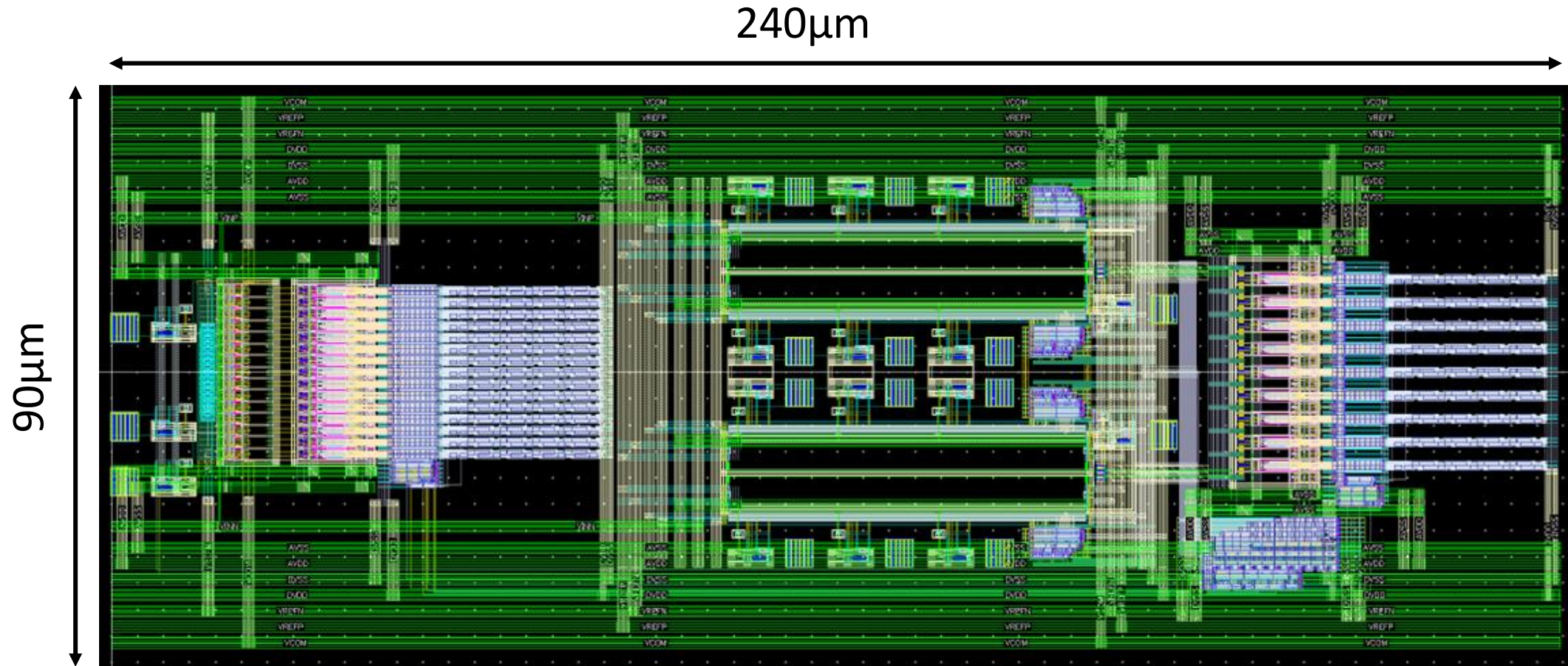
Conventional SAR ADC



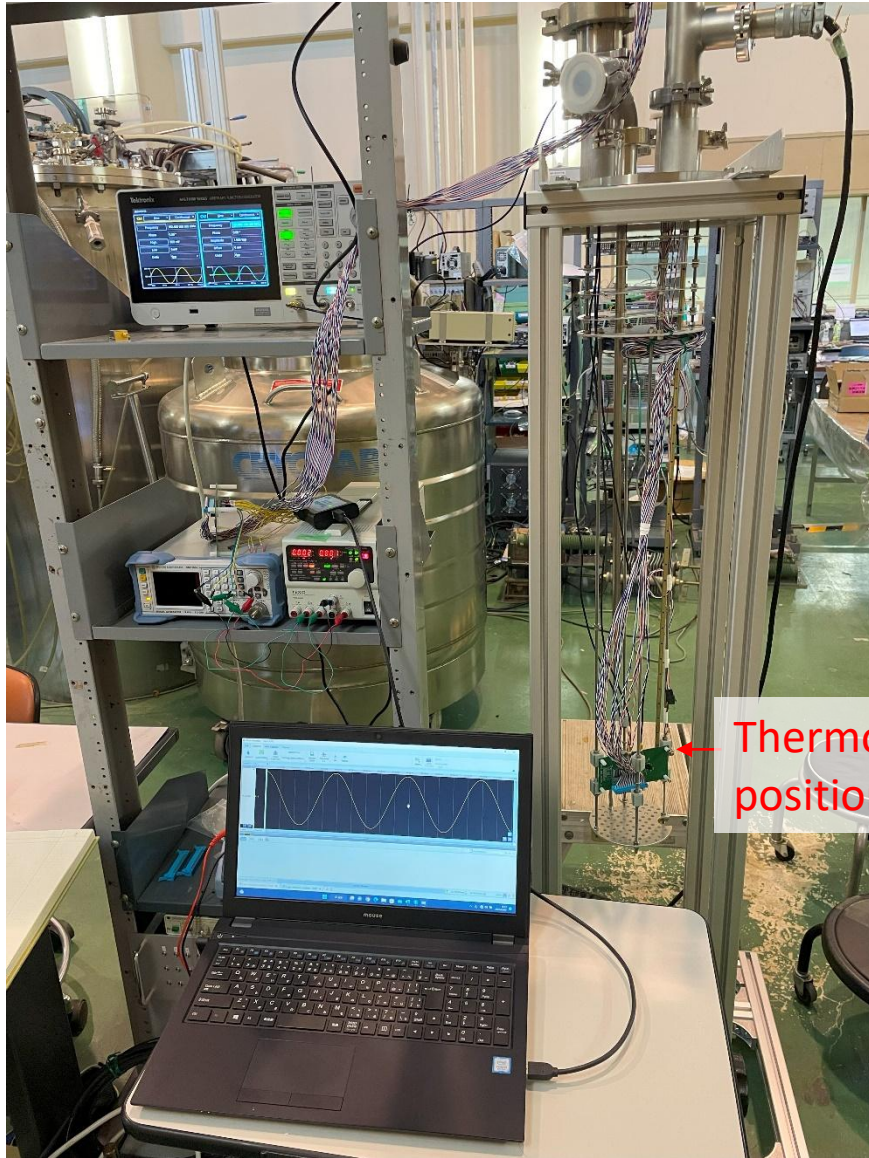
- 3bit conversion for higher speed.  
Ex.)  $N=10$ ,  $10 \rightarrow 3$  cycle/conv., **3x faster**
- Only one reference voltage thanks to interpolation technology
- Conversion errors other than the last can be ignored by redundancy
- CDAC and comparators determine ADC performance

# ADC Layout

1<sup>st</sup> prototype of ADC was fabricated using TSMC 22nm Bulk CMOS.  
Occupied area is 90 $\mu\text{m}$  x 240 $\mu\text{m}$ .



# Connection with Insert



Thermometer position

- **Concepts**

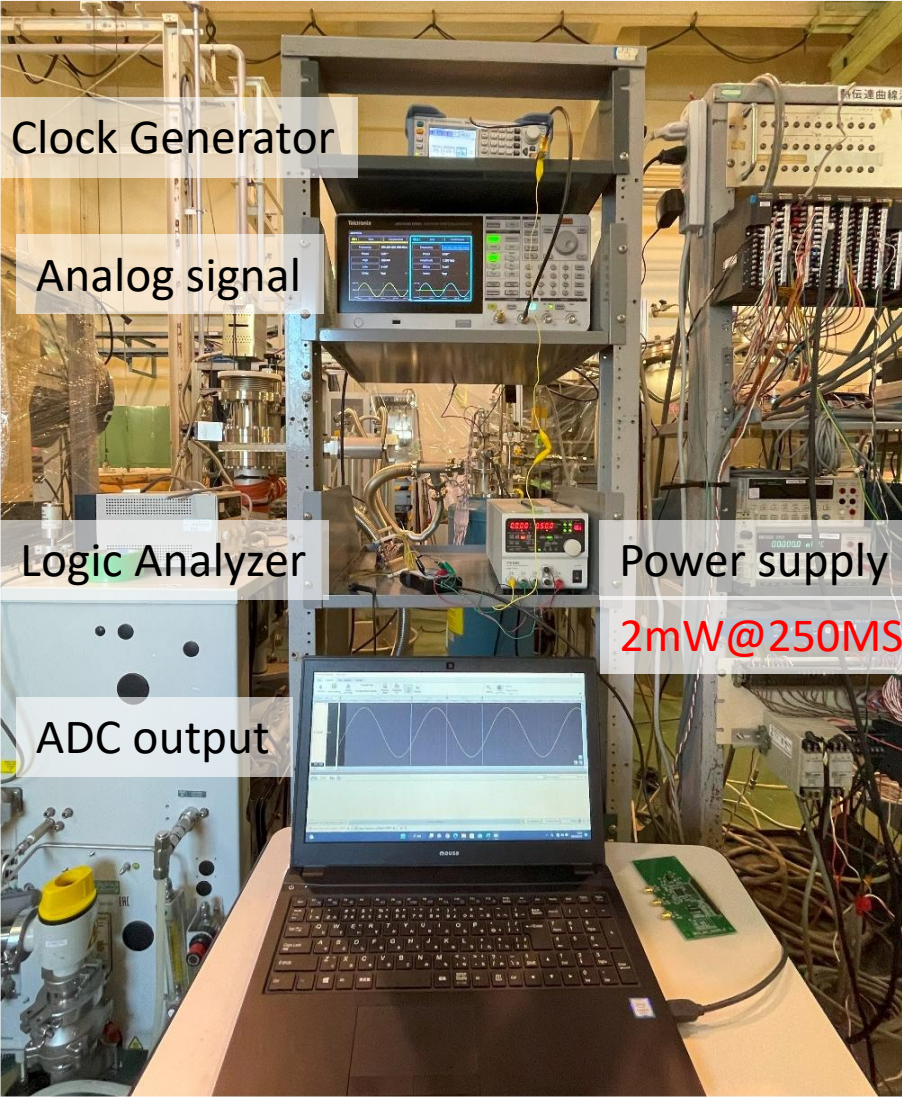
- ✓ 40 flat cables (1.27mm pitch) and 3 SMA cables are connected.
- ✓ Digital and clock output lines are twisted pair with ground line.
- ✓ A balun is used to generate differential signals for the analog inputs of the ADC.



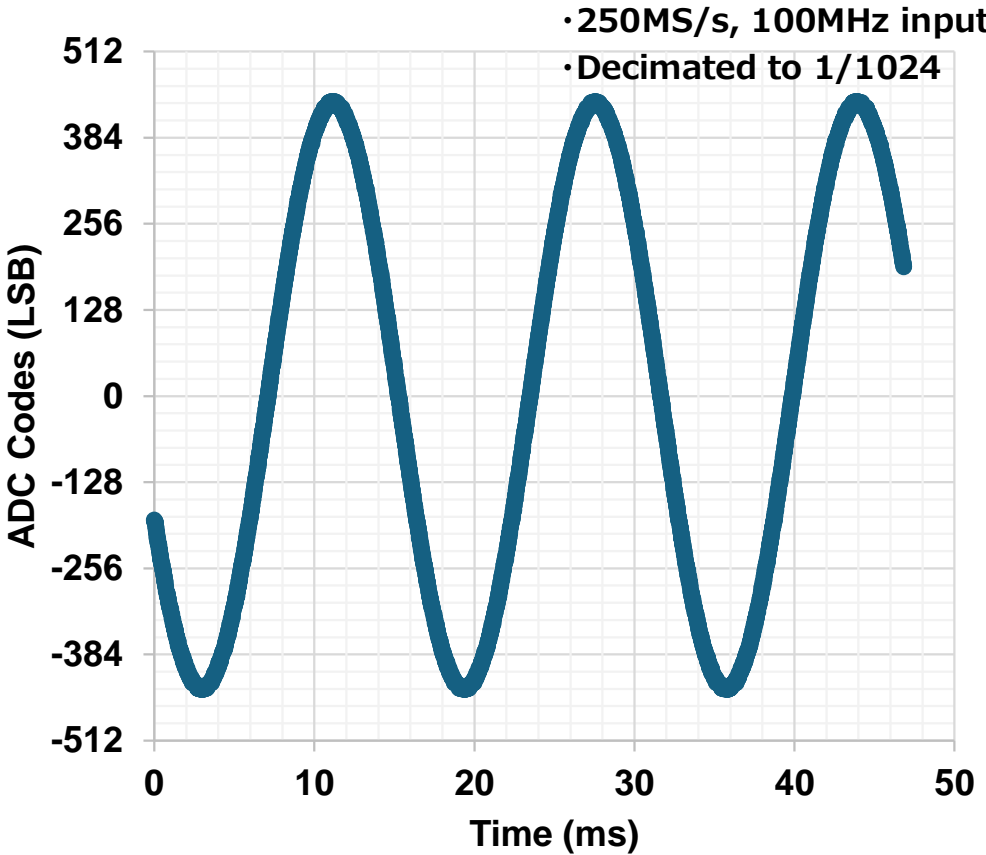
Balun

Setting of balun

# Measurement result of ADC



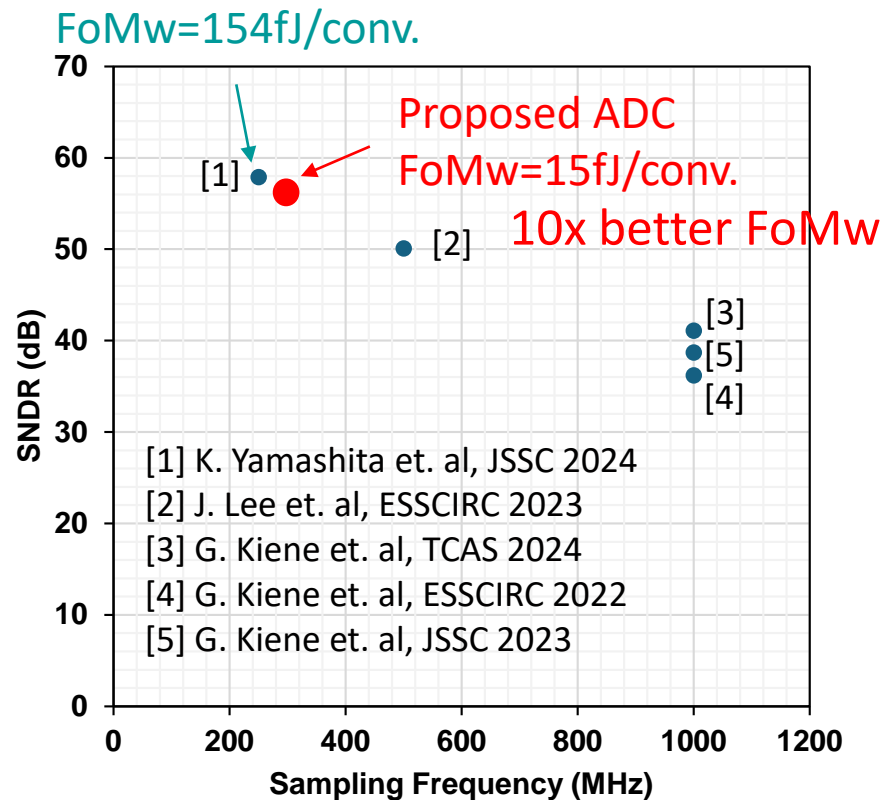
Proposed ADC has been confirmed to operate normally at 4.2K with no degradation in speed and accuracy.



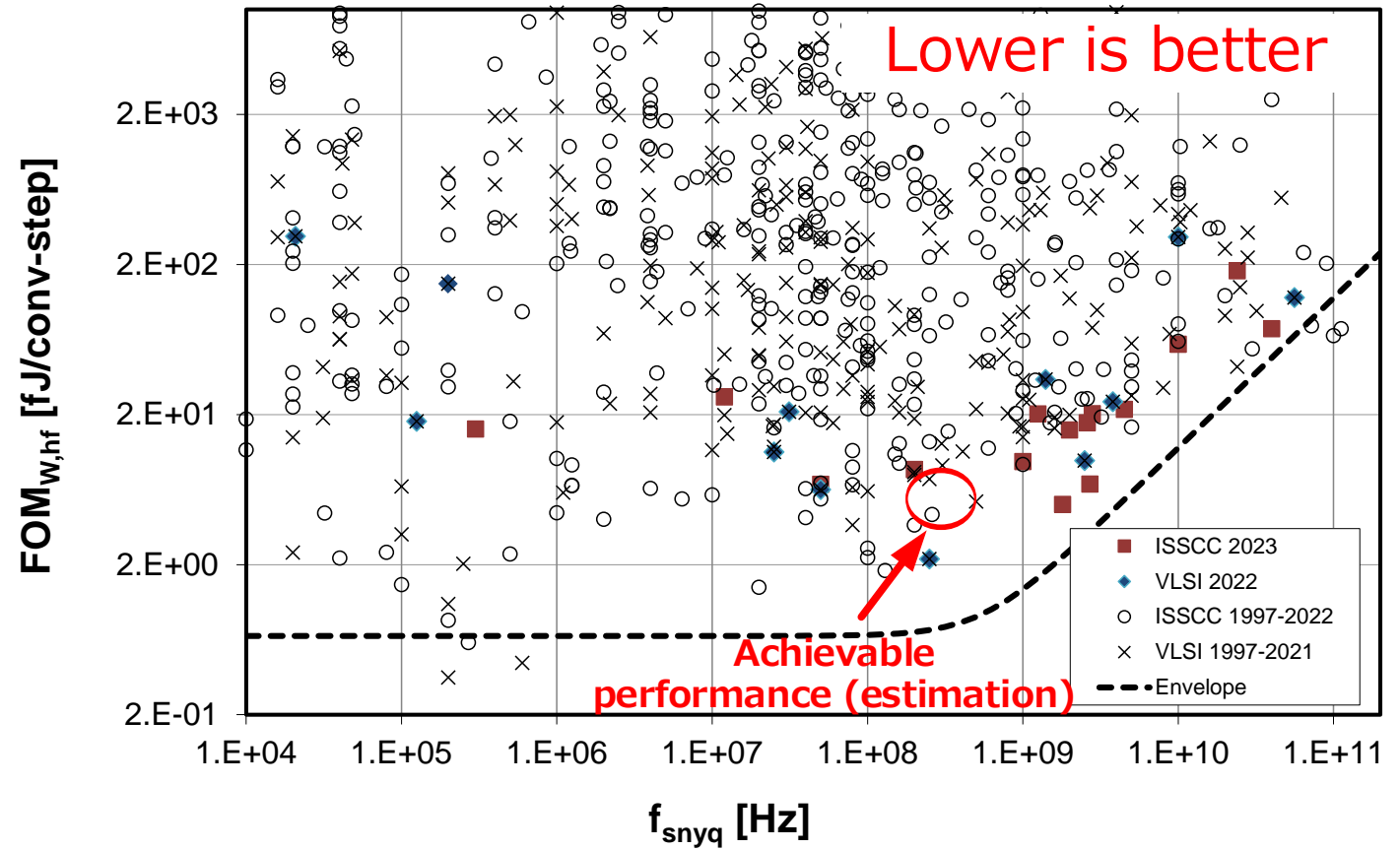
Sine wave input test of ADC @4.2K

# Performance comparison

$$FoM_W = \frac{P_D}{2^{ENOB} \cdot F_S} \text{ (J/conv.step)}$$



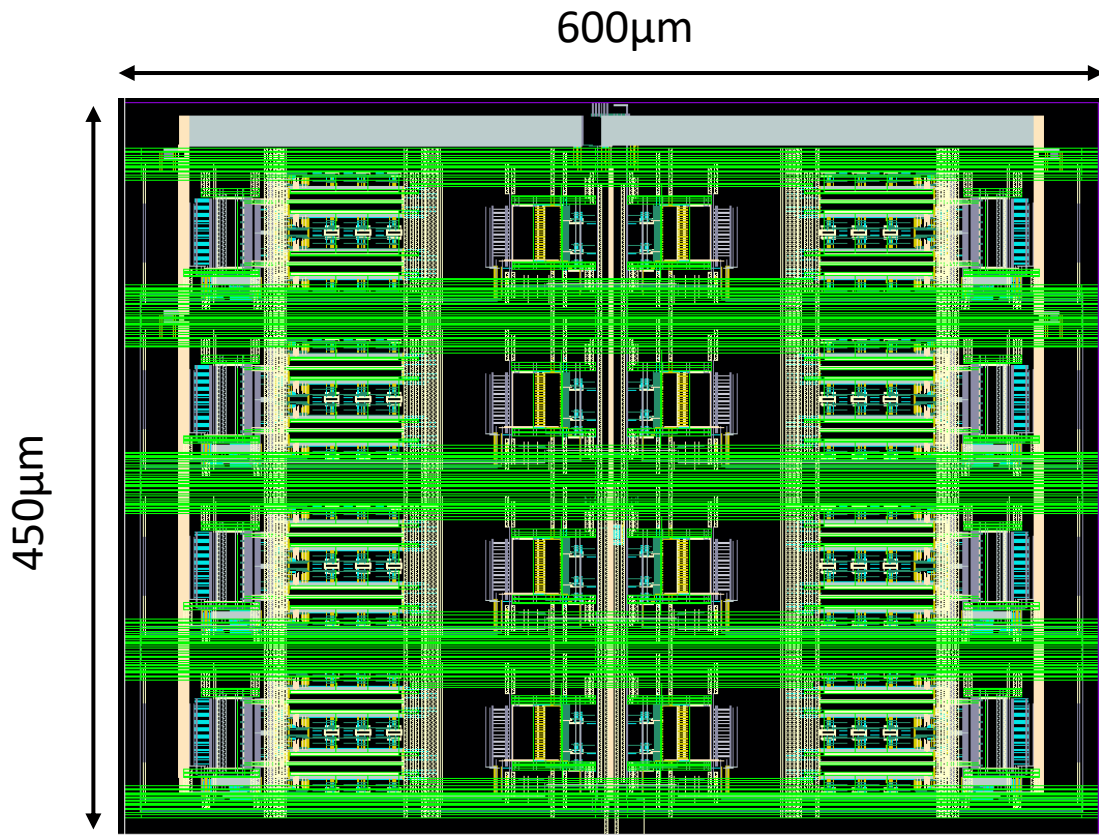
Performance comparison with Cryogenic ADCs



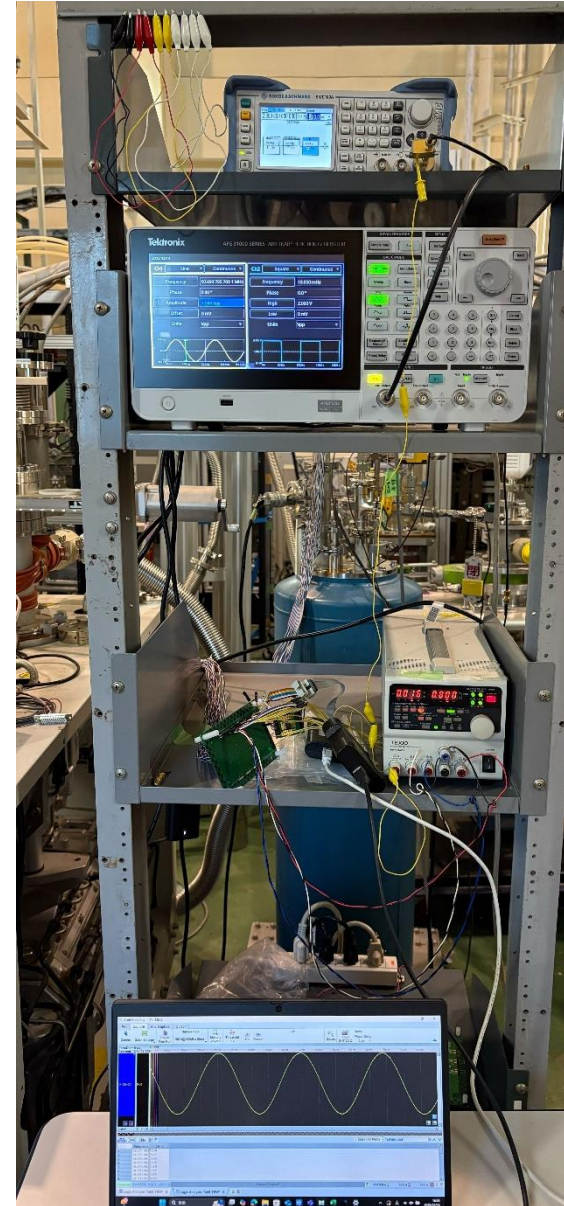
Performance comparison with state-of-the-art ADCs

# Latest result of ADC

- **8x Time-interleaving ADC**
  - ✓ 10bit, 2GS/s, 13mW ADC was properly operated at room temperature and 4.2K.



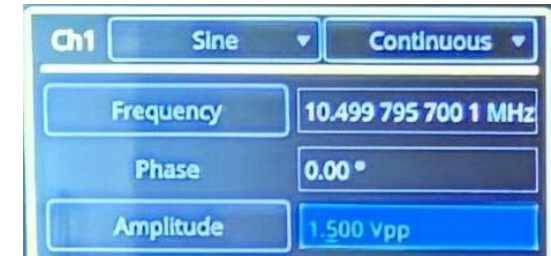
Time interleaved ADC layout



LHe test setup



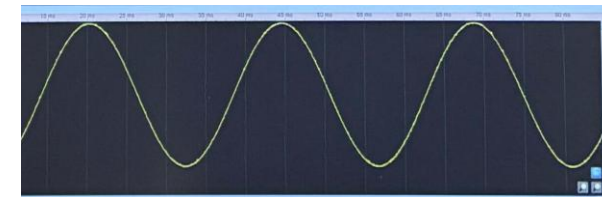
Clock Frequency



Analog input



Current Voltage  
Power supply

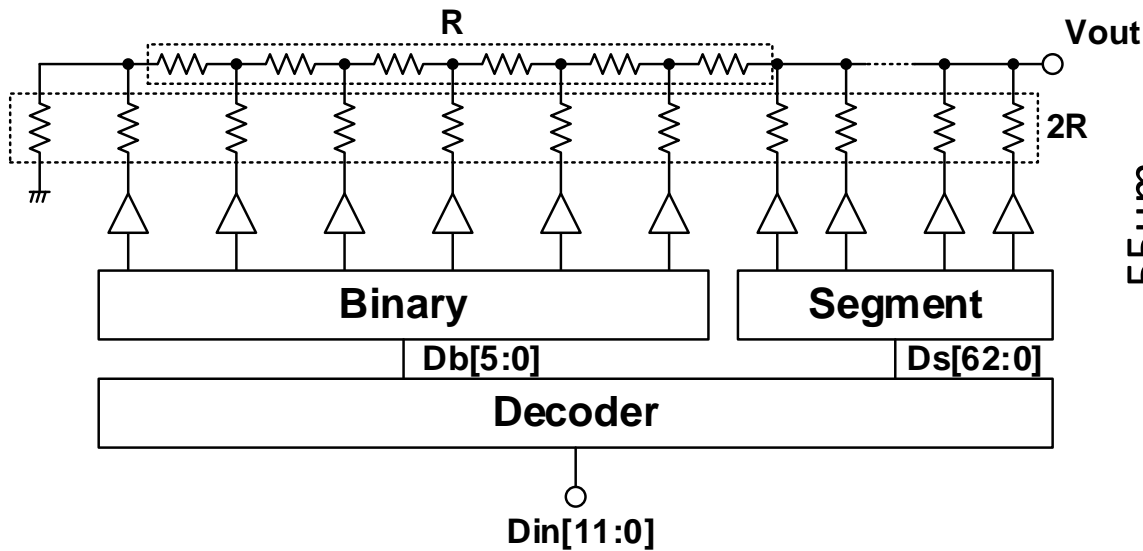


ADC digital output

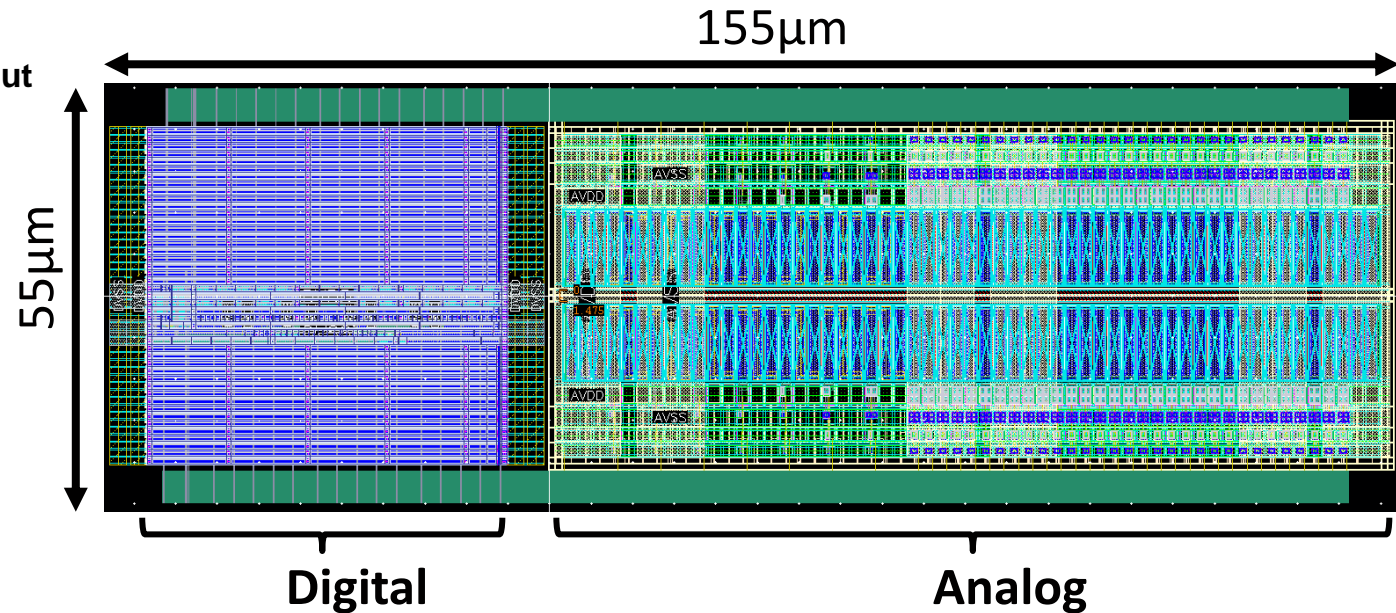
# Cryo CMOS DAC

- Analog signal generation for ADC testing

- ✓ Resolution : 12bit
- ✓ Sampling rate : 2GS/s
- ✓ 0~0.8V rail-to-rail output for single, -0.8V~+0.8V output for differential
- ✓ Output resistance: 200  $\Omega$
- ✓ Power consumption : ~5mW@2GS/s

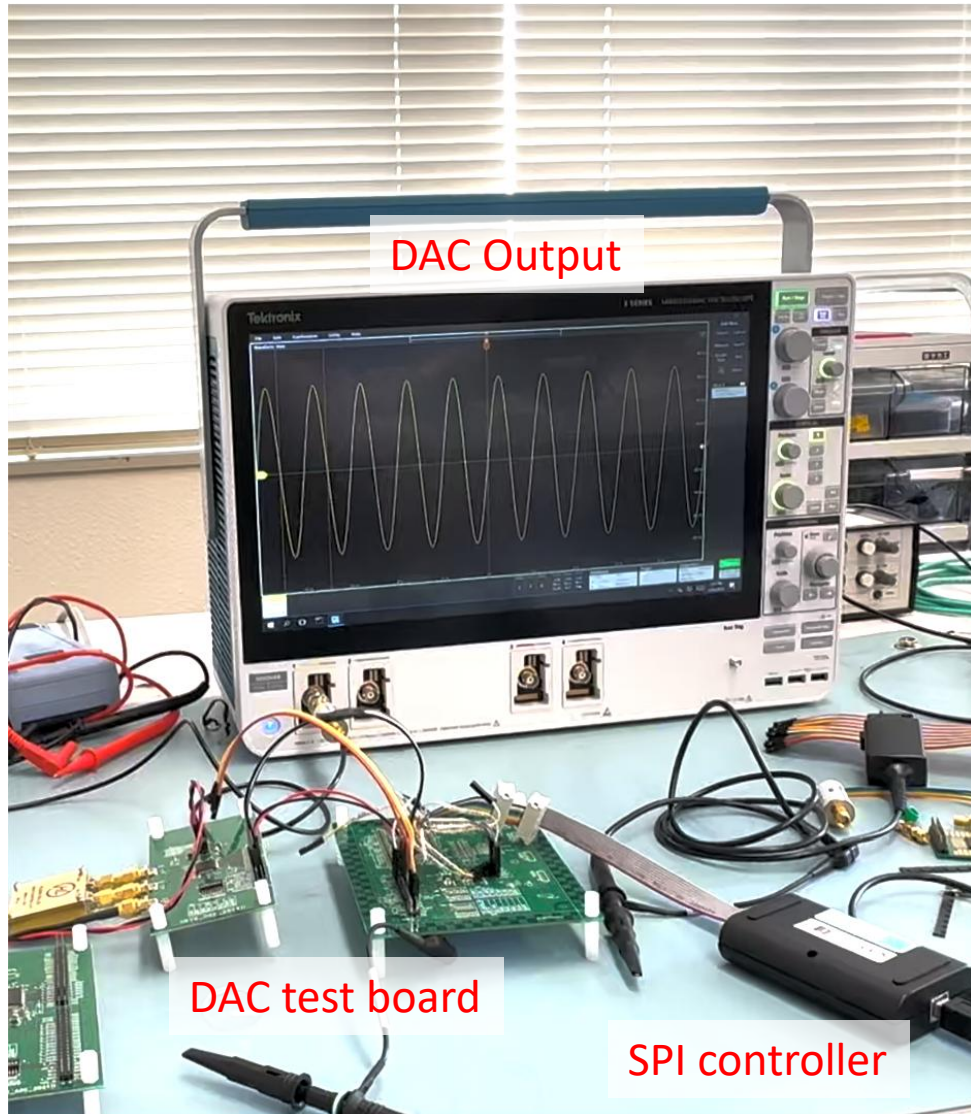


Hybrid resistor DAC



Layout

# Status of DAC measurement



- **Digital input**

- ✓ Sine wave generator (SWG, developed by Kyoto Institute of Technology) of digital data was implemented on chip.
- ✓ Arbitrary digital signals can be input from SPI.

- **Measurement results**

- ✓ **2GS/s operation @ RT**
- ✓ Demo video: 31.25MHz~250MHz sine wave output (1 sec. interval).
- ✓ An ASIC with integrated DAC and ADC has also been developed and is working properly.
- ✓ Scheduled for testing at 4.2K in Apr/2025.

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# Conclusion and Future works

## ● Conclusion

- ✓ Cryo CMOS ASICs for qubit controller operating at cryogenic temperatures ( $\sim 4\text{K}$ ) are developed.
- ✓ Prototype ASICs have been developed using a 22nm bulk CMOS process, and proper operation at 4.2K was confirmed.
  - 10bit 250MS/s ADC  $\rightarrow$  10bit 2GS/s ADC
  - 12bit 2GS/s DAC (Cryo test: Apr/2025)

## ● Future works

- ✓ Detailed evaluation at cryogenic temperatures
- ✓ Development and evaluation of SoC implementing more complex functions

# Acknowledgements

- **This work was supported by JST Moonshot R&D Grant Number JPMJMS226A.**
- **This work was also supported through the activities of VDEC, The University of Tokyo, in collaboration with Cadence Design Systems.**