

# NAT-MCH Gen4

MTCA workshop for accelerator and physics in Japan 2025

KEK, Tsukuba

August 28<sup>th</sup>, 2025

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## The new NAT-MCH Gen4 in 15 minutes

- Status of current NAT-MCH generation 3
- NAT-MCH-G4: the new NAT-MCH generation 4
- Migration from NAT-MCH Gen3 to NAT-MCH Gen4

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## NAT-MCH Gen3

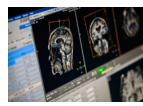
- Today the NAT-MCH Gen3 is being used in almost any vertical market:



Quantum Computer



Vision and AI



Medical



(Tele-) Communication



Military



Traffic



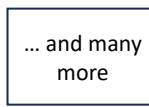
Research



Industrial Control



Test & Measurement



- The NAT-MCH Gen3 is shipped since early 2007 with more than 18.500 deployed units
- Component obsolescence and limitations for extensions require new design

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## NAT-MCH

Generation 4

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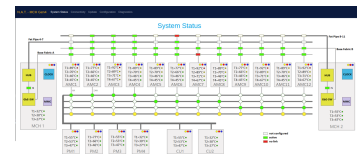
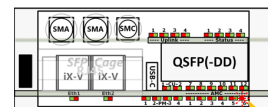
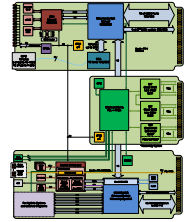
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## NAT-MCH Gen4 – in a nutshell

- New design providing new and improved functionality and optional features
  - Base MCH: Fabric A 10GbE, user core
  - CLK module: jitter cleaner, IEEE1588, optional OCXO and GPS
  - Ethernet Hub: 40/100GbE
  - PCIe Hub: PCIe gen5, optional optical uplinks
  - Harmonized CLI, new web interface
- Backward compatible with NAT-MCH Gen3
- Full form fit and function replacement
- Complies with MTCA.0 R3
- NextGen MTCA ready
- Open to future requirements



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## Main differences between Gen3 and Gen4 (excerpt)

	NAT-MCH Gen3	NAT-MCH Gen4 <i>(improvements)</i>
CPU + O/S + memory	Single core NXP Coldfire + OK1 + 64Mb	<b>Dual</b> ARM core (A9, Xilinx Zynq) + FreeRTOS + <b>1GB</b>
Base Switch	Broadcom 1GbE	Microchip 1/ <b>10/40GbE</b> , <b>dual ARM core</b> (A53)
Base Fabric + Uplinks	12x 1GbE + 2x 1GbE (RJ45)	12x 1/ <b>2.5/10GbE</b> + 2x 1/ <b>10GbE</b> (RJ45/ <b>IX/SFP-DD</b> )
Clock Module + ext. Input/output	CLK123, CLK12F, CLK-PHYS + dual input/output	<b>CLK-G4</b> + dual input/output and <b>GPS</b>
IEEE1588/SyncE + TSN support + OCXO	Not supported+ Not supported + NAMC-PTM	<b>Supported</b> + <b>Supported</b> + <b>OCXO</b>
Fat pipe Ethernet switch	Marvell Amstrong-LP 40GbE	Marvell Amstrong-LP 40GbE
Fat Pipe + Uplinks	12x XAUI + MPO	12x XAUI/ <b>10/40G</b> + <b>SFP-DD</b>
Fat pipe PCIe Switch + PCIe Gen	PLX + Gen3	MicroChip + <b>Gen4</b>
Fat Pipe + Uplinks	12x PCIe Gen3 + Finisar BOA (NAT-MCH-PHYS80)	12x PCIe <b>Gen4</b> + <b>SFP-DD</b>
Fat pipe SRIO Switch + SRIO Gen	IDT + Gen2	?
Fat Pipe + Uplinks	12x SRIO Gen2 + Infiniband	?
User Interfaces	CLI, Web (GoAhead) => Update with 2.22.x	<b>unified</b> CLI, <b>reworked</b> Web (Mongoose) <b>incl. CLI</b>
NATView: HPM update + backplane viewer + FRU-Ed	JRE on external device	<b>Integrated into Web interface</b> (excl. FRU-Editor)

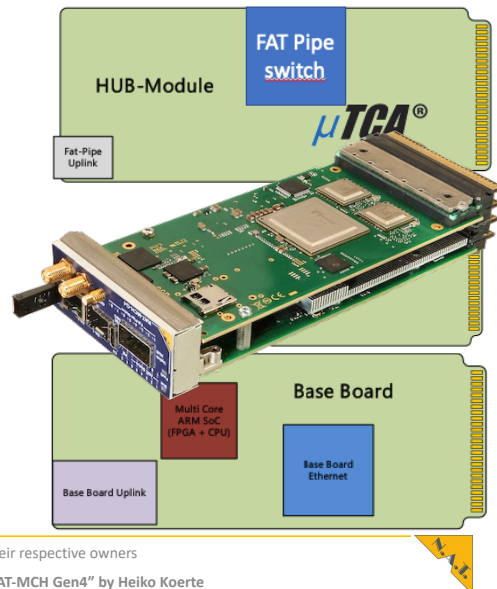
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## NAT-MCH-G4 – generation 4 building blocks

- **Fat-Pipe HUB Modules**
  - 1/10/40/100 GbE
  - PCIe gen4 (52-ports) + gen5 (84-ports)
  - QSFP/QSFP-DD uplinks for all Fat Pipes
- **Clock-Module (IEEE 1588)**
  - IEEE1588 support
  - Optional OXCO and GPS
  - Front panel I/O
- **Base Board**
  - Multi Core ARM SoC
  - Base Board Ethernet
  - Base Board Uplink



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## NAT-MCH Gen4

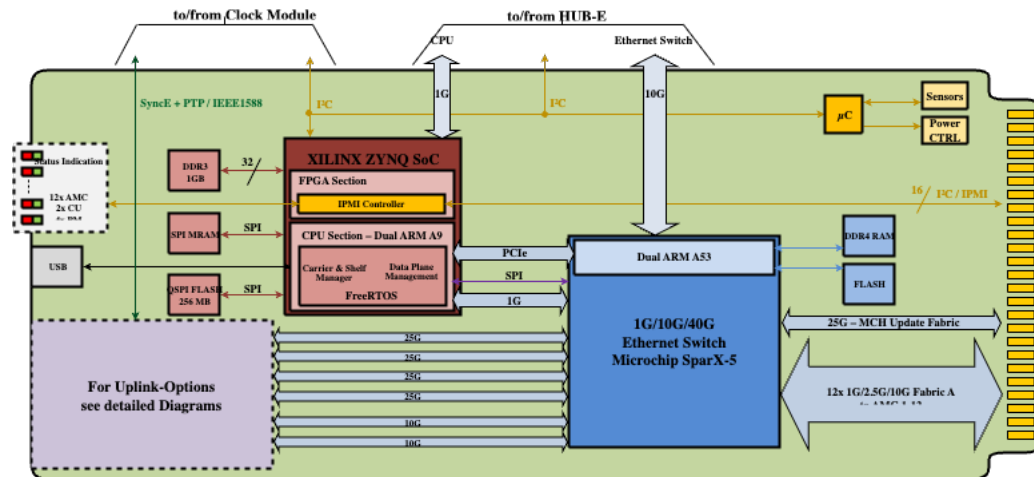
Base Boards

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## NAT-MCH-G4 (single-width base board)

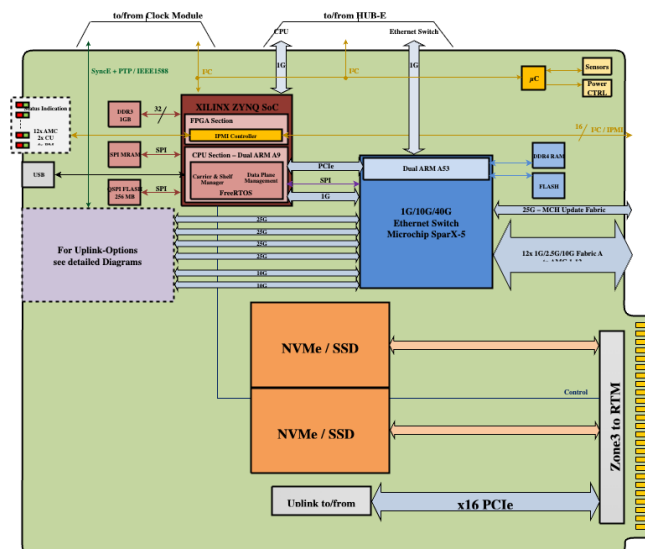


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## NAT-MCH-S4 (double-width base board)

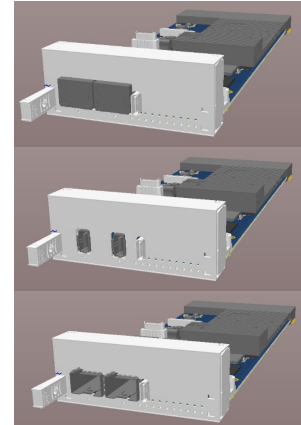
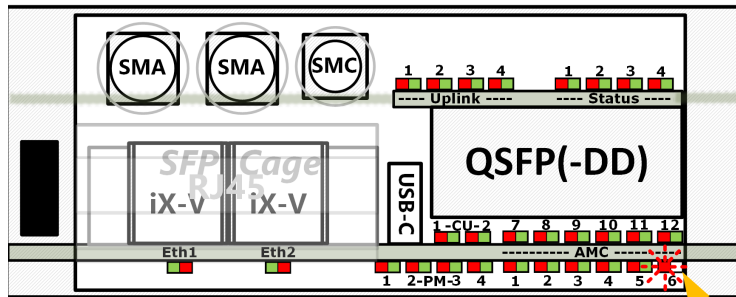


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## NAT-MCH-G4 – front panel view



Fault AMC1

- USB-C for serial terminal: debug + info + configuration
- Basic status indication via red/green LED

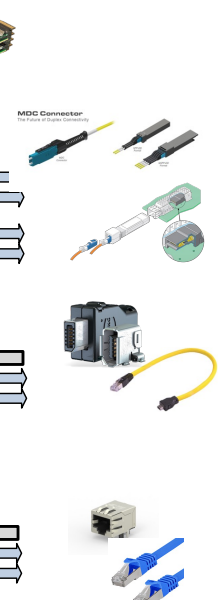
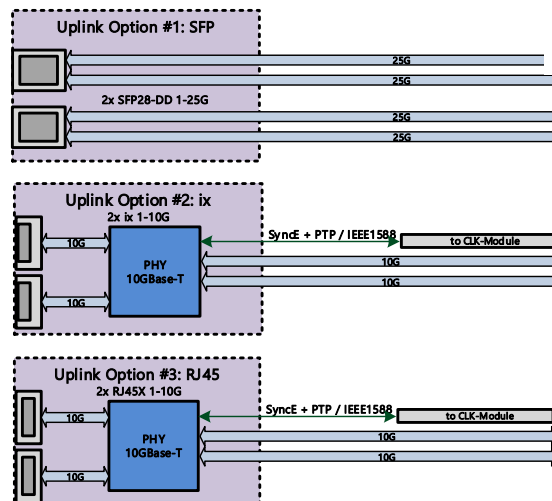
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## Base Board Uplink three choices

- Option #1: **SFP(-DD)**
  - 1-25G
  - Optical / Copper via SFP
- Option #2: **ix**
  - 1-10G (10GBASE-T)
  - Copper
- Option #3: **RJ45**
  - 1-10G (10GBASE-T)
  - Copper



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# NAT-MCH Gen4

## Clock Module

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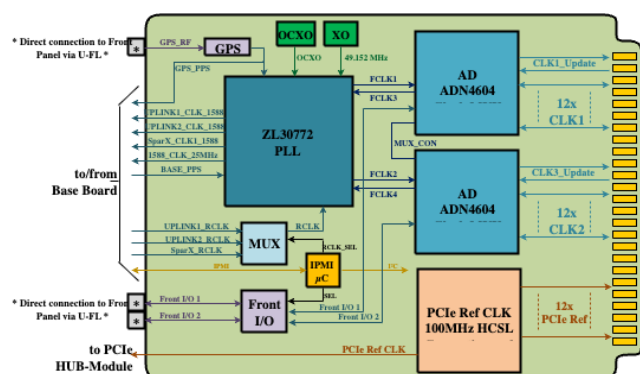
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## Clock Module

- PLL synthesizer and dedicated FPGA

- several options of switching
- Several option for clock manipulation
  - IEEE 1588 Support
  - Synchronous Ethernet Support
  - 2 low-Jitter Clock mux offer CLK1 + CLK2
  - 3<sup>rd</sup> mux for CLK3 or PCIe Reference Clock
  - GPS via SMA connector at front as option
  - Optional OCXO on Base Board



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# NAT-MCH Gen4

Fat Pipe Hub Modules

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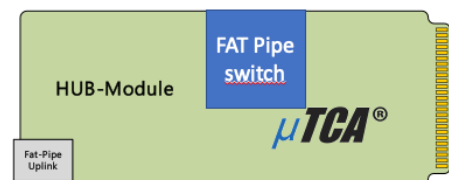
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## Fat pipe hubs

- HUB-EX (single-width)
  - 40/100GbE (still supporting XAUI)
  - Managed switch, Marvell Suite running on onboard CPU
  - QSFP-DD cage for uplinks up to 100GbE
- HUB-Px52 (single-width)
  - Microsemi PCIe gen4, 52 ports
  - QSFP cage for uplinks (x4)
- HUB-Px84 (double-width)
  - Microsemi PCIe gen5, 84 ports
  - QSFP-DD cage for uplinks (x8+x8 or x16)



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# NAT-MCH Gen4

Firmware

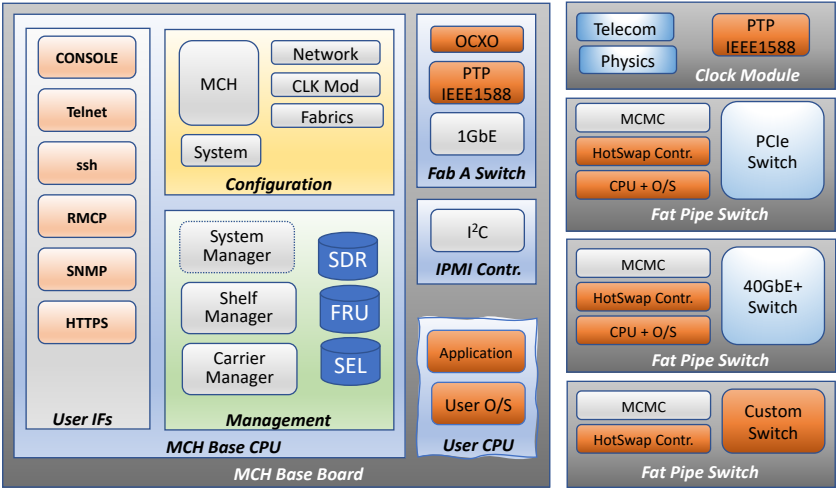
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## NAT-MCH Gen4 function blocks and compatibility



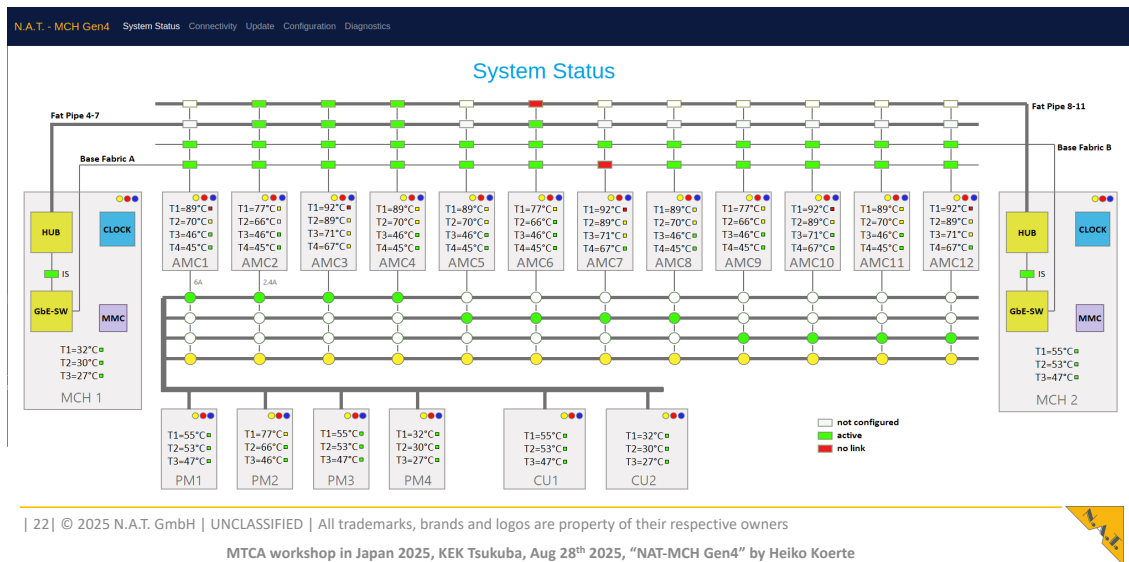
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## Software interfaces of Gen4 base board **web interface**



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## Software interfaces of Gen4 base board **overview**

- Improved software interfaces with Gen4 base board.
  - Webinterface with a new look
- Command Line Interface with new syntax
  - Currently a combination of CLI and interactive mode
    - fan\_ctl -> 3 -> 1 -> 4
    - show\_fruinfo 50
  - Shall be unified to keyword driven CLI like set, get, print
    - Syntax: <keyword><function><opt.sub function><fruId><opt.param>
      - set fan level 40 4
      - get fan level 40 -> nat> 4
      - print fruinfo 50



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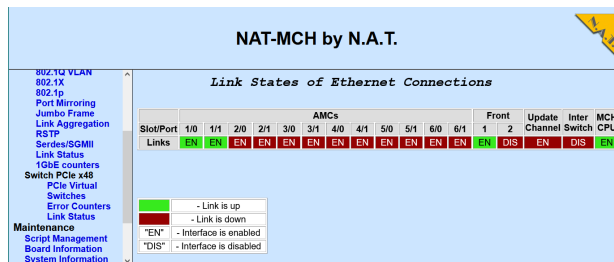
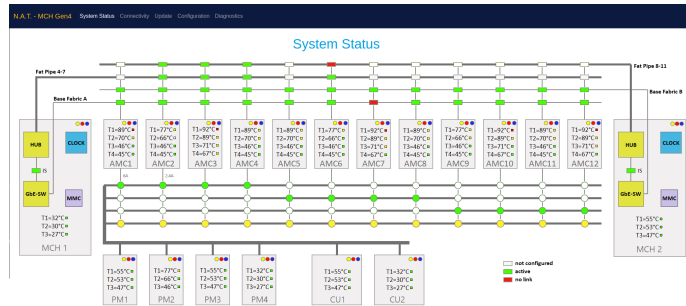
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```
nat> print sensorinfo 5
```

Sensor Information for FRU 5 / AMC1

#	SDRType	Sensor Entity	Inst	Value	State	Name
-	MDevLoc	0xc1	0x61			NAMC-ZYNQUP-FMC
1	Compact	0xf2	0xc1	0x01		HotSwap
2	Full	Voltage	0xc1	0x61	12.361 V	ok
3	Full	Voltage	0xc1	0x61	3.870 V	ok
4	Full	Voltage	0xc1	0x61	3.359 V	ok
5	Full	Voltage	0xc1	0x61	3.345 V	ok
6	Full	Voltage	0xc1	0x61	3.303 V	ok
7	Full	Voltage	0xc1	0x61	2.497 V	ok
8	Full	Voltage	0xc1	0x61	1.802 V	ok
9	Full	Voltage	0xc1	0x61	1.794 V	ok

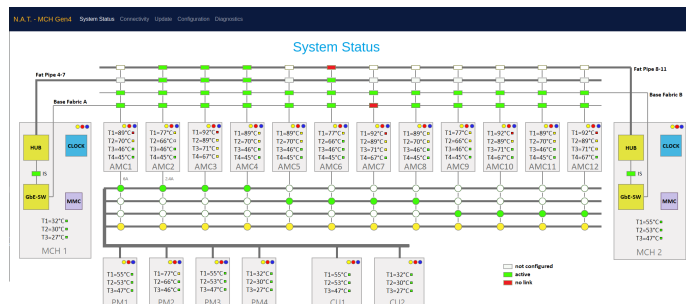
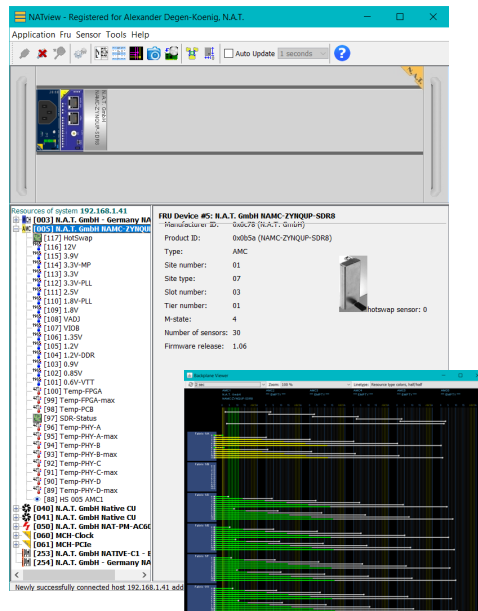


- combine web interface and CLI:
  - print fru , print fruinfo 5
  - print linkstate , print ports
  - print sensorinfo 5

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- combine web interface and NATview:
  - backplane viewer
  - sensor readings
  - real-time link state
  - (NATview will remain)

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## Mongoose web server – by Cesanta Software Ltd.

- small footprint cross-platform embedded web server
  - for Linux, Windows, FreeRTOS ...and generally easy portable
  - for every BSD API network stack e.g. LwIP, FreeRTOS-Plus-TCP
- extensively tested
  - 18 years on the market – 100M+ devices deployed
  - used by hundreds of businesses
- secure and up-to-date
  - continuous integration test powered by GitHub
  - Google's oss-fuzz scans for potential vulnerabilities
  - periodic vulnerability reports from groups like Cisco, Microsoft, NASA
- feature rich
  - Plain TCP/UDP, HTTP, MQTT, Websockets, SSL/TLS by mbedTLS or OpenSSL

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## Summary

- Why NAT-MCH Gen4?
  - New functions and requirements
  - MTCA.0 Rev 3
  - Upcoming component obsolescence with NAT-MCH Gen3
  - NAT-MCH Gen3 will reach EOL soon, LTB in 2025 and LTS in 2025/2026
- How to migrate and when?
  - NAT-MCH Gen4 is a full form, fit and function replacement for NAT-MCH Gen3
  - Migration is expected to be smooth and easy
  - Customers may encounter minor changes in CLI when using shell scripts
  - Customers started migrating already
  - Migration is expected to be finished 2025

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Thank you very much!

**Heiko Körte**  
Director Sales & Marketing  
heiko.koerte@nateurope.com



N.A.T. GmbH  
Konrad-Zuse-Platz 9  
53227 Bonn  
Germany

[www.nateurope.com](http://www.nateurope.com)

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## PICMG – Next Generation MicroTCA

- New PICMG work group “Next Generation MicroTCA”

- Since end of 2019
- Members represent
  - Manufacturers
    - Chassis (incl. cooling and backplane)
    - Power Modules
    - MCHs
    - AMCs
    - Mechanical components such as connectors
    - Semiconductors
  - Users



**μTCA®**

**AdvancedMC™**

- Goal
  - Improve MicroTCA so that it can meet the requirements for the **next 10-15 years**
  - Keep next generation of MicroTCA backward compatible
- Intermediate step
  - MicroTCA v3 adopted in December, 2023
- Next Step: Next Generation spec.

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