Digitizers

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TELEDYNE SP DEVICES
Everywhereyoulook™

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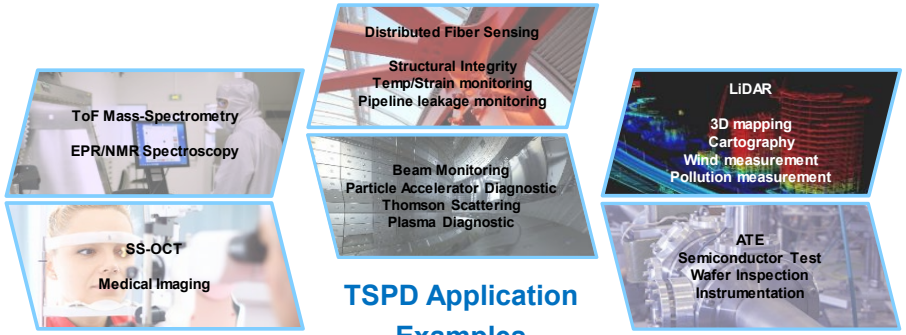
Agenda

- Company Introduction
- Product Overview and Specification
- Multi-Channel Acquisition
- Application Specific Firmware
  - FWPD : Pulse Detection
  - FWATD : Waveform Accumulation(Averaging)
  - FW2DDC : Digital Down Converter (Mixer)
  - DEVDAQ, DEV8DAQ : Development Kit

TSPD has been designing and manufacturing High-Performance Digitizers for over ~20yeas

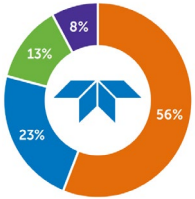
- High sampling rate (GSps) and high resolution (10-14b)
- Onboard pre-processing by Open field-programmable gate array (FPGA)
- Offboard high data throughput to host PC
- Peer-to-peer streaming to graphics processing unit (GPU)
- System design services for resource optimization



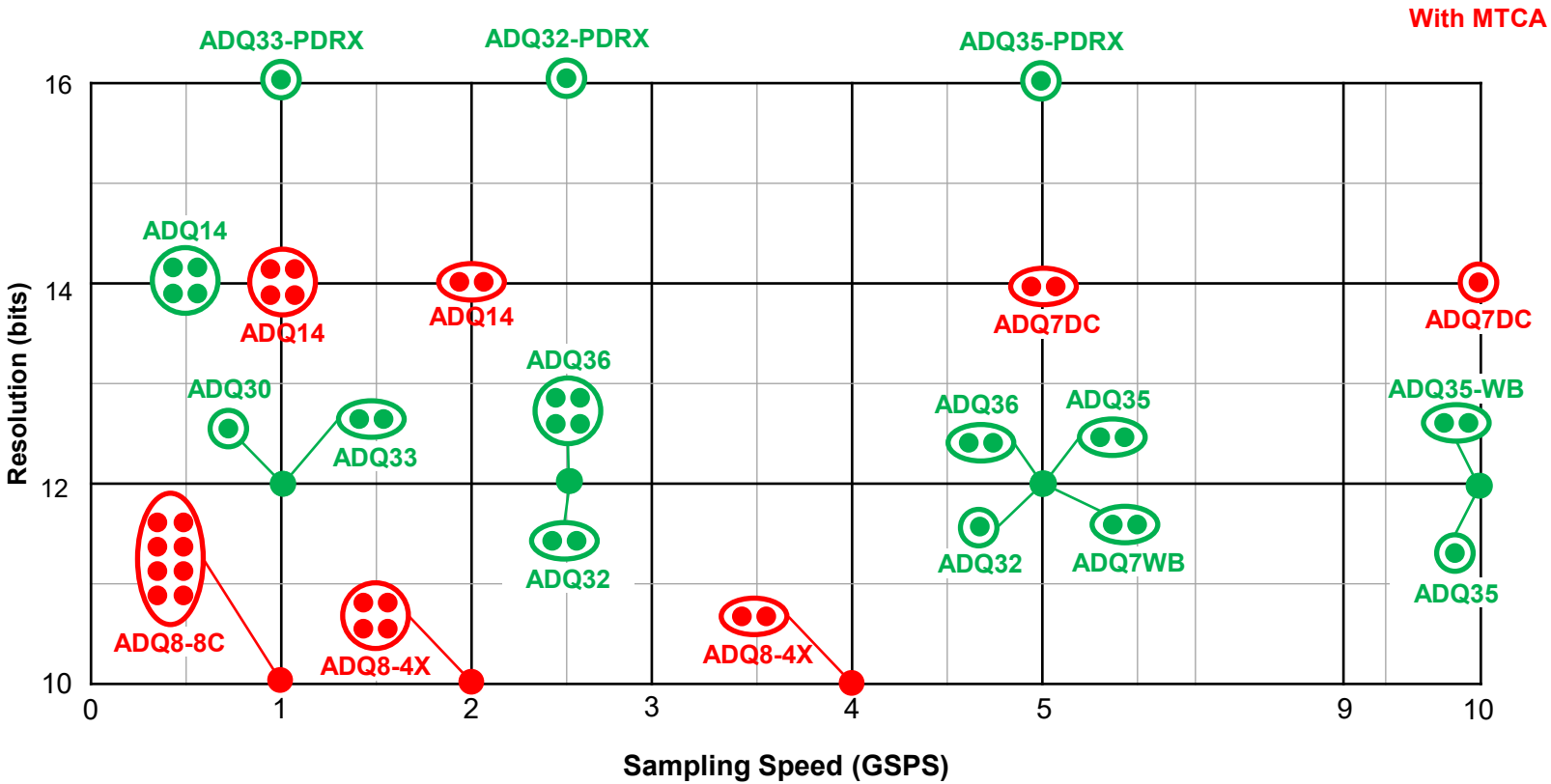
TSPD Application Examples

TELEDYNE TECHNOLOGIES

- 5.64 billion USD in net sales (2023 annual report)
- Over 15,000 employees
- More than 70 office locations worldwide
- TSPD is a part of Teledyne Technologies and in Instrumentation segment



Product Overview



MTCA Product Specification

Device	Res	Ch	Sample Rate (GSPS)	Input Range	Input Bandwidth (GHz)	MTCA Datarate (Sustained)	Firmware	Notes
ADQ7DC	14	2, 1	5.0, 10.0	1.0Vpp	DC to 3.0	3.4 GB/s (Gen3)	FWATD, FWPD, FW2DDC, DEVDAQ	EPICS support
ADQ14DC (4C, 2X)	14	4(4C) 2(2X)	1.0(4C) 2.0(2X)	0.5Vpp (4C) 1.0Vpp (2X)	DC to 0.7(4C), 1.2(2X)	1.6 GB/s (Gen2)	FWATD, FWPD, DEVDAQ	EPICS support, No VG option, GPIO option as default
ADQ08-8C	10	8	1.0	0.25Vpp to 5Vpp programmable	DC to 0.5	1.3 GB/s (Gen2)	DEV8DAQ	Daisy Chain Trigger support
ADQ08-4X	10	4, 2	2.0, 4.0	0.25Vpp to 5Vpp programmable	DC to 1.0	1.3 GB/s (Gen2)	DEV8DAQ	Daisy Chain Trigger support

ADQ7DC-MTCA

ADQ14-4C-MTCA

ADQ8-8C-MTCA

<Firmware>

DEVDAQ, DEV8DAQ :
Development Kit for customers to implement their own logic.
AMD Synthesis tool is necessary.

FWATD : Waveform Accumulation

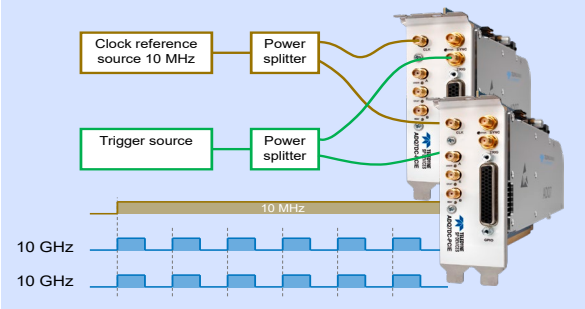
FTPD : Pulse Detection

FW2DDC :
Digital Down Convert

Multi-Channel Acquisition

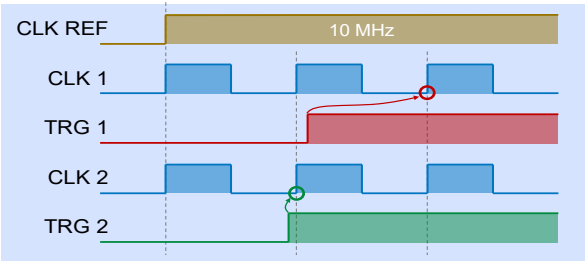
Consideration1: Sampling alignment over multiple digitizers

Use Common 10MHz external clock(backplane or front panel) for sampling alignment across all digitizers. Jitter cleaner PLL available for approximately 200 fs jitter.

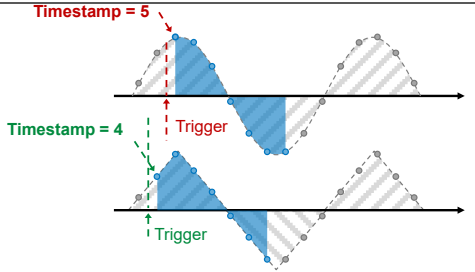


Consideration2: Trigger Jitter

Record start timing could differ over multiple digitizers due to trigger jitter



Solutions for Trigger Jitter

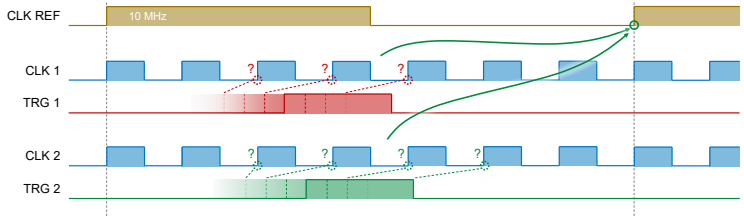


C2_s1:
Correction of record start by Timestamp

Timestamp can be utilized to identify and correct differences in record start times across multiple digitizers.

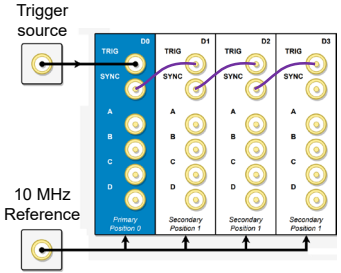
C2_s2:
Phase-locked Trigger

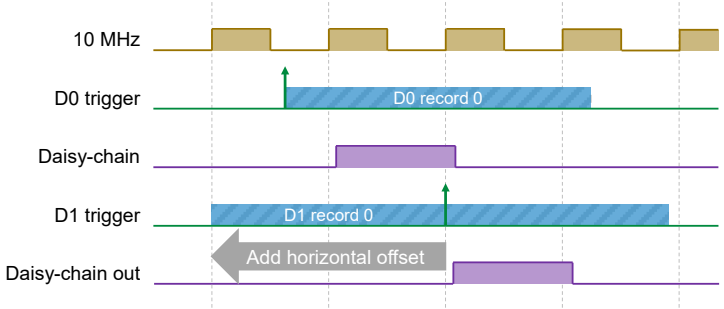
External trigger source uses 10MHz digitizer reference clock. Digitizers synchronize the trigger with 10MHz reference clock.



C2_s3:
Daisy Chain trigger

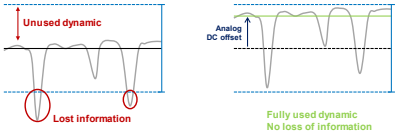
Connect the trigger in a daisy chain





Application Specific Firmware : FWPD (Pulse Detection)

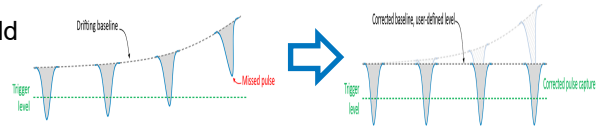
DC Offset
- Programmable DC offset allows unipolar signals to utilize the entire input range of the digitizer



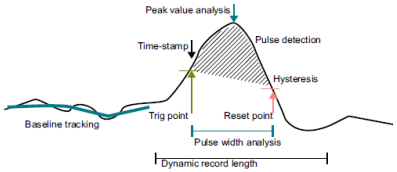
Doubling dynamic range for uni-polar pulses

DBS & MA
- DBS tracks baseline fluctuations, adjusts the baseline to a user-defined target value, and suppresses pattern noise. For rapid baseline change, MA(Moving Average) is available.

Baseline is reference for threshold & trigger and needs to be stable



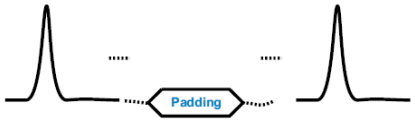
Peak Detection & Analysis
- Detect the pulse and calculate leading and training edges
- Analyze meta data(a pulse for peak value, pulse width and timing)



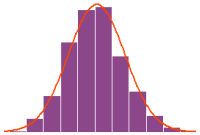
Meta data allows large reduction in amount of data to be transferred to Host, hence high throughput

Data collection & Latency Control
- Make records of data and control latency to get a minimum throughput with dummy data

Small amount of data stays in buffer for long, and padding flushes data to Host with certain minimum latency



Histogram
- Generate histogram of peak value and pulse width



Histogram result is read out by ADQAPI

Example) ADQ7DC : 14bit, 10GSPS, ~430msec time period for monitoring, Ave pulse rate 600Mpulses/sec

Application Specific Firmware : FWATD (Advanced Time Domain)

DC Offset
- Programmable DC offset allows unipolar signals to utilize the entire input range of the digitizer

DBS
- DBS tracks baseline fluctuations, adjusts the baseline to a user-defined target value, and suppresses pattern noise

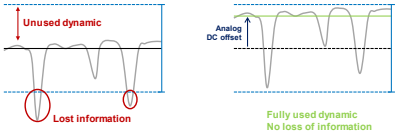
Data Path Filter
- A frequency-selective digital filter helps reduce noise for input signals with known limited bandwidth without loss of signal information

Threshold Operation
- The non-linear advanced threshold operation with filter is a complement to the succeeding WFA, tailored for rarely occurring weak pulses

WFA
- Waveform averaging **(WFA)** reduces random noise via repeated measurements

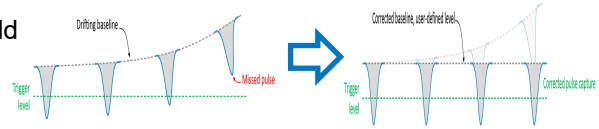
Seamless Acquisition
- Dead-time free **seamless** accumulation and acquisition

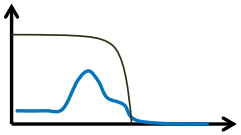
Example) ADQ7DC : 14bit, 10GSPS, ~2.1Msamples/record, ~262K waveform accumulation, dead time 32nsec



Doubling dynamic range for uni-polar pulses

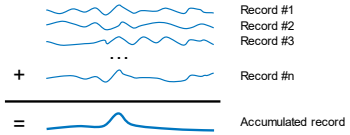
Baseline is reference for threshold & trigger and needs to be stable





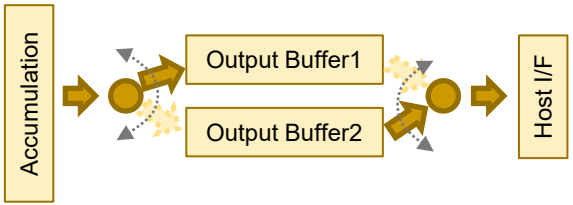
FIR digital filter reduces noise power outside of the frequency band of interest

Remove out noise under threshold



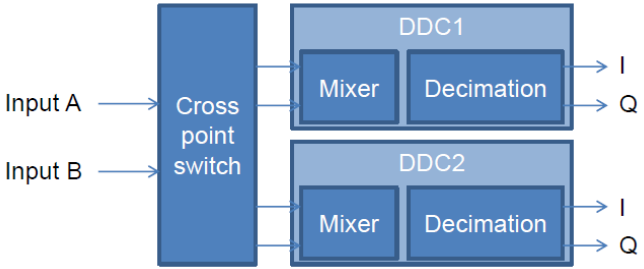
ADQ7DC : 2Msamples/record, accum count 18bit
ADQ14 : 2Msamples/record, accum count 16bit

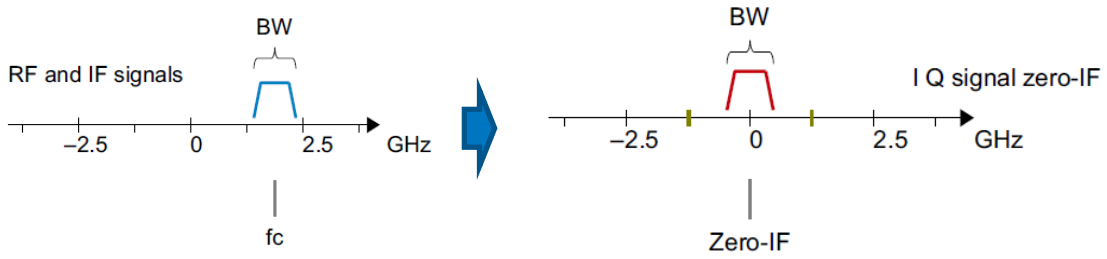
Double Buffer allows seamless accumulation and data transfer

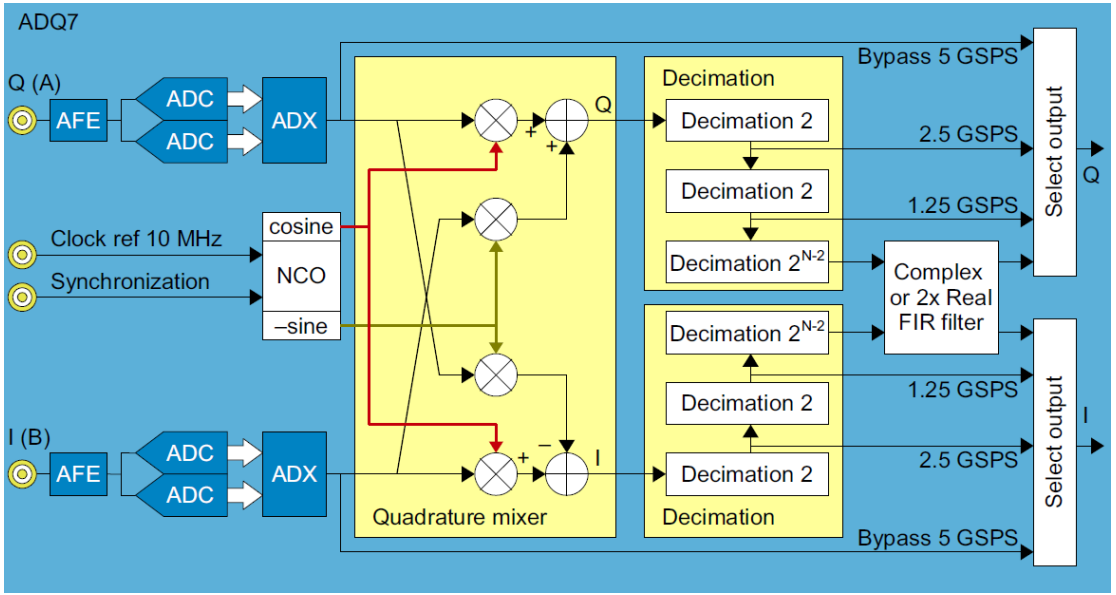


Application Specific Firmware : Digital Down Converter (FW2DDC)

- Frequency down conversion by Numerical Controlled Oscillator(NCO) and DDC (Digital Mixer)
- Built-in decimation to reduce data
- Support multiple input modes
  - One IQ Input
  - Two Real Inputs
  - One Differential Input

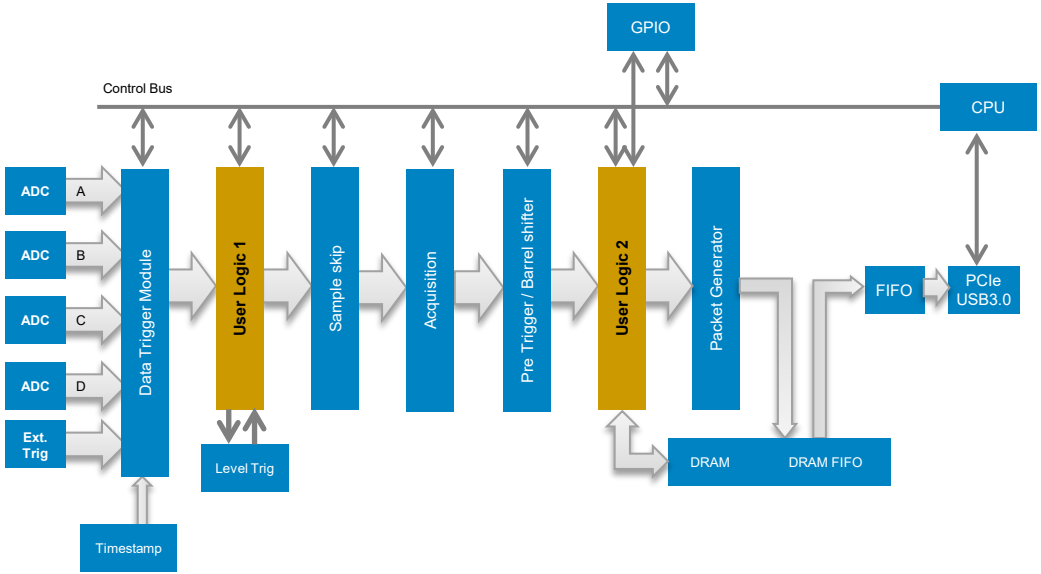


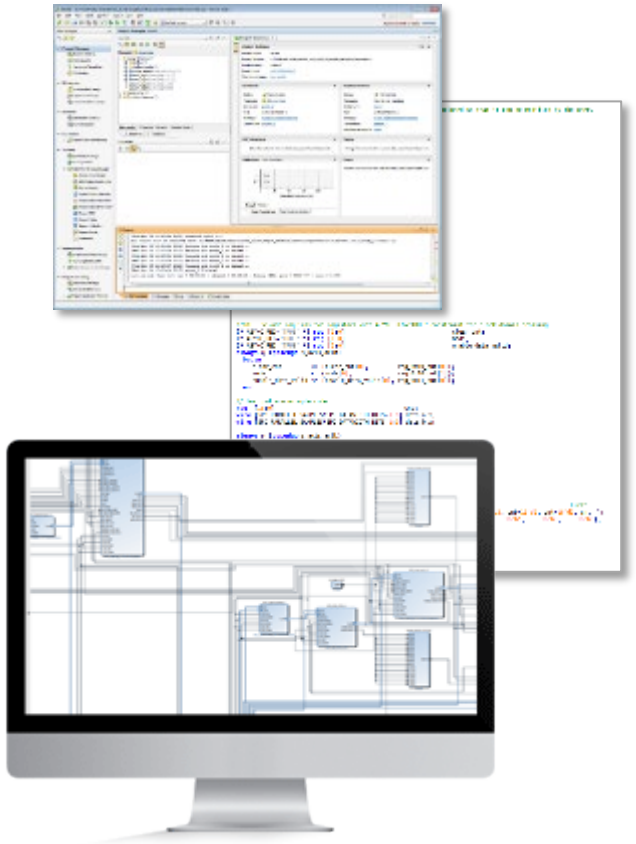




FPGA Development kit(DEVDAQ, DEV8DAQ)

- "User Logic1" sees all data stream, and "User Logic2" sees only triggered records.
- With those two blocks, customers can focus on their algorithm





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