MTCA workshop for accelerator and physics in Japan 2025

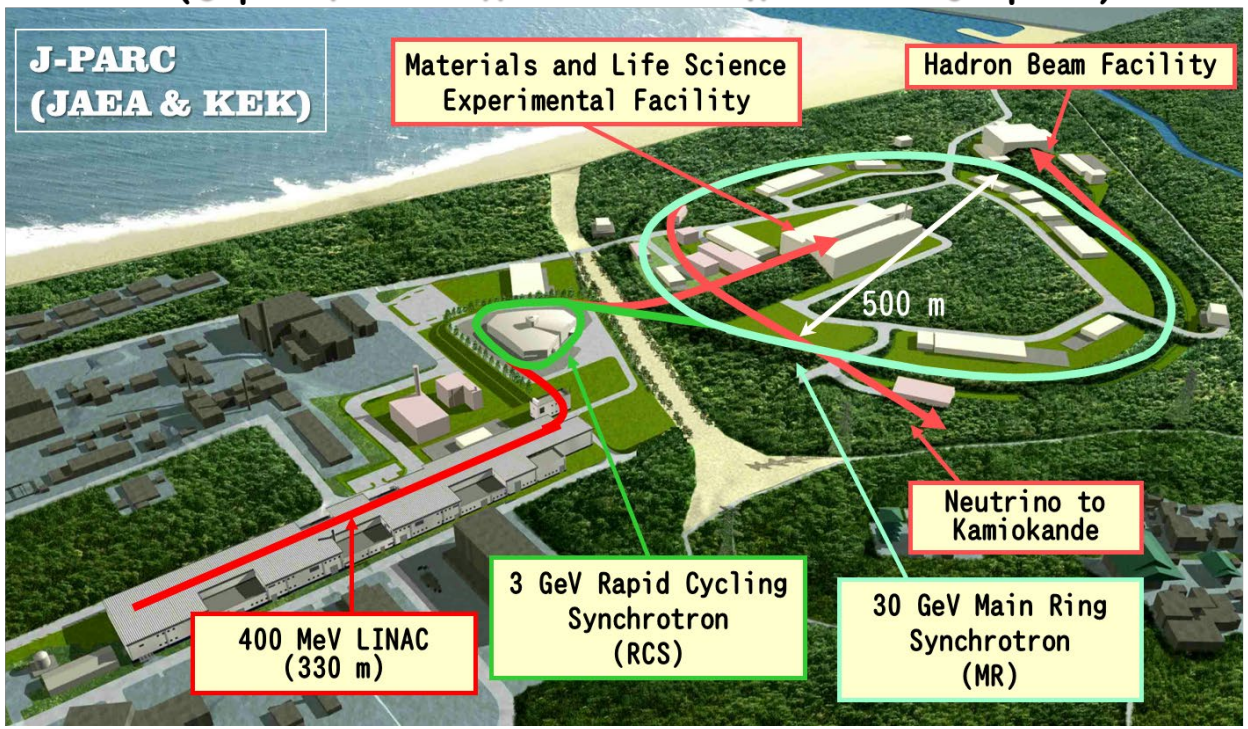
DFB&FF System based on MTCA @ J-PARC LINAC LLRF

High Energy Accelerator Research Organization (KEK),
Kenta Futatsukawa
and J-PARC LLRF Gr.

Aug. 27－29, 2025, KEK Tsukuba Campus

J-PARC & J-PARC LINAC

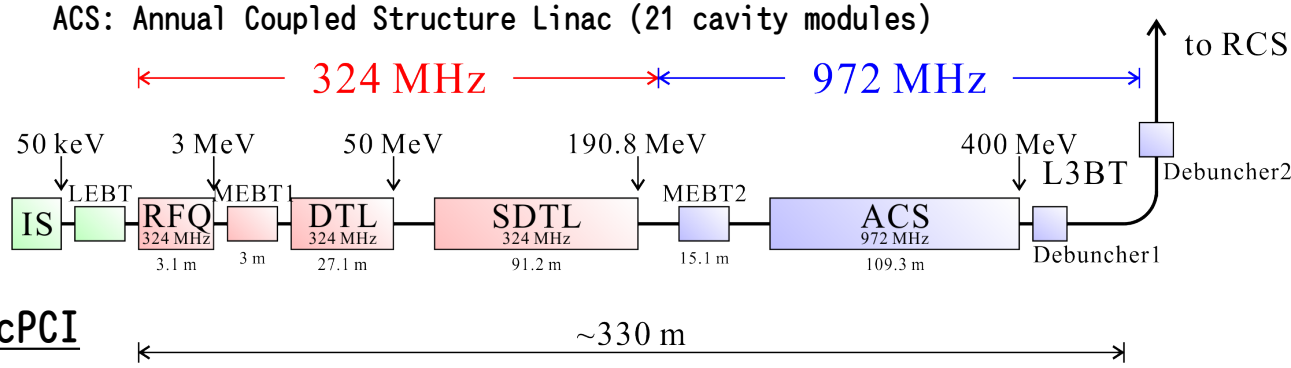
J-PARC (Japan Proton Accelerator Research Complex)



J-PARC Linac

- Particles: H^- (negative hydrogen)
- Kinetic Energy: 400 MeV
- Peak Current: 50 mA
- Acceleration Frequency: 324 MHz (24) + 972 MHz (25)
- Pulse Width: 500 μs (Beam), 650 μs (RF)
- Repetition: 25Hz

IS: H^- Ion Source
RFQ: Radio Frequency Quadrupole Linac
DTL: Drift Tube Linac (3 cavity modules)
SDTL: Separate-type Drift Tube Linac (16 cavity modules)
ACS: Annual Coupled Structure Linac (21 cavity modules)



Digital Feedback & Feedfoward (DFB&FF) system based on cPCI
Development: ~~~early 2000s~~1999~.
Start of J-PARC Linac operation: Oct. 2006
Start of J-PARC user operation: Dec. 2008

Required Gradient Stability : ±1% in amplitude, ±1 deg. in phase
→ DFB : ±0.3% in amplitude, ±0.3 deg. in phase
→ Beam Loading Compensation System : ±0.3% in amplitude, ±0.3 deg. in phase
→ Reference Distribution System : ±0.3 deg. in phase

DFB&FF System @J-PARC LINAC

Previous System:

cPCI boards for DFB/DFF

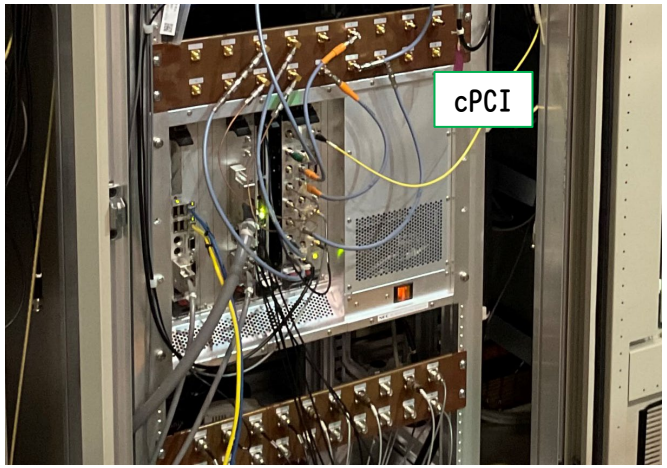
- ✓ FPGA board: discontinued
- ✓ DSP board: discontinued
- ✓ CPU board: discontinued
- ✓ RF&CLK board: discontinued

development environment

- ✓ FPGA: Xilinx ISE Ver 6.2i
- ✓ DSP: TI Code Composer Studio Ver 2.1
- ✓ host program: Redhat 8.0 gcc compiler Ver 3.2
- ✓ application: python 2.4/wxPython 2.6

→ We cannot keep the development environment.

→ We gave up on updating the FPGA logic modification.



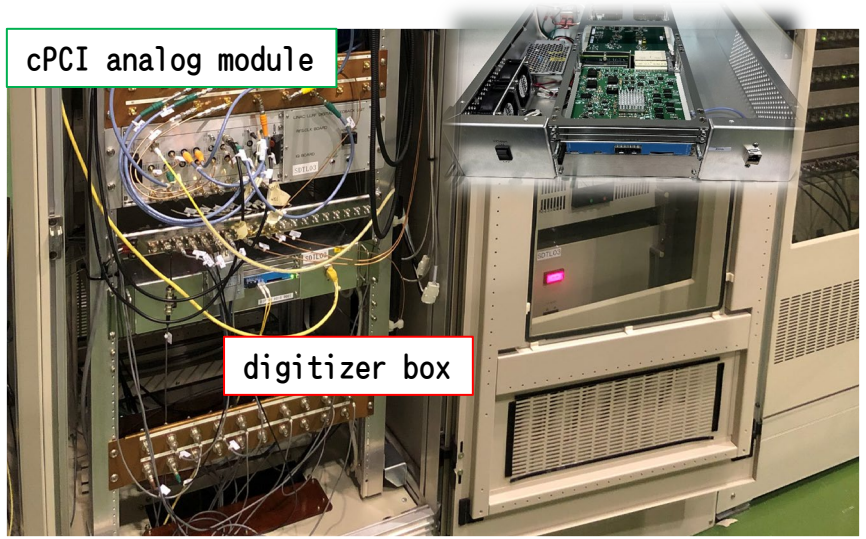
digitizer box (MEDS):

A/D-D/A signal processing MTCA.4 based AMC board

- ✓ platform: MTCA.4 AMC
- ✓ FPGA: Zynq XC7Z045-1FFG900C, QSPI FLASH-ROM 16MB, SD-card Remote Update
- ✓ RAM: DDR3-SDRAM 1GB×2 (PL, PS)
- ✓ OS: Xilinx Linux (EPICS-IOC)
- ✓ ADC: 8ch 16bit 370MSPS(max.), BW: 800MHz
- ✓ DAC: 2ch 16bit 500MSPS
- ✓ SFP: 2ports

MTCA.4 based RTM board:

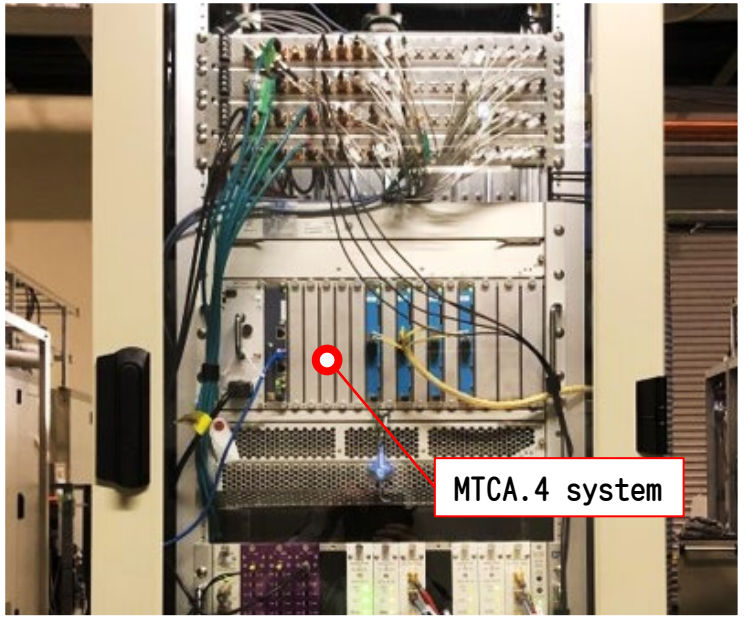
- ✓ clock generation (120 MHz, 240 MHz)
- ✓ level conversion



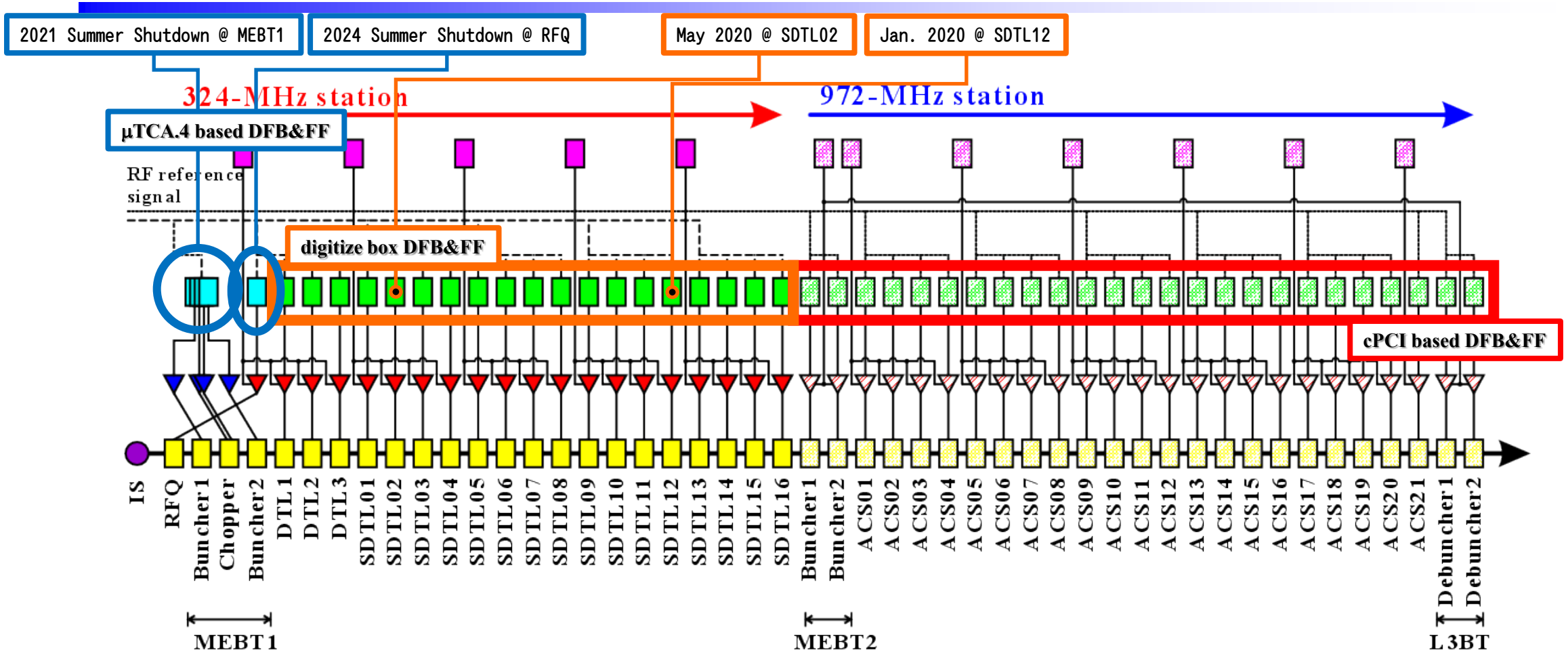
MTCA.4 w RF backplane (MEDS):

- AMC: A/D-D/A signal processing
  → same as the digitizer box
- MRTM: 8-ch down-converter, IQ modulator
- eRTM: clock generator (312 MHz, 324 MHz, 120 MHz, 240 MHz, 12 MHz), distribution
  → manufactured by CANDOX

no communication between boards



Cavity & RF Status @J-PARC LINAC

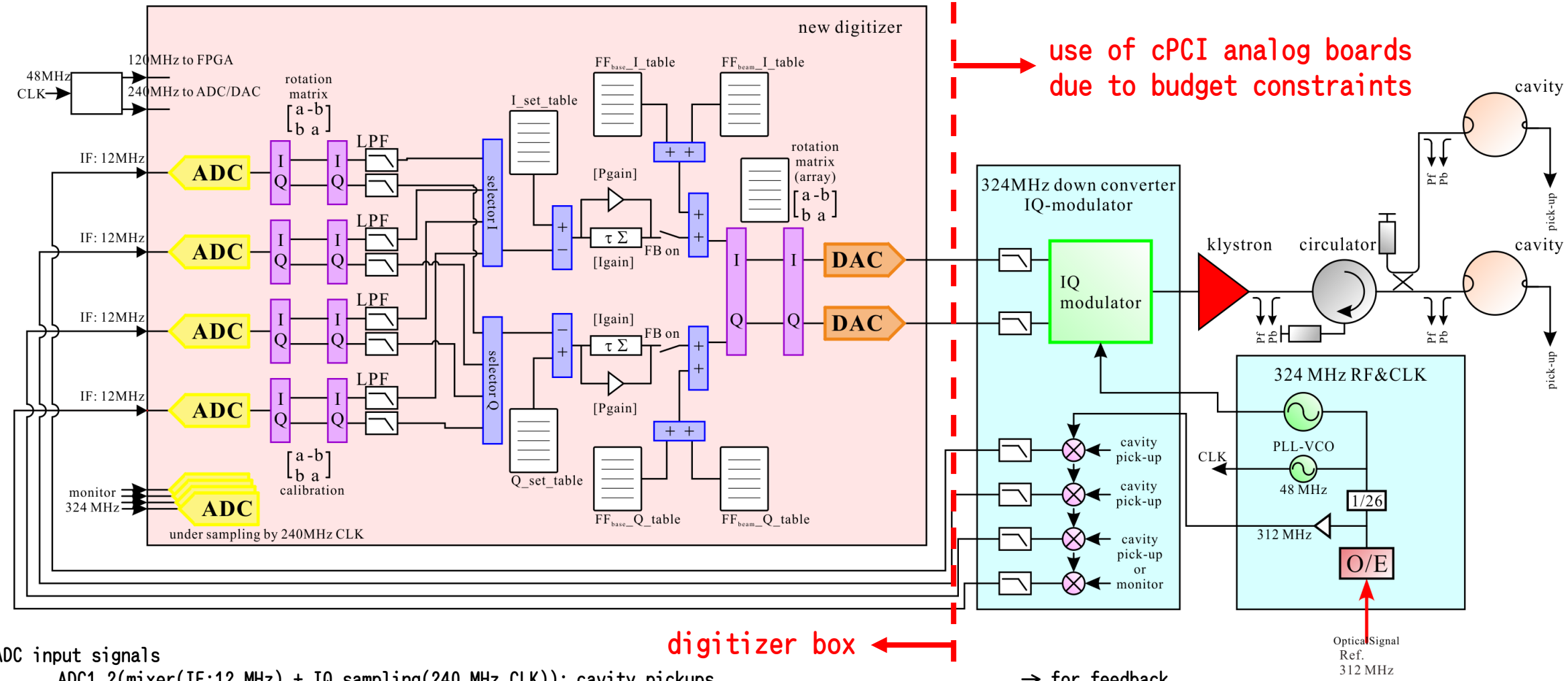


#components	HVDC PS	LLRF(DFB and DFF)	RF source	cavity station
324 MHz	5	5(μTCA.4) 19(digitizer box)	20(klystron) 4(SSA)	24
972 MHz	7	25(cPCI)	25(klystron)	25

2021 Summer Shutdown @ RFQ, DTL1-2

2020 Summer Shutdown @ DTL3, SDTL01-16

DFB&FF System Using Digitizer Box

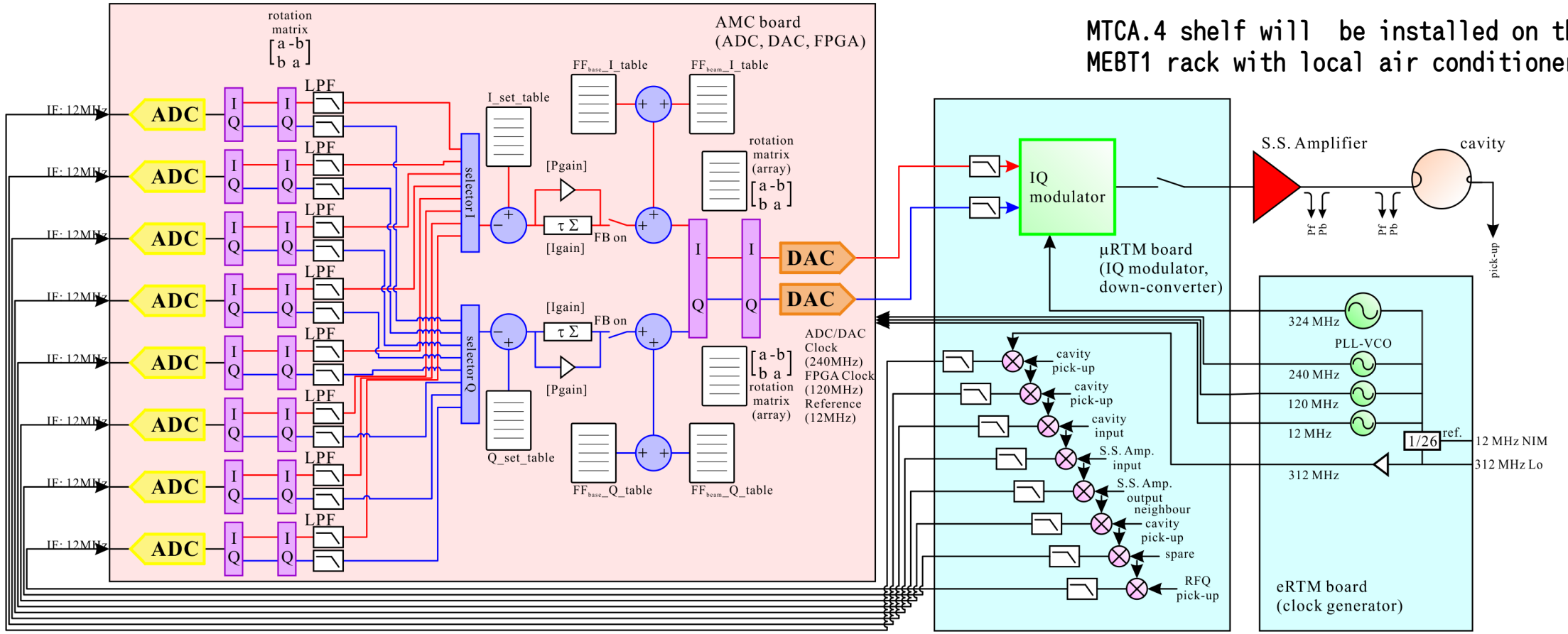


ADC input signals

ADC1,2(mixer(IF:12 MHz) + IQ sampling(240 MHz CLK)):	cavity pickups	→ for feedback
ADC3,4(mixer + IQ sampling):	cavity input (Pf)	
ADC5(direct sampling(240MHz CLK)):	klystron drive amplifier input	→ for drive amplifier gain calculation
ADC6(direct sampling):	klystron input (drive amplifier output)	→ for drive amplifier/klystron gain calculation
ADC7(direct sampling):	drive amplifier output	→ for klystron gain calculation
ADC8(direct sampling):	neighbor cavity pickup (ex. upstream cavity)	→ for phase drift check

DFB&FF System Using MTCA.4 Shelf

MTCA.4 shelf will be installed on the MEBT1 rack with local air conditioner.



ex) ADC input signals, Buncher1 @MEBT1

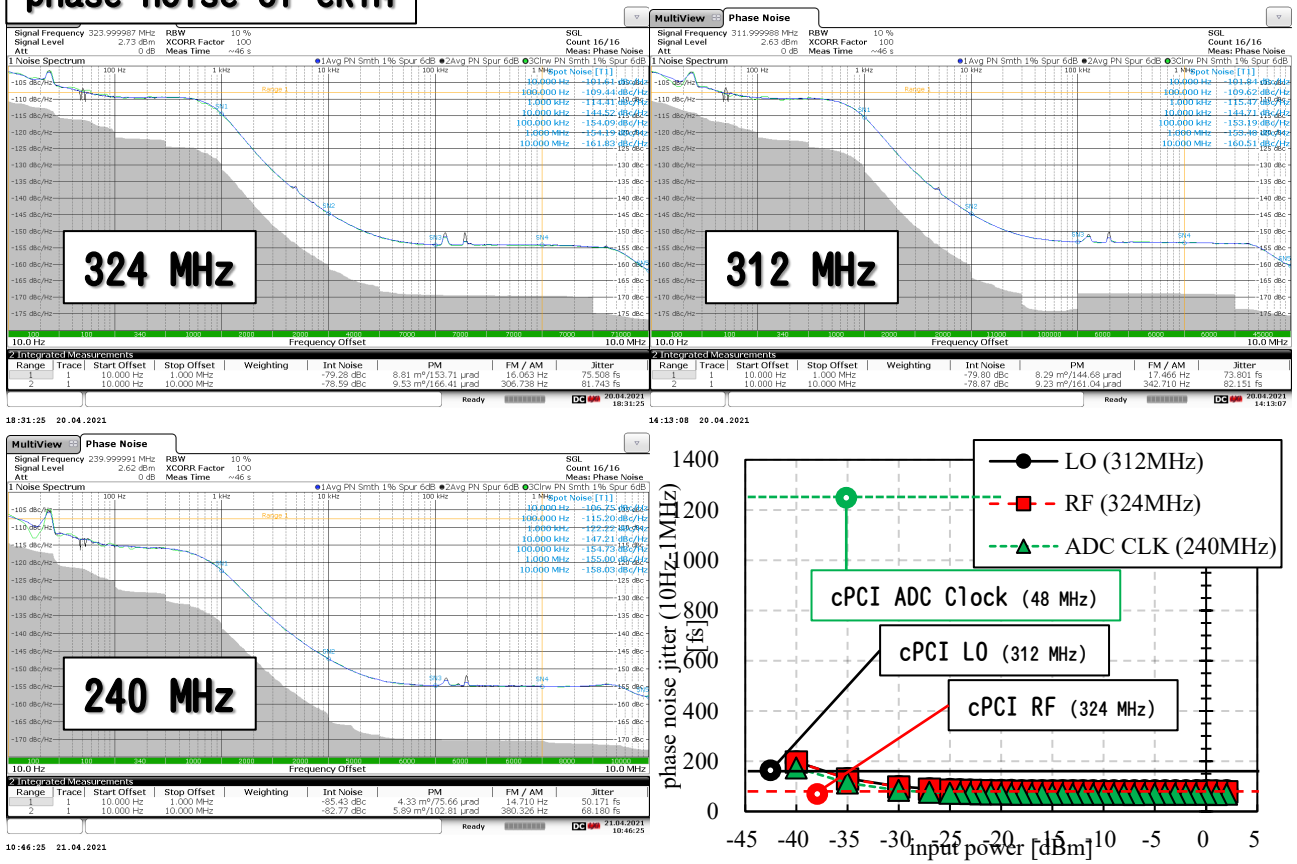
ADC1,2(mixer(IF:12 MHz) + IQ sampling(240 MHz CLK)):	cavity pickups	→ for feedback
ADC3(mixer + IQ sampling):	cavity input (Pf)	
ADC4(mixer + IQ sampling):	SSA input	→ for SSA gain calculation
ADC5(mixer + IQ sampling):	SSA output	→ for SSA gain calculation
ADC6(mixer + IQ sampling):	cavity input coupler (Pb)	
ADC7(mixer + IQ sampling):	Buncher2 pickup	→ for phase drift check/compensation
ADC8(mixer + IQ sampling):	RFQ pickup	→ for phase drift check/compensation

Performance of MRTM, eRTM Boards

Performance of eRTM, MRTM for J-PARC LINAC LLRF

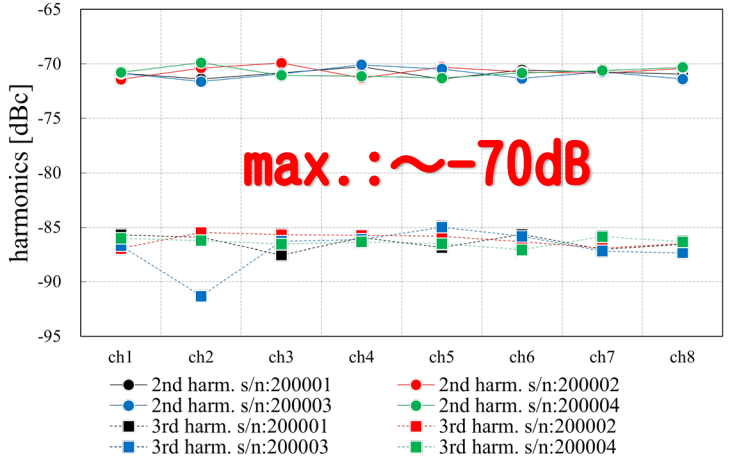
- ✓ phase noise of eRTM
- ✓ harmonics of IF outputs of MRTM
- ✓ cross-talk of MRTM

phase noise of eRTM



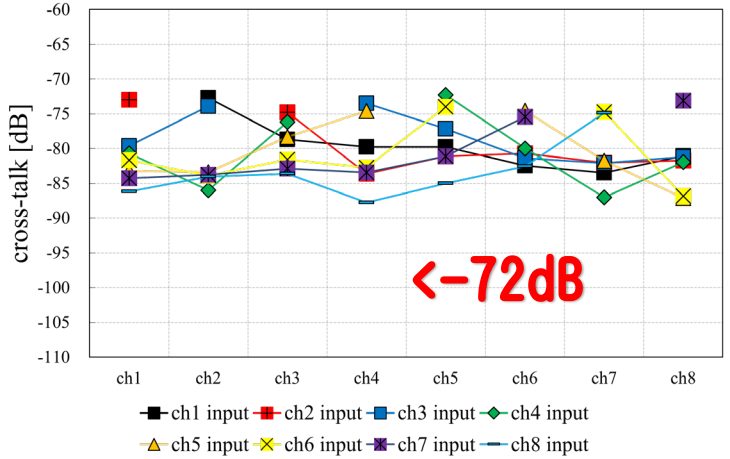
RF/LO phase noise: almost same as that cPCI RF&CLK board
ADC Clock phase noise: greatly improved

harmonics of IF outputs of MRTM



-70dB~0.031%: Neglective on our system

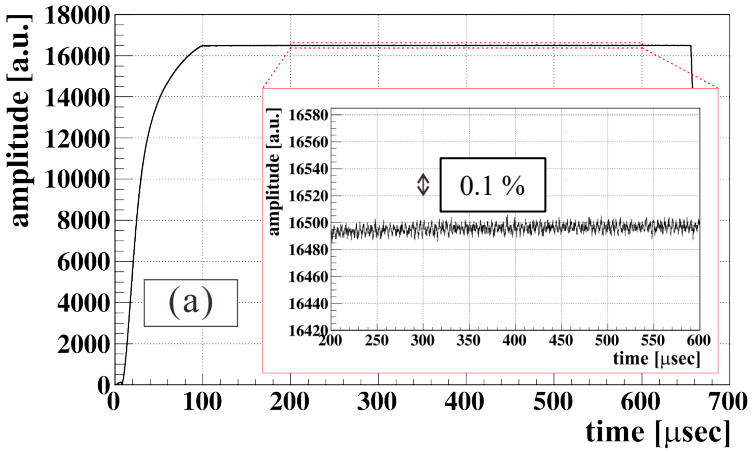
cross-talk



-72dB~0.025%: Neglective on our system

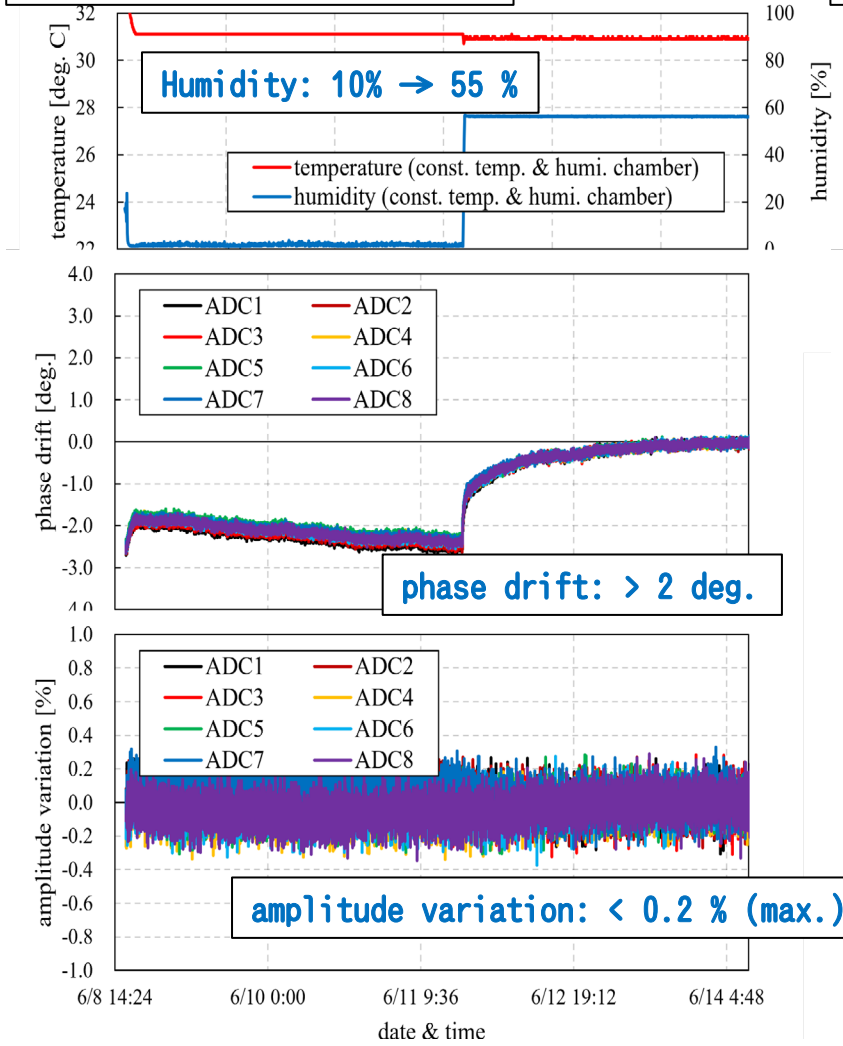
Stability of Amplitude and Phase

amplitude and phase stability @MEBT1 Buncher1

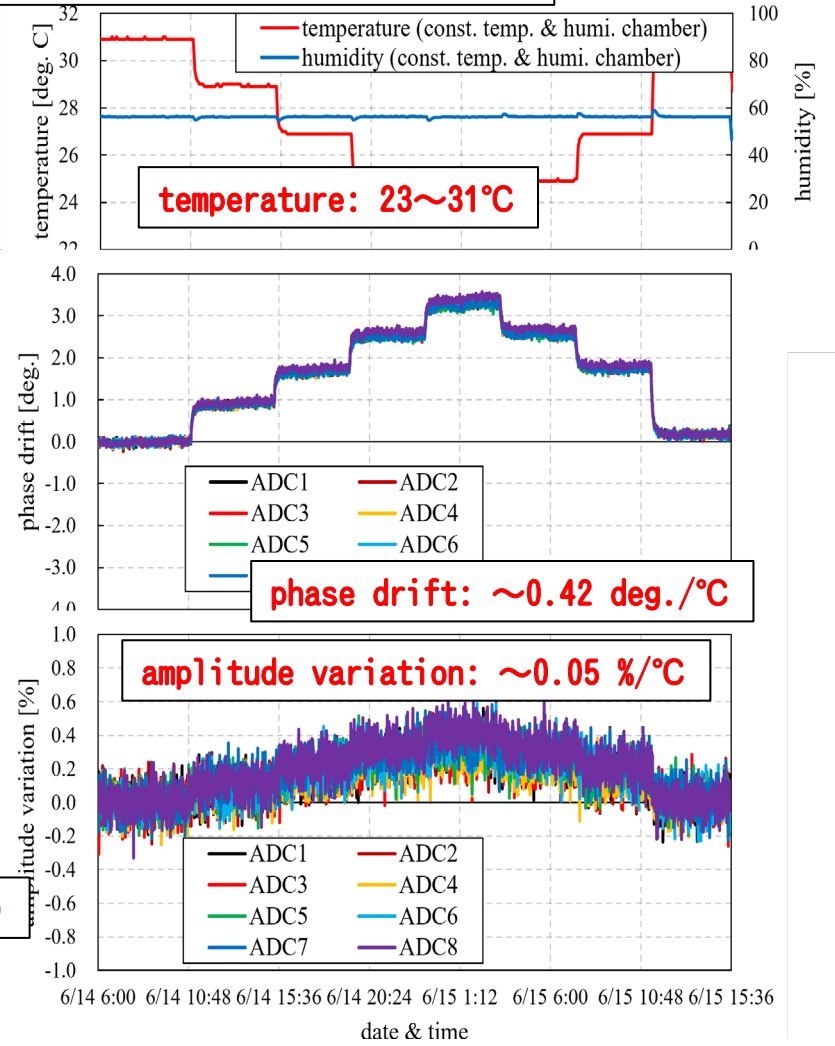


performance ～+/−0.1% in amplitude,
～+/−0.1 deg. in phase

humidity dependence test



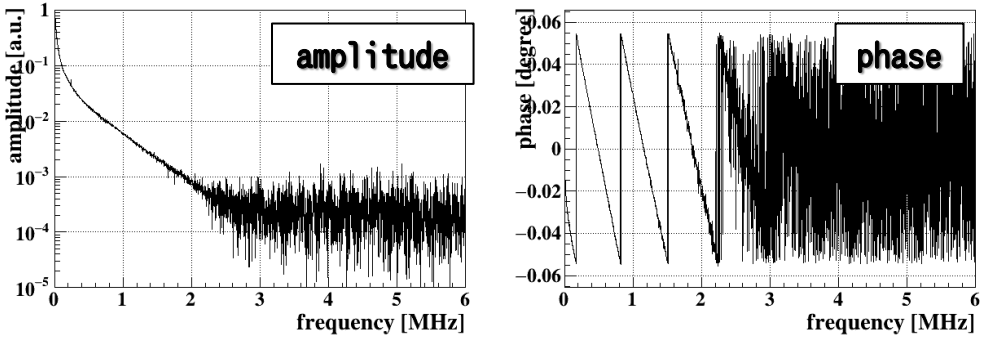
temperature dependence test



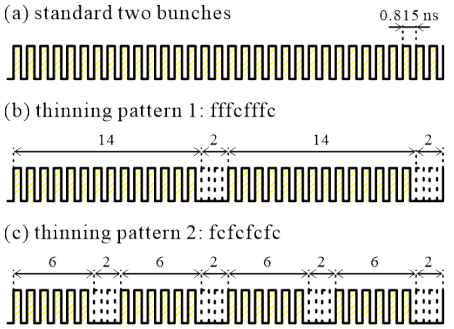
The substrate material (Ro4003C) was tested and sorted in advance, but good results were not obtained as a humidity characteristic test.

Beam Loading Compensation System

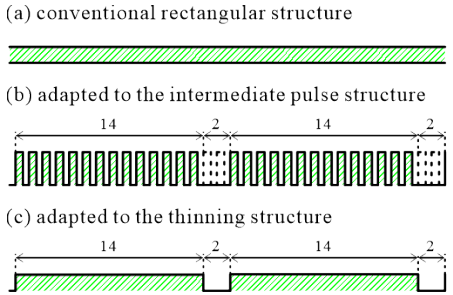
Obtained transfer function at SDTL01



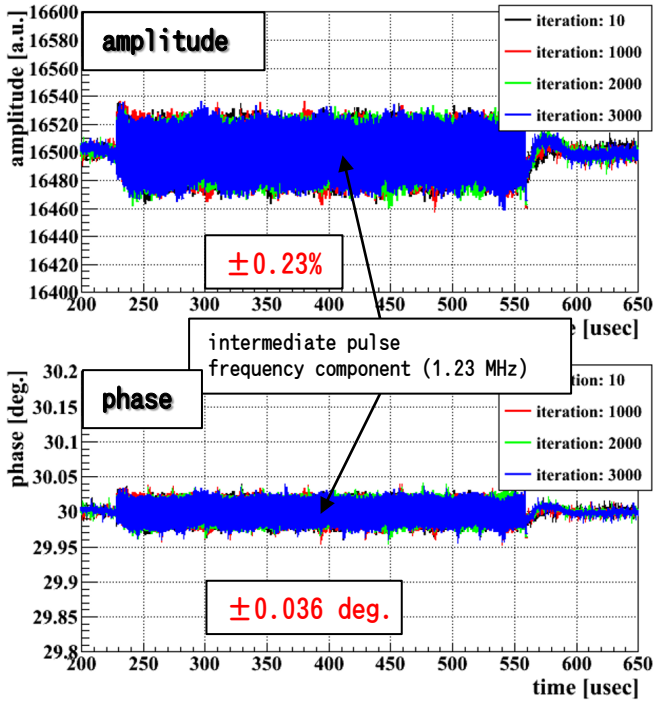
intermediate pulse



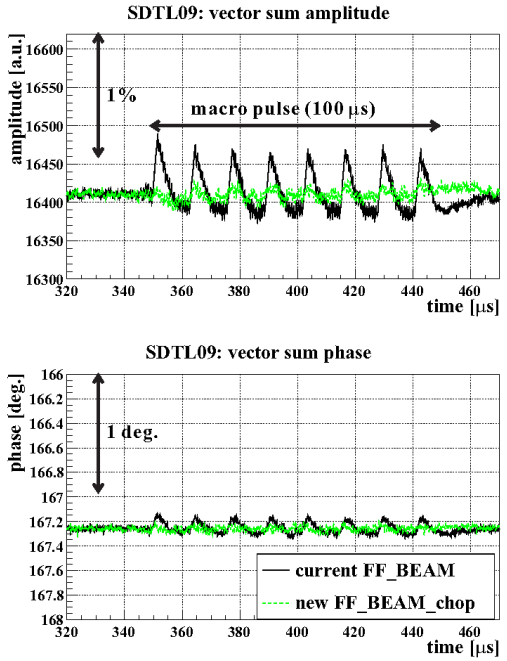
beam loading compensation



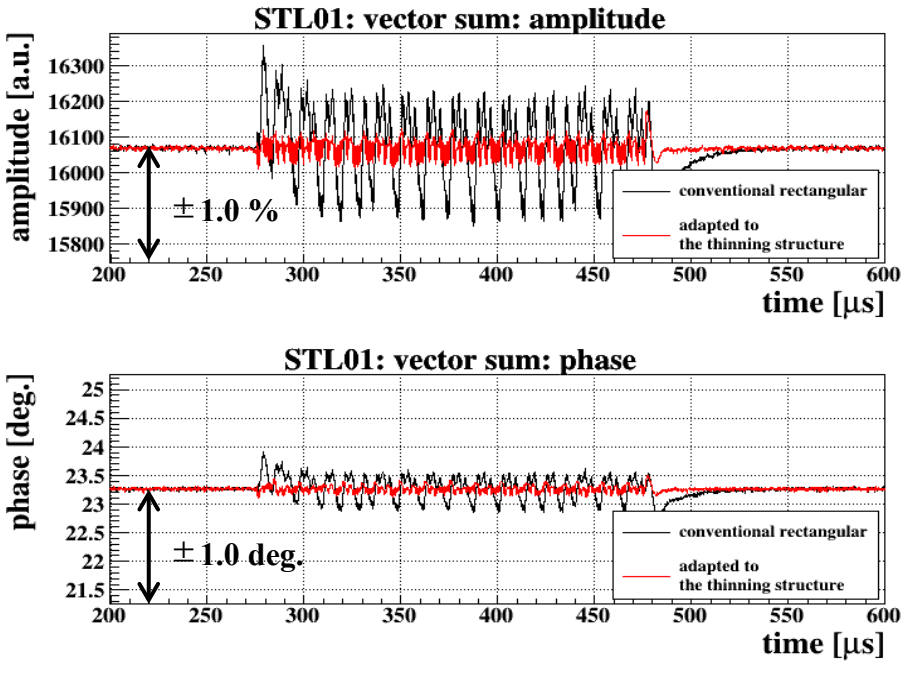
for standard two bunches @SDTL02



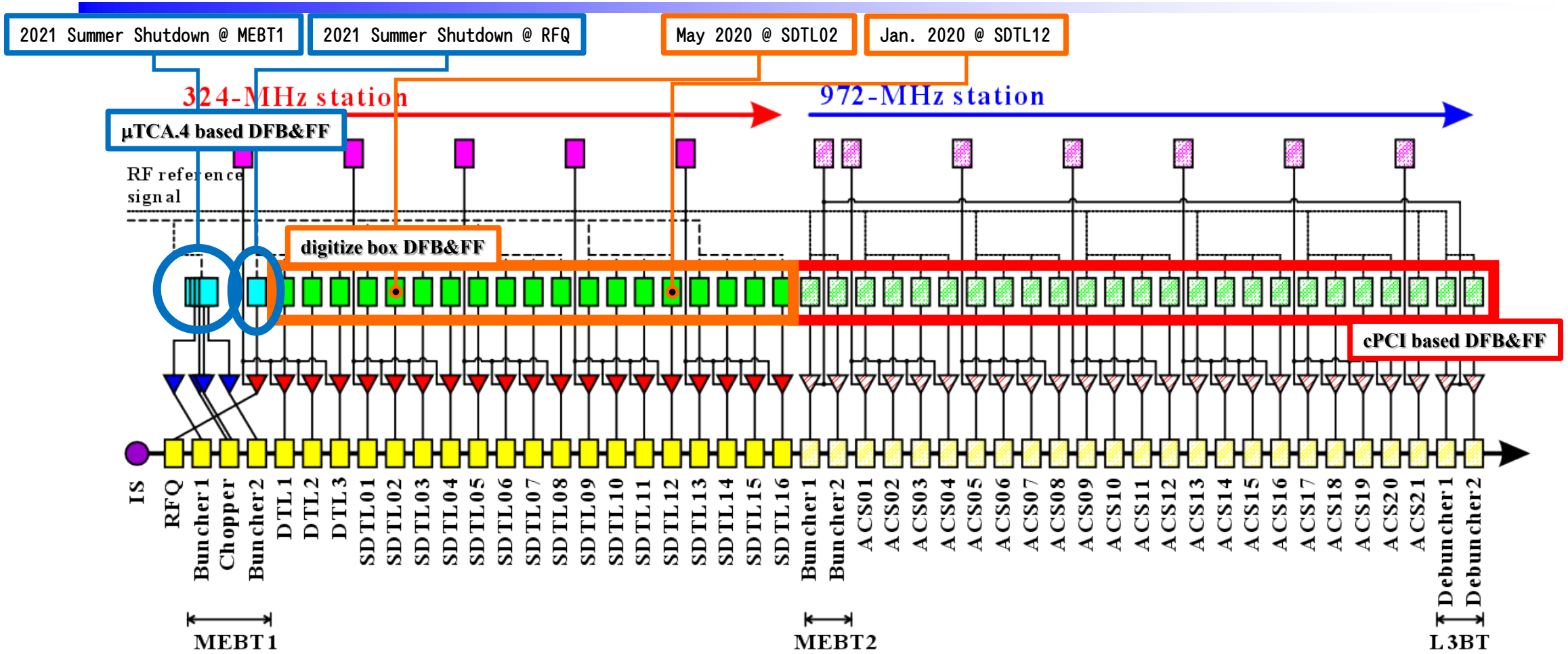
adapted to intermediate pulse @SDTL09



adapted to thinning structure @SDTL01



Cavity & RF Status @2025



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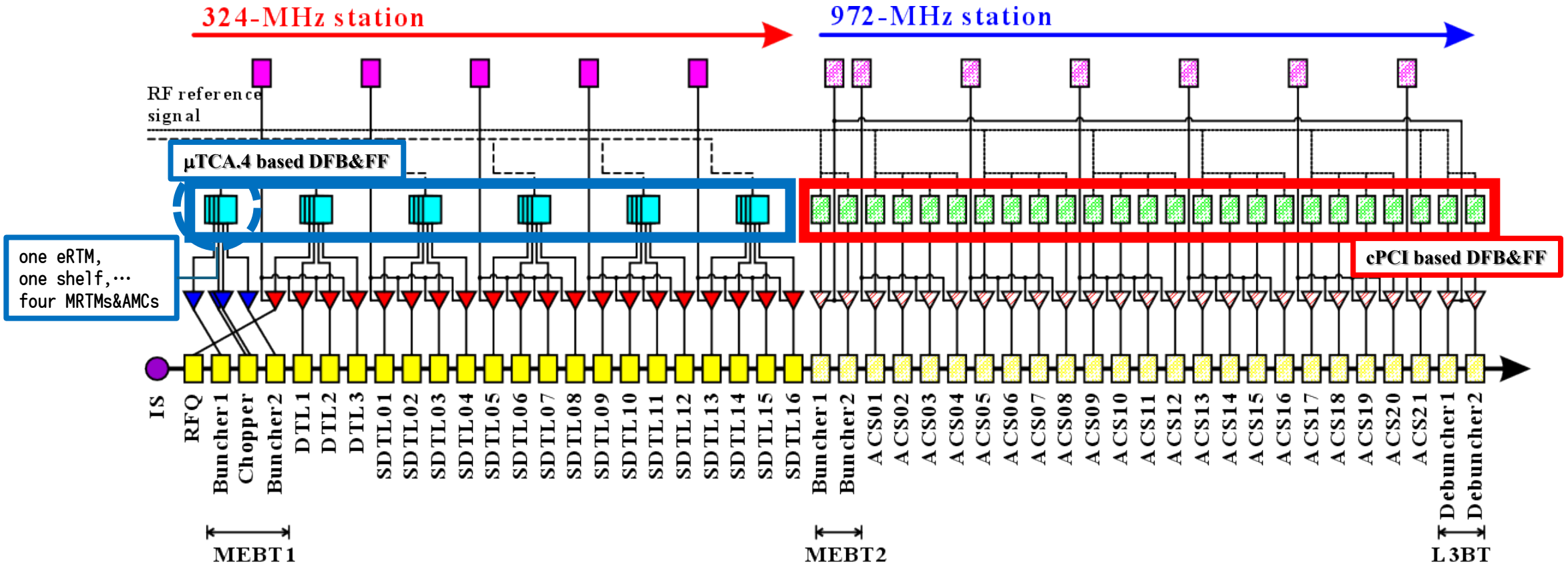
972 MHz	7	25(cPCI)	25(klystron)	25

2021 Summer Shutdown @ RFQ, DTL1-2

2020 Summer Shutdown @ DTL3, SDTL01-16

Cavity & RF Status @2026

We are purchasing items this fiscal year in preparation for next year's upgrade.



#components	HVDC PS	LLRF(DFB and DFF)	RF source	cavity station
324 MHz	5	24(μTCA.4) 0(digitizer box)	20(klystron) 4(SSA)	24
972 MHz	7	25(cPCI)	25(klystron)	25

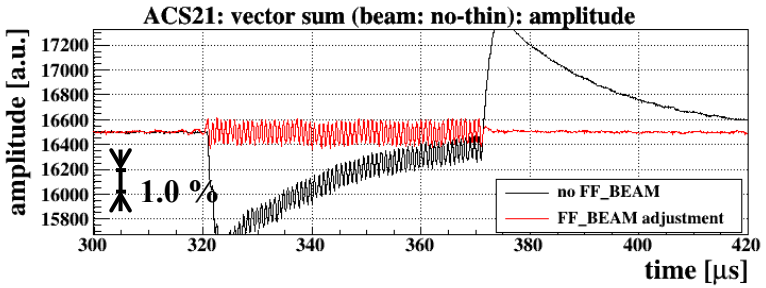
Logic Test @972 MHz

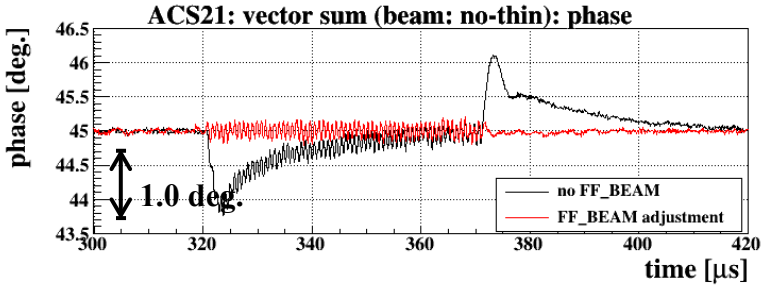
We “temporarily” installed a digitizer box in the ACS21 station and conducted logic tests.

- ✓ wo Beam
  - parameter adjustment program (IQ offset, ADC/DAC rotation)
  - transfer function measurement
- ✓ w Beam
  - Beam loading compensation system

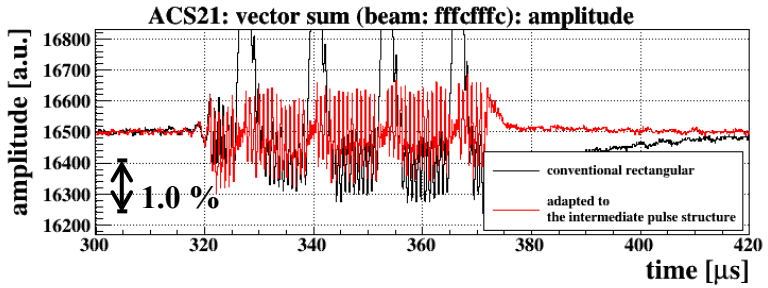
Results of Beam Loading Compensation

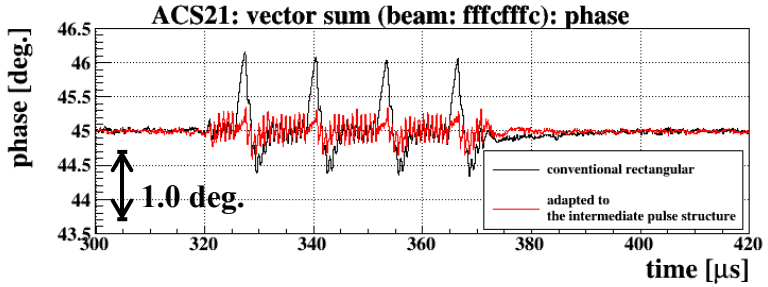
for standard two bunchers



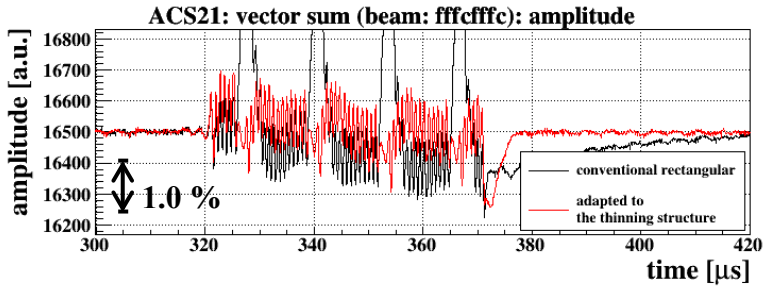


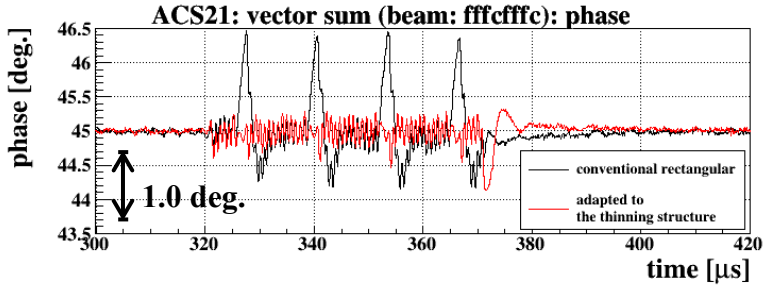
adapted to intermediate pulse





adapted to thinning structure



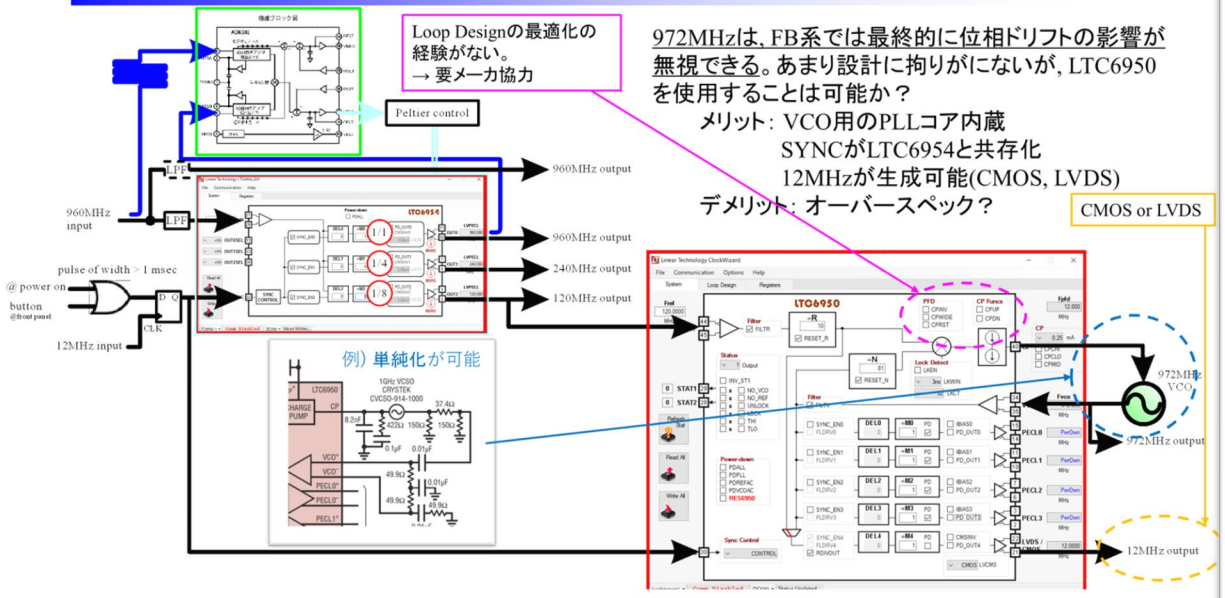


Excluding detailed adjustments, we confirmed that the logic worked without any issues.

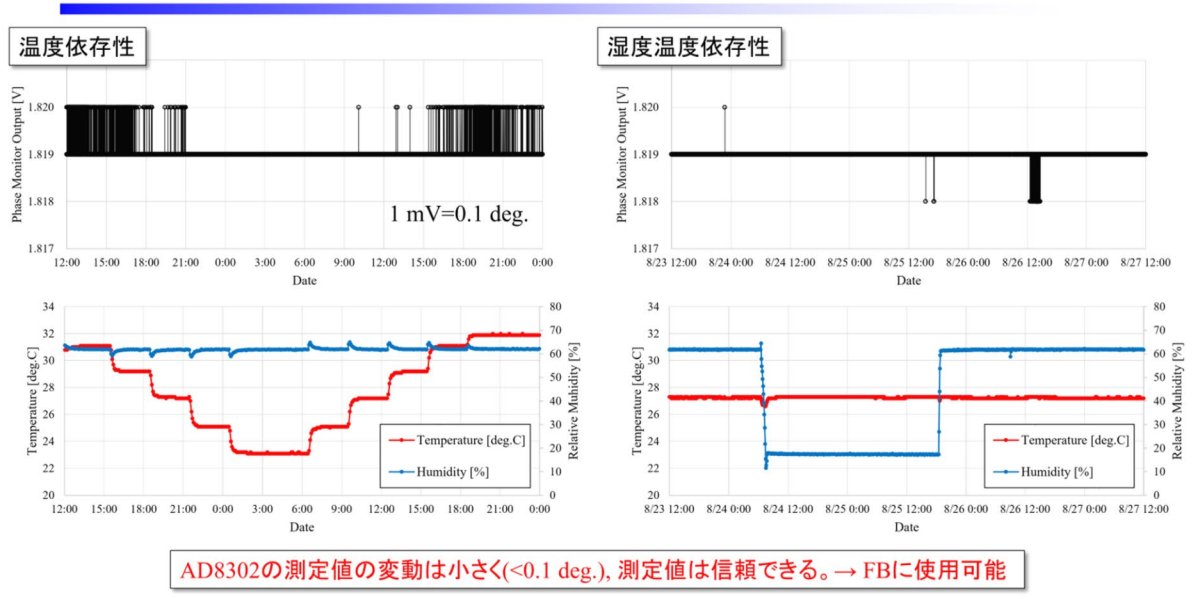
Hardware Development @972 MHz

The eRTM and MRTM boards for the 972 MHz system are currently under development.
The prototypes have already been manufactured, and performance test is in progress.

eRTM w LTC6954: 972MHz生成



AD8302評価ボードの温湿度依存性



Feature of 972-MHz DFB&FF prototype system:

The eRTM prototype board implements a phase drift compensation function using the phase detector AD8302. Both the AD8302 and the frequency divider LTC6954/LTC6950 have been tested using evaluation boards.

Summary

- ✓ We have been developed and operated the cPCI-based DFB&FF system. It is currently being replaced by the MTCA.4-based system, which provides improved performance.
  - ☐ Present Status:
    - MTCA.4: MEBT1(buncher x2, chopper x2), RFQ
    - digitizer box: DTL(3), SDTL(16)
    - cPCI: 972-MHz(25)
  - ☐ 2025 (plan):
    - MTCA.4: 324 MHz(24=6 sets)
    - cPCI: 972 MHz(25)

- ✓ We are confident that updating the digital system of the 972-MHz stations will significantly improve the beam quality.
- ✓ Preparations for the 972 MHz DFB&FF system are also in progress, and replacement to the new system will be implemented sequentially, if the budget allows.