MTCA workshop for accelerator and physics in Japan 2025

Report of Contributions

Contribution ID: **1** Type: **not specified**

From organizers

Wednesday, 27 August 2025 14:00 (10 minutes)

Presenter: TAMURA, Fumihiko (J-PARC Center, Accelerator Division)

Contribution ID: **2** Type: **not specified**

Welcome address

Wednesday, 27 August 2025 14:10 (30 minutes)

Presenter: KOMATSUBARA, Takeshi

Contribution ID: **3** Type: **not specified**

Tutorial Lecture: FPGA Development for MicroTCA Platforms: Open-Source Tools and Best Practices

Wednesday, 27 August 2025 15:40 (1 hour)

Field-Programmable Gate Array (FPGA) development is a crucial component in the realization of applications based on MicroTCA systems. Engineers and researchers new to this standard often face significant complexities in handling Advanced Mezzanine Card (AMC) modules, particularly concerning interface implementation (e.g., PCIe, Ethernet, Point-to-Point links), algorithm development, and verification. These common challenges frequently lead to duplicated efforts and "re-inventing the wheel" for recurring FPGA development problems. This tutorial will introduce attendees to a suite of existing open-source tools and applications designed to accelerate these development efforts. We will provide practical tips and tricks for the initial bring-up of any AMC board featuring a modern FPGA. The session will feature concrete examples and established solutions deployed in experimental physics facilities across Europe, demonstrating how to avoid common pitfalls and streamline the development lifecycle.

Presenter: GUMUS, Cagil (DESY)

Contribution ID: **5** Type: **not specified**

Development of MTCA-based boards for the LLRF at the KEK PF 2.5 GeV ring

Friday, 29 August 2025 11:40 (20 minutes)

At the KEK Photon Factory 2.5 GeV ring (PF ring), a new LLRF system was installed in 2023. The new system is composed of digital boards based on the MTCA.4 standard. This presentation will summarise the development of these digital boards.

Presenter: NAITO, Daichi (KEK)

Session Classification: Session 6

Contribution ID: **6** Type: **not specified**

Applications of MTCA at J-PARC

Thursday, 28 August 2025 10:00 (20 minutes)

The first application of MTCA at J-PARC is the RCS LLRF control system, which was deployed in 2019. Since then, the number of the applications at J-PARC is steadily increasing. The LLRF control systems for MR and Linac are now fully operational. We have several future applications, for example, the digitizer for Linac beam loss monitors and the timing system. The status and future plan of the MTCA application at J-PARC are presented.

Presenter: TAMURA, Fumihiko (J-PARC Center, Accelerator Division)

Session Classification: Session 1

Contribution ID: **7** Type: **not specified**

NAT-MCH Gen4

Thursday, 28 August 2025 17:00 (20 minutes)

The 4th generation of NAT-MCH is the successor of the 3rd generation of NAT-MCH, which - after more than 18 years of successful deployments - is coming to its end of life now. The 4th generation MCH provides a lot of improvements and new features and functions, such as 10GbE base switch with 25GbE uplinks, new 40/100GbE fat pipe hub with 10/40/100GbE uplinks, new PCIe Gen 4 fat hub, new CLK module with replacement for IDT multiplexer, new web and harmonized CLI interface in order to name a few. Also, the 4th generation MCH is MTCA.0 Rev 3 compliant and has been designed to meet the upcoming requirements addressed by the next generation of MicroTCA as close as possible already. To ensure product continuity, the family of NAT-MCHs of the 4th generation include ready-to-go products for science and research, similar to the NAT-MCH-PHYs and NAT-MCH-PHYS80. After a short overview comparing the 3rd generation NAT-MCH with its 4th generation, N.A.T. will explain how existing customers can easily migrate to the 4th generation MCH in existing applications.

Presenter: KOERTE, Heiko (N.A.T.)

Session Classification: Session 4

Contribution ID: **8** Type: **not specified**

Operational experience of MTCA.4-based BPM electronics for SPring-8

Thursday, 28 August 2025 10:40 (20 minutes)

The single-pass BPM electronics at SPring-8 has been replaced by MTCA.4-based electronics. BPM signals are processed by an RTM and sent to a high-speed digitizer AMC. The BPM signal has an RF component synchronized to the acceleration RF frequency of 508.58 MHz. This component is extracted from the filter on the RTM, the signal level is adjusted, and the RF signal is directly sampled by the digitizer. The sampling rate of the digitizer is 363.27 MHz, which is 5/7 of the RF frequency. The sampling clock is generated by a clock eRTM and distributed through an RF backplane for MTCA.4. The acquired data is processed by an FPGA on the digitizer, and the beam position is calculated. This new readout system provides beam position data of both single-pass and COD (Closed Orbit Distortion) in parallel. The new readout system will be utilized for all the BPMs in the SPring-8-II storage ring, which is a low-emittance upgrade of SPring-8. The position resolution of the new BPM system was confirmed to be less than 100 μm for a single-pass mode with a bunch charge of 100 pC, and less than 1 μm for a fast acquisition (10 kHz) COD mode. In this contribution, we present the operational experience of the new BPM readout electronics.

Presenter: MAESAKA, Hirokazu (RIKEN SPring-8 Center)

Session Classification: Session 1

Contribution ID: **9** Type: **not specified**

Application of MTCA to collision feedback system in SuperKEKB

Thursday, 28 August 2025 11:30 (20 minutes)

SuperKEKB implements a collision feedback system to maintain stable collision. The system consists of several MTCA boards. This presentation describes the application of MTCA to the feedback system.

Presenter: FUKUMA, Hitoshi (KEK)

Session Classification: Session 2

Contribution ID: **10** Type: **not specified**

MMC Software Engineering: Challenges and Solutions

Thursday, 28 August 2025 15:10 (20 minutes)

The Module Management Controller (MMC) is a critical intelligent controller responsible for managing AMC boards. It communicates with the MTCA Carrier Hub (MCH) via the Intelligent Platform Management Bus Local (IPMB-L). Since 2010, we have been developing MMC software for our AMC and uRTM boards. During development, we encountered challenges related to the complex protocols defined in the Intelligent Platform Management Interface (IPMI) specifications, including the AMC, ATCA, and MTCA standards. Additionally, the use of a small microcontroller imposed strict limitations on ROM and RAM capacity, making it difficult to fully implement all required specifications. This presentation provides a concise overview of our experience in developing MMC software.

Presenter: KITAGAWA, Ryuta (MITSUBISHI ELECTRIC DEFENSE AND SPACE TECHNOLOGIES CORPORATION)

Session Classification: Session 3

Contribution ID: **11** Type: **not specified**

Operational experience of MTCA.4 modules used at LLRF of SPring-8 storage ring

Thursday, 28 August 2025 11:50 (20 minutes)

We had four RF stations in SPring-8 storage ring. We replaced the NIM module based system to MTCA.4 module based system at RF station A in 2018. The replacement of the LLRF system at other three RF stations were carried out step by step. In this talk, operational experience of MTCA.4 modules will be shown.

Presenter: OHSHIMA, Takashi (JASRI)

Session Classification: Session 2

Contribution ID: **12** Type: **not specified**

OPERATION STATUS OF A LLRF CONTROL SYSTEM AT WERC

Thursday, 28 August 2025 10:20 (20 minutes)

A LLRF control system for a synchrotron based on MTCA.4 has been developed and operated at WERC. The system was replaced old one consisted of DDS (Direct Digital Synthesizer), DSP (Digital Signal Processor) and analog RF circuits. The new system consists of three AMCs. One is for feedback control of RF frequency and the others are for processing beam position signals. In 2018-2019, we designed and made an FPGA circuit based on the J-PARC LLRF system. From 2020 to 2021, we confirmed the operation of the cavity voltage feedback in the off-beam state. From November 2021, we repeated beam tests to find and correct defects. In parallel with the above, we developed operation interfaces. From October 2023, we began using the feedback control unit for normal operation. This increased the acceleration efficiency from ~70% to ~80%, and the extraction current from ~ 2.5 nA to ~3 nA. Previously, frequency control was performed using B-Clock, but in 2024, adjustment of a frequency pattern using T-Clock was established. From fiscal year 2025, operations using T-Clock patterns will be introduced. In November 2024, COD measurements were performed using the BPM signal processing system. The validity of the measurement results was confirmed by comparing them with measurements using the old system.

Presenter: KURITA, Tetsuro (The Wakasa Wan Energy Research Center)

Session Classification: Session 1

Contribution ID: **13** Type: **not specified**

A high-speed MTCA.4-based digitizer for the J-PARC MR

Thursday, 28 August 2025 14:50 (20 minutes)

J-PARC Main Ring (MR) delivers the 30-GeV protons to the particle physics experiment. Microwave instabilities have been observed in the J-PARC MR during both the acceleration for the beam to the neutrino experiment and the debunching process for the beam to the hadron experiment. Since the instability does not occur every shot, monitoring the waveform of the beam signal for every shot is desired to investigate the source of the instability. Currently, the oscilloscopes are used to monitor and record the waveform of the beam signal. Since the data acquisition from the oscilloscope via Ethernet is not fast enough for the fast repetition cycle of the MR, we introduced an MTCA-4-based high-speed digitizer to record the waveform. The large memory on the module and the data transfer via the PCI Express bus enable us to monitor and record the whole acceleration cycle. In this presentation, we present the current status of the new digitizer in the J-PARC MR.

Presenter: SUGIYAMA, Yasuyuki (KEK/J-PARC)

Session Classification: Session 3

Contribution ID: **14** Type: **not specified**

Introduction of digitizers with MTCA interface and application specific firmwares

Thursday, 28 August 2025 14:30 (20 minutes)

TSPD offers digitizer products with various interfaces. We will introduce the models with MTCA interface, along with application-specific firmware developped for those products.

Presenter: KAWAMATA, Yoshikazu (Teledyne SP Devices)

Session Classification: Session 3

Contribution ID: **16** Type: **not specified**

MicroTCA-based LLRF systems used at the STF at KEK

Friday, 29 August 2025 09:50 (20 minutes)

In this contribution we present the MicroTCA-based LLRF systems used for the STF-II accelerator. At the same facility a vertical test stand for the R&D of superconducting cavities is operated. The over 20-year-old analog control system is being replaced by a MicroTCA.4-based system. We report on the commissioning status of it. In addition to this an outlook for the planned MicroTCA.4-based digital LLRF system for the test of an ILC prototype CM is being presented.

Primary author: OMET, Mathieu (KEK)

Co-author: Prof. MATSUMOTO, Toshihiroo (KEK)

Presenter: OMET, Mathieu (KEK)

Session Classification: Session 5

Contribution ID: **17** Type: **not specified**

Present Status of J-PARC LINAC LLRF (Tentative)

Friday, 29 August 2025 09:30 (20 minutes)

Presenter: FUTATSUKAWA, Kenta (KEK)

Session Classification: Session 5

Contribution ID: **18** Type: **not specified**

Upgrade plan of MicroTCA based event timing system at KEK LINAC

Friday, 29 August 2025 11:00 (20 minutes)

VME-based event timing system plays an important role for the synchronization of beam diagnostics and accelerator device control at KEK LINAC. However, with some VME modules approaching its market end-of-life, transitioning to modern platforms like MicroTCA is becoming necessary. We decide to migrate the timing system by focusing on a phased upgrade approach, where new MicroTCA based MRF 300-series timing modules will coexist with and eventually replace the legacy VME timing modules. This talk introduces the plan and current status of timing system upgrade.

Presenter: WANG, Di (KEK)

Session Classification: Session 6

Contribution ID: **19** Type: **not specified**

Automated Passband Mode Resonance Peak Finding Algorithm Using MicroTCA.4-Based Digital LLRF System

Friday, 29 August 2025 10:10 (20 minutes)

The vertical test (VT) stand at the KEK Superconducting RF Testing Facility (STF) uses an analog RF control system which is over 20 years old now. We are currently in the process of replacing this old system with a new digital LLRF system based on the MicroTCA.4 architecture. The digital system also allows for greater flexibility regarding configurability and software automation due to the integration of a CPU in the MicroTCA.4 crate. It is our goal to automate the VT process to improve measurement repeatability, reliability, and speed. One crucial step towards this goal is automated identification of multi-cell (3 and 9-cell) cavity passband modes. To accomplish this, we have developed an automated resonance peak finding algorithm which utilizes broadband noise injection and calculates the FFT spectrum of the cavity response. We have developed a method to combine multiple FFT measurements across different frequency ranges to improve frequency resolution and signal to noise ratio. To demonstrate the capabilities of this method for multi-cell cavity passband mode identification, we have successfully measured all the passband modes of a 3-cell cavity during VT.

Primary author: VIKLUND, Eric (KEK)

Co-authors: UMEMORI, Kensei; OMET, Mathieu (KEK)

Presenter: VIKLUND, Eric (KEK)

Session Classification: Session 5

Contribution ID: **20** Type: **not specified**

Keynote Talk: Future Linear Collider and its LLRF system

Thursday, 28 August 2025 16:30 (30 minutes)

Presenter: MICHIZONO, Shinichiro (KEK)

Contribution ID: **21** Type: **not specified**

Closing

Friday, 29 August 2025 12:20 (20 minutes)

Presenter: TAMURA, Fumihiko (J-PARC Center, Accelerator Division)

Contribution ID: **22** Type: **not specified**

Operation status of MTCA.4 based LLRF control system for the J-PARC MR

Friday, 29 August 2025 11:20 (20 minutes)

Presenter: SUGIYAMA, Yasuyuki (KEK/J-PARC)

Session Classification: Session 6

Contribution ID: **23** Type: **not specified**

Towards Migration from VME to MicroTCA in Accelerator Control Systems at SuperKEKB and Linac

Thursday, 28 August 2025 12:10 (20 minutes)

The VME system has long been used for accelerator controls in SuperKEKB.
However, since this architecture is now outdated, we have been considering migration to a microTCA-based system.
In this talk, we will present the background and criteria for this transition.

Primary author: SUGIMURA, Hitoshi (KEK ACCL)

Presenter: SUGIMURA, Hitoshi (KEK ACCL)

Session Classification: Session 2

Contribution ID: **24** Type: **not specified**

Current Status of the LLRF System for the Muon Linac of g-2/EDM Experiment at J-PARC.

Friday, 29 August 2025 12:00 (20 minutes)

Presenter: CICEK, Ersin (KEK)

Session Classification: Session 6