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Development of 3D-SOI pixel sensor for the vertex detector of future e^+e^- collider

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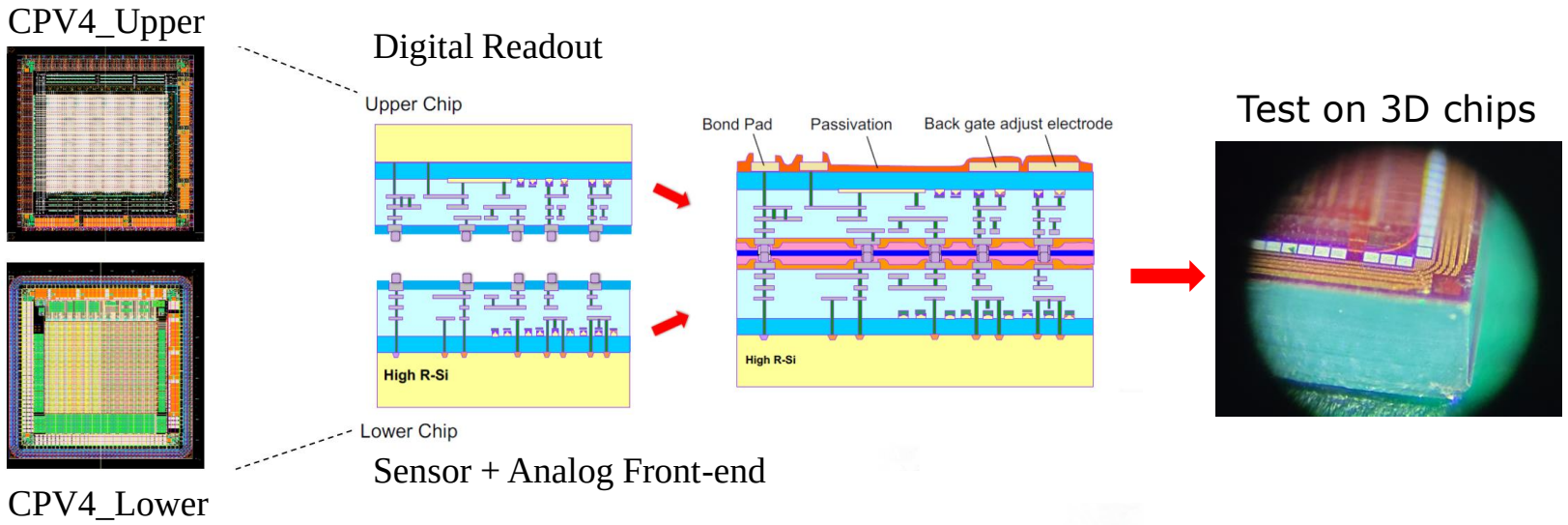
Outline

- Introduction
  - Challenges in vertex detector for future e^+e^- experiment
- Features of CPV-4 design and 3D-SOI process
  - Sensing diode
  - Analog/Digital separation
  - 3D compatibility
- Verification of lower tier
  - Reverse bias voltage
- Verification of upper tier
  - Removal of handle wafer
- Verification of 3D integration
  - connectivity
- Summary and Outlook

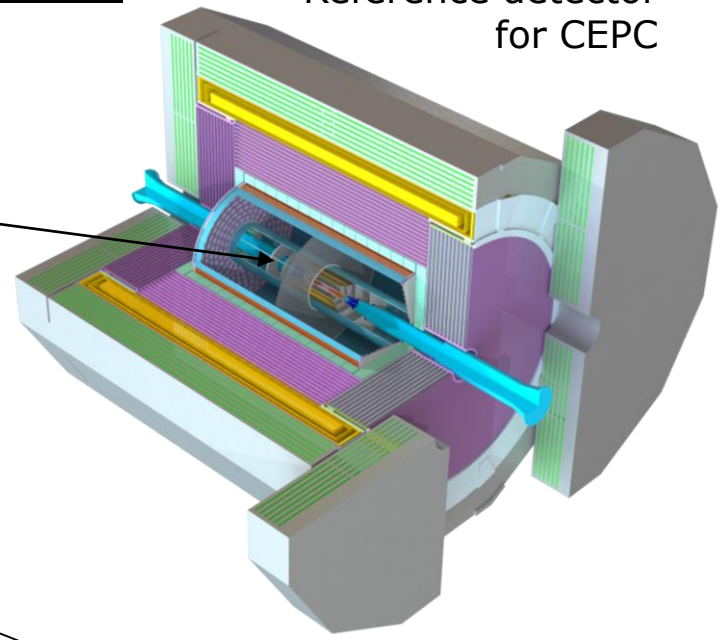


Requirements of Vertex detector for the future e^+e^- experiment

- Measure charged particles with high position resolution at high collision rate
  - Impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,(\mu m)$$

Reference detector for CEPC



Vertex sub-detector is the inner-most part of collider experiments

Physics driven requirements | **Running constraints** | **Sensor specifications**

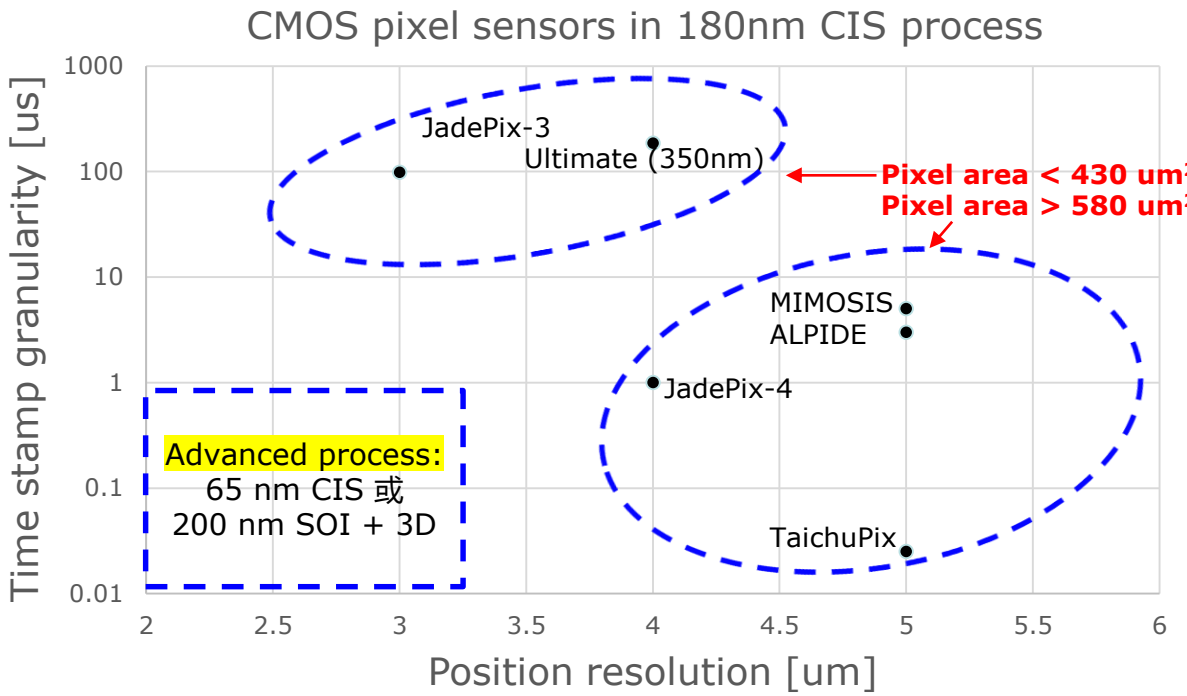
- $\sigma_{s.p.}$ 2.8 μm → Small pixel <20 μm
- Material budget 0.15% X_0 / layer → Thinning ~50 μm
- → Air cooling → Low power <50 mW / cm^2
- r of Inner most layer 16 mm → beam-related background → Time stamp 1 ~ 100 μs
- → radiation damage → Radiation tolerance
  - *3.4 Mrad / year*
  - *$6.2\times10^{12} n_{eq}$ / (cm^2 year)*

Challenges in pixel design

Trade off between Position resolution and Time stamp granularity

- Comparison of pixel sensors using 180nm CIS process
  - Small pixels lose time resolution
  - Fast time stamp use more pixel area

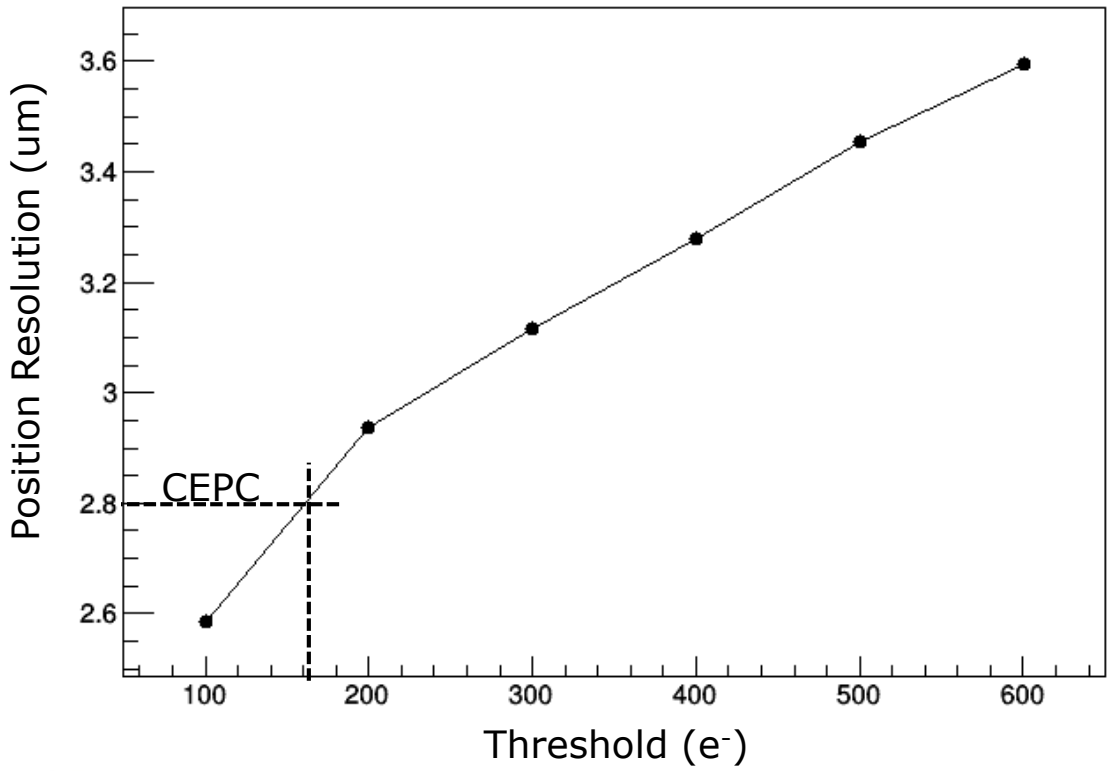
Name	Pixel size [um²]	Position Resol. [um]	Time Stamp [us]	Readout scheme	Pixel area
MIMOSIS	26.88x30.24	5	5	Data driving	812
ALPIDE	28x28	5	3	Data driving	784
TaichuPix	25x25	5	0.025	Data driving	625
JadePix4	20X29	4	1	Data driving	580
Ultimate	20.7x20.7	4	186	Rolling shutter	428
JadePix3	16x23.11	3	98.3	Rolling shutter	370



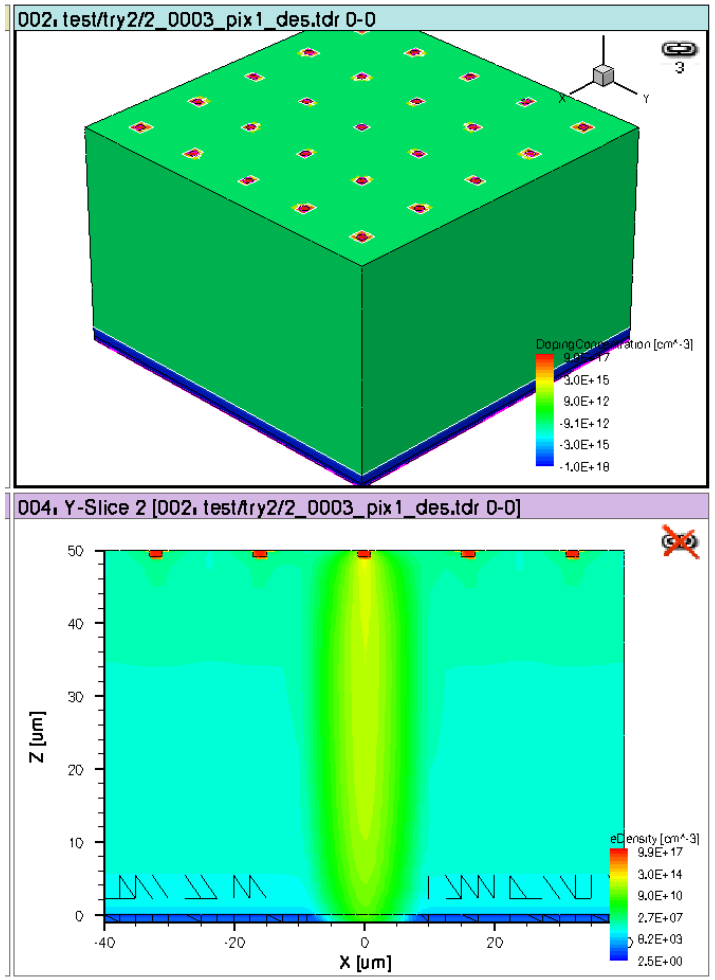
- Advanced process to accommodate needed transistors within a pixel area < 400 μm² (e.g. 16 x 25)
  - 65 nm CIS process
  - 200nm SOI + 3D integration

Device simulation（TCAD）

- Pixel pitch = 16 μm & Sensor thickness = 50 μm
- **Low threshold** is essential for the high position resolution
  - Threshold < 200 e^-
  - ENC ~ 20 e^-



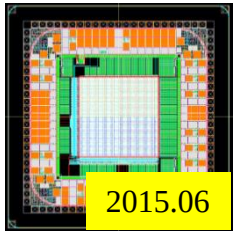
Charge transportation in TCAD simulation



Development of the CPV SOI pixel sensor

- Targeting on a **position resolution ~ 3 um** and a readout scheme compatible with the proposed CEPC experiment
  - CPV-1&2 for the study of position resolution of small pixels with simplified readout (FEE2018)
  - CPV-3 for the study of PDD sensing diode (NIMA 1040 (2022) 167204)
  - CPV-4 for the 3D architecture (this talk)

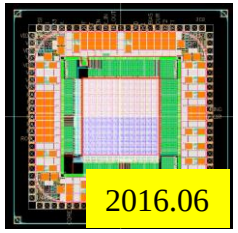
Pixel size:
16 μm × 16 μm



CPV-1

Process assessment

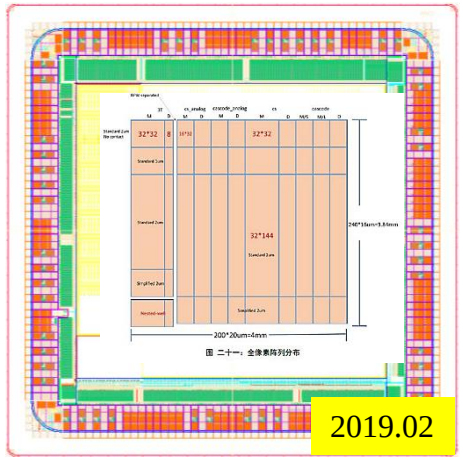
Pixel size:
16 μm × 16 μm



CPV-2

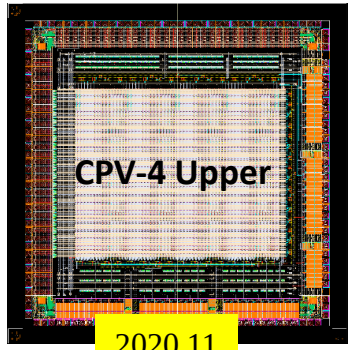
S.P. Resolution 2.3 μm;
Thinned to 75 μm

Pixel size:
16 μm × 20 μm

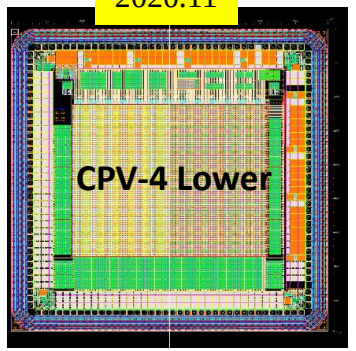


CPV-3

Pinned Depleted Diode;
Optimized for low FPN 12 e⁻



Pixel size:
17 μm × 21 μm



CPV-4

3D architecture;
Stacking process;

Compact Pixel for Vertex (CPV)

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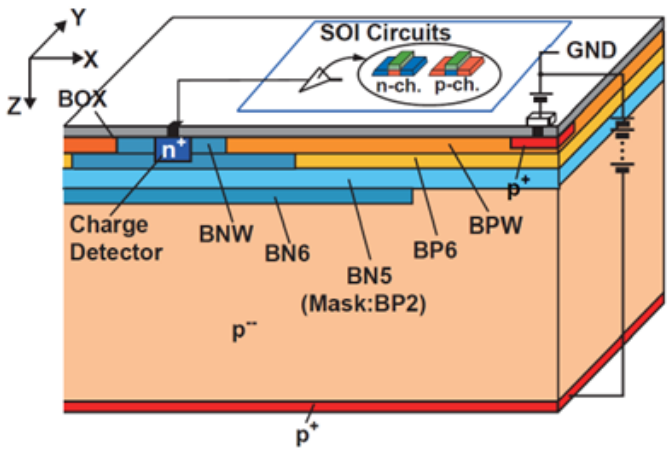
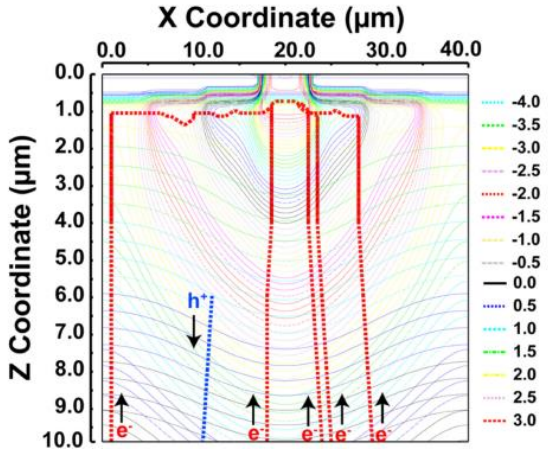
PDD structure

- Improvement of sensing diode
  - Pinned Si surface layer → reduction of surface leakage by 2 orders of magnitude
  - Depleted charge collection electrode → reduction of diode capacitance
  - Lateral electric field → improved charge collection efficiency





Proposed by Shoji Kawahito (Shizuoka U.)
Ref: Sensors 2018, 18, 27; doi:10.3390/s18010027

- Pinned Depleted Diode (PDD)
  - CPV-3&4 chip design
- Double-SOI
  - CPV-1&2 chip design
- Nested-wells
- Buried P-Well (BPW)

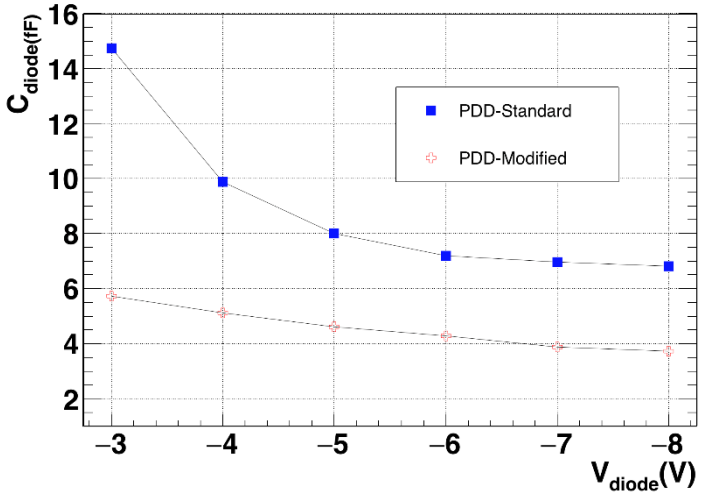
Evolution of SOI detector process

CPV-4 sensing diode

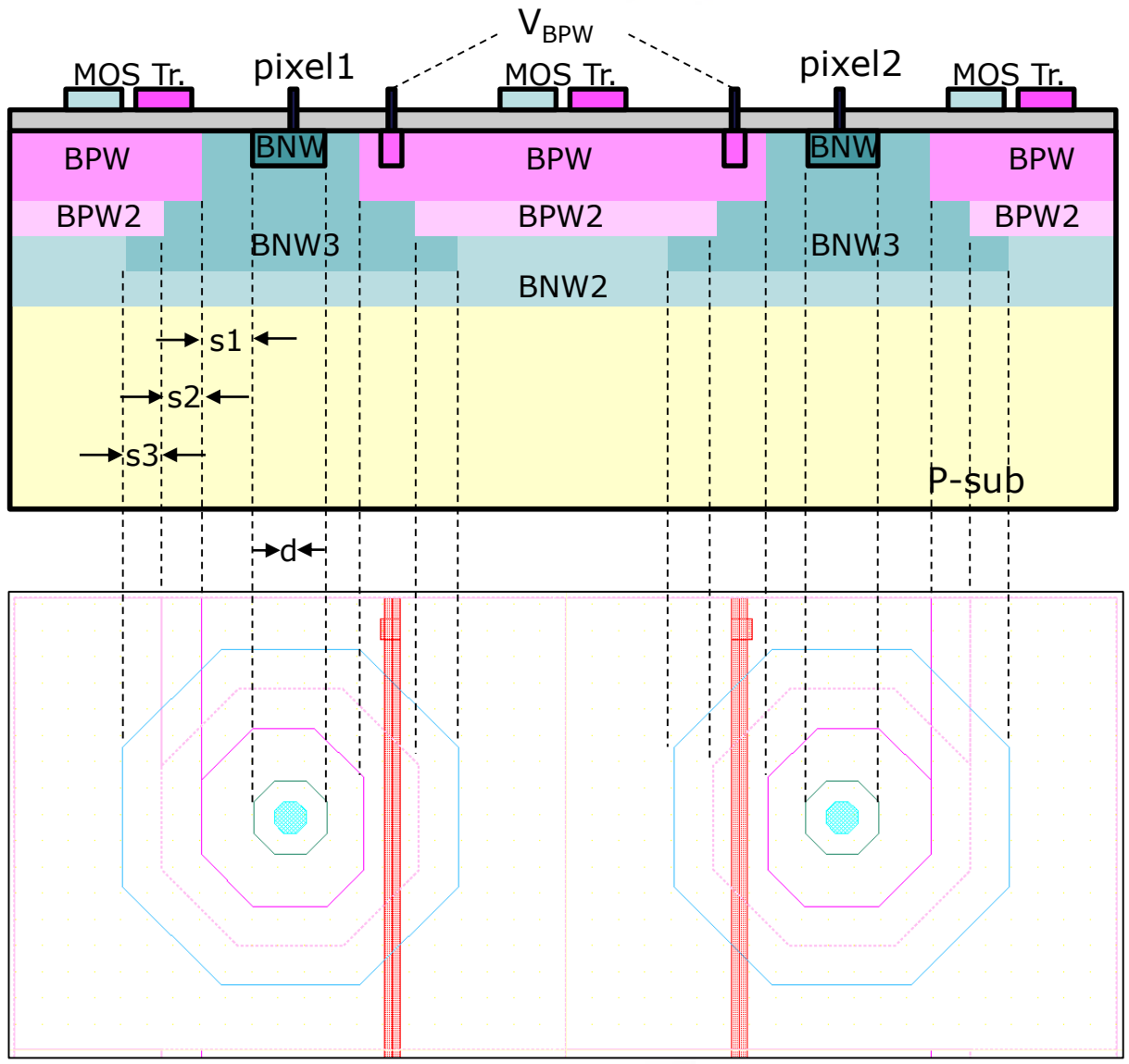
- Geometry parameter optimized for **small pixel pitch**
  - Indicated in the diagram as d, s1, s2, s3

PDD type	d	s1	s2	s3
Standard	2.8 μm	2 μm	1.5 μm	1.5 μm
Modified	2.8 μm	2 μm	N/A	N/A

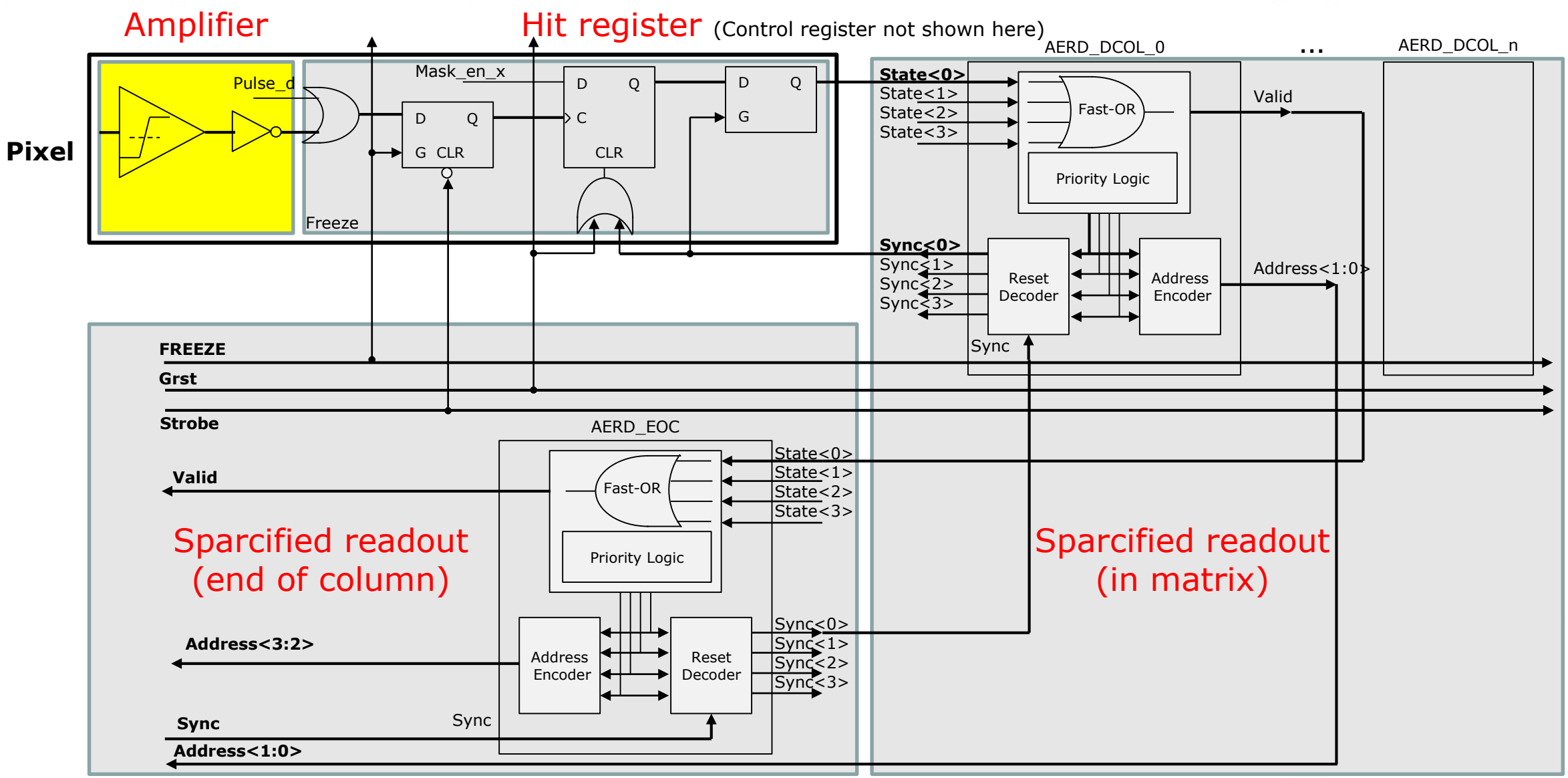
- "Modified" has the BNW3/BPW2 removed
  - Lower diode capacitance than PDD "Standard"



Diode capacitance measured on CPV-3 chip
$V_{diode} = V_{BPW} - V_{bnw}$ with V_{PSUB}=-20V

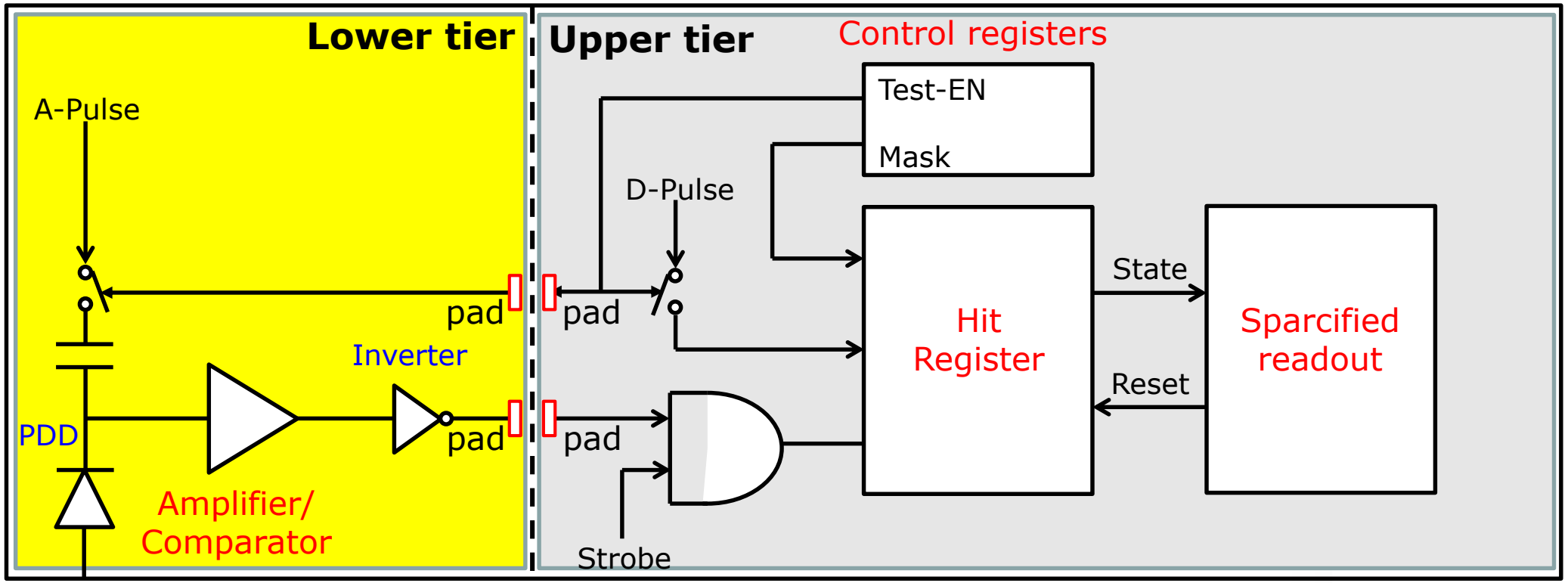


CPV-4 Pixel Readout Scheme



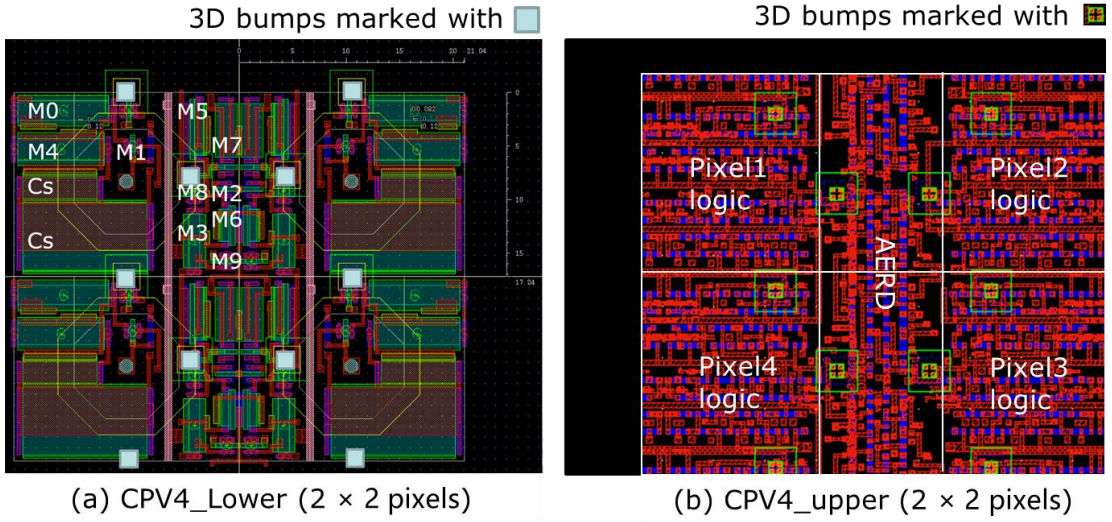
Division of upper and lower functionality

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit D-Flipflop + Control register + AERD readout
- **2 vertical connections** in each pixel: comparator output and switch of test pulse
  - Power and Ground are connected to the lower tier via the pad ring



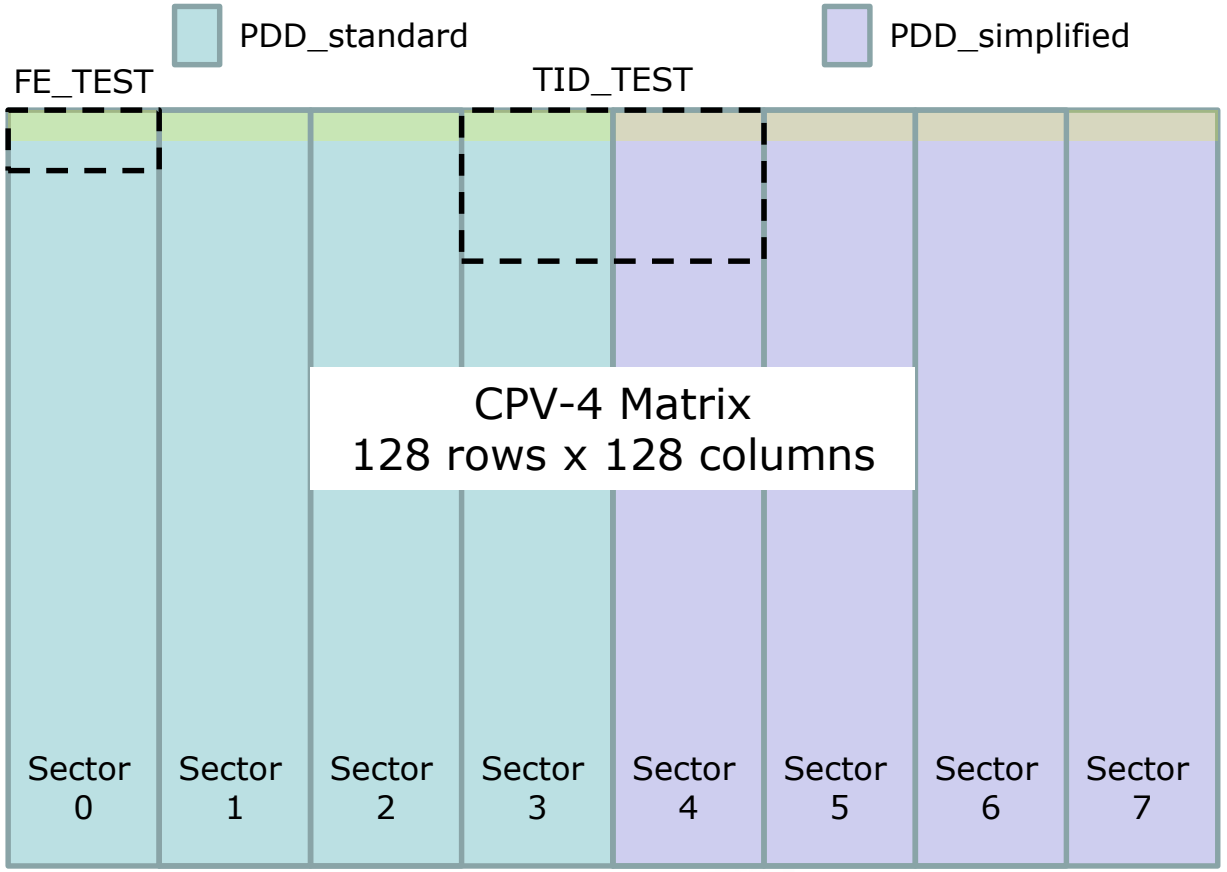
CPV-4 Matrix

- 128 rows x 128 columns, divided into 8 sectors
  - PDD standard vs simplified
  - 2 variants of Front-end
  - H-gate transistor to improve TID tolerance
- Pixel pitch 17µm x 21 µm
  - Smallest pitch of similar design
  - Pixel Area ~ 360 µm^2



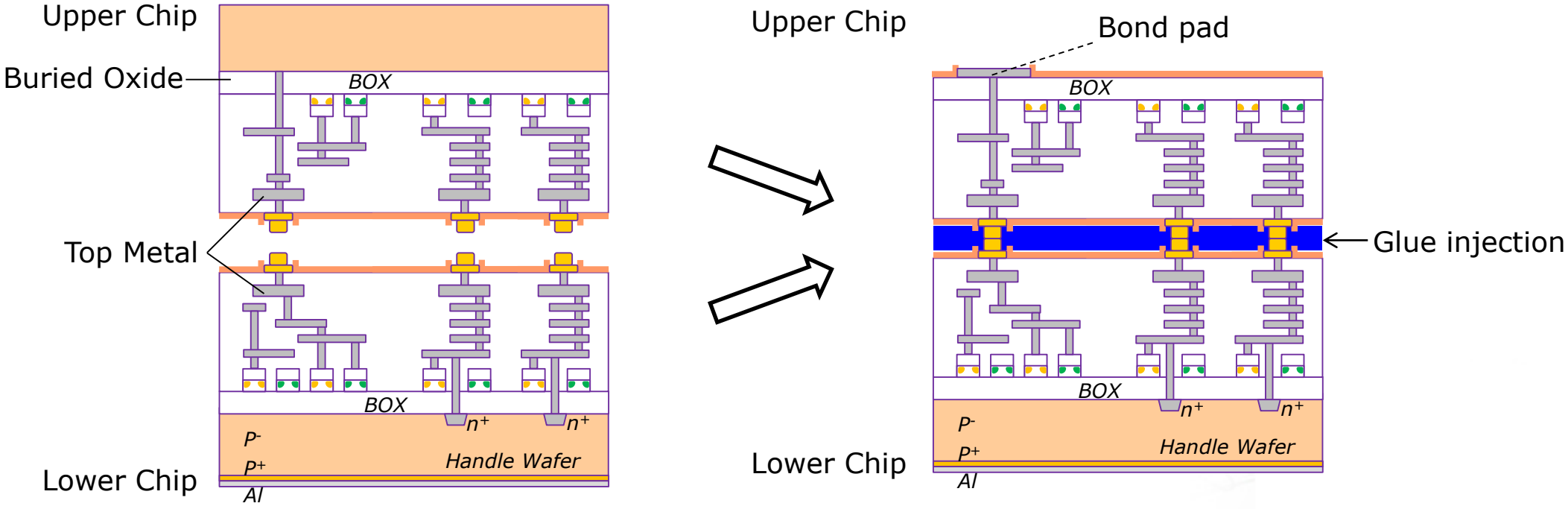
(a) CPV4_Lower (2 × 2 pixels)

(b) CPV4_upper (2 × 2 pixels)



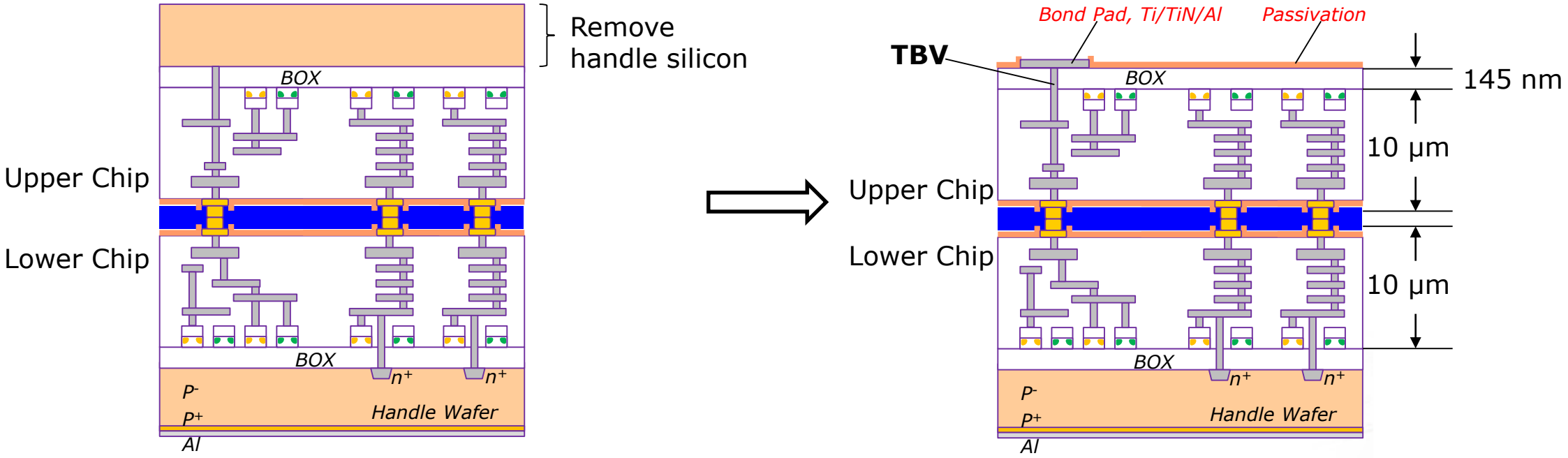
3D-SOI vertical integration

- Originally developed by T-micro and KEK
  - Au bump, diameter ~ 3.5 um, pitch ~ 7 um, resistance 0.3 ~ 0.4 Ω
  - **Multiple bumps in each pixel**, for signals and (optional) power/ground connections
  - Glue injection for mechanical strength
  - Bond pads and passivation on top of BOX



Compatibility between SOI and 3D

- Through Box Via (TBV) used for the bond pad connections
  - The same type as the connection to the sensing diode
  - Naturally a **Via-first** method
- Handle silicon of the upper chip removed **precisely**, reaching the thin BOX layer and exposing TBVs
  - Wet etching stopped automatically by the Buried Oxide (BOX)



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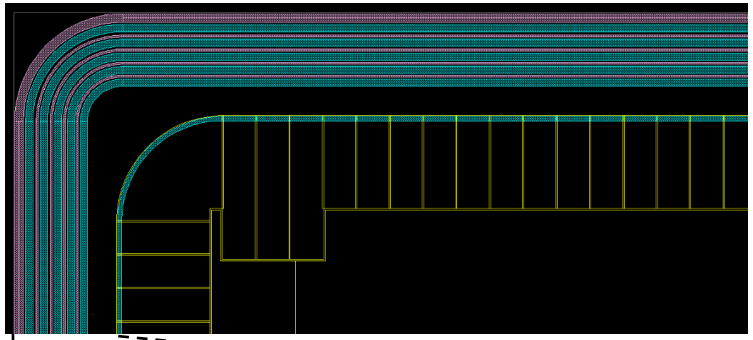
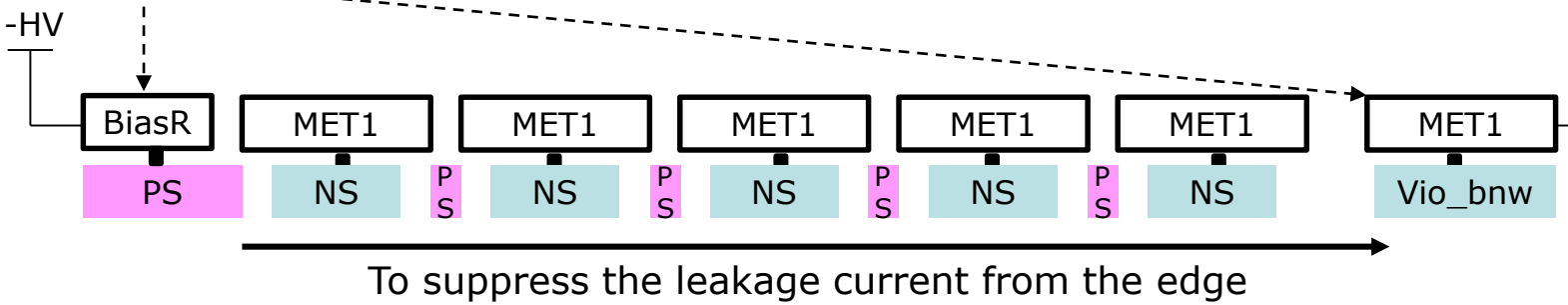
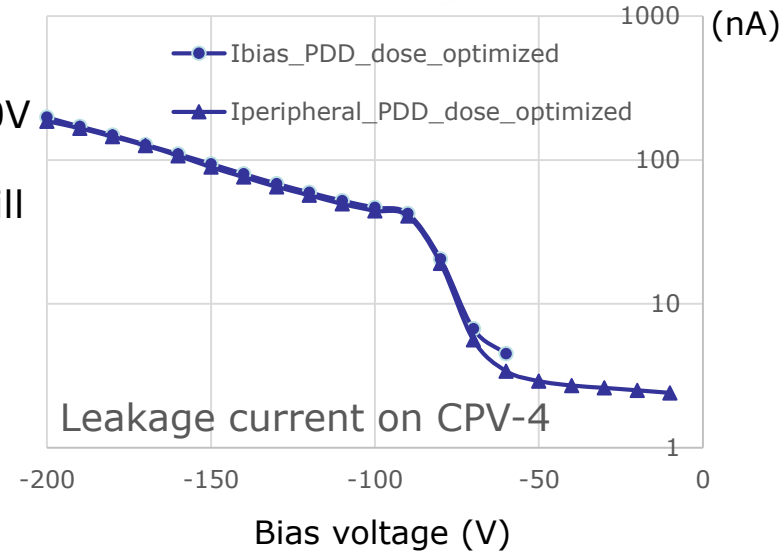
Improvement of Leakage current

- GuardRing on the CPV-4 lower chip

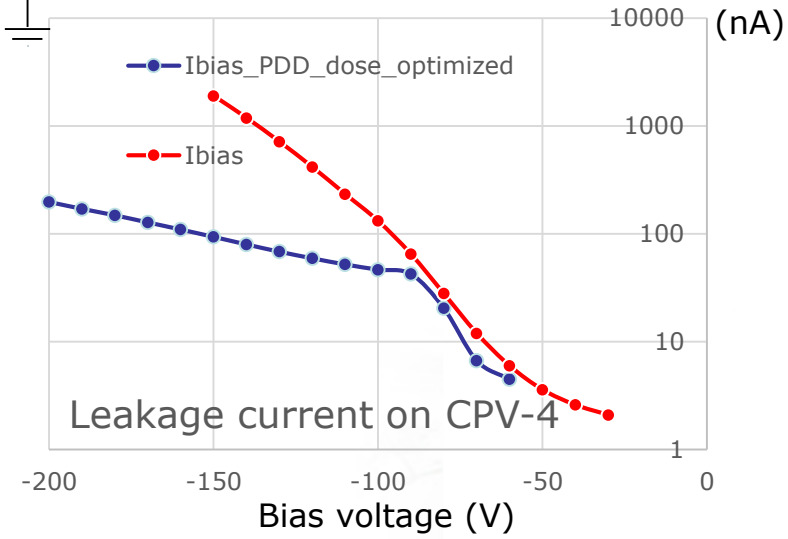


☺ Leakage current 190 nA@-200V measured at room temperature,
☺ Can be improved further as still dominated by peripheral current



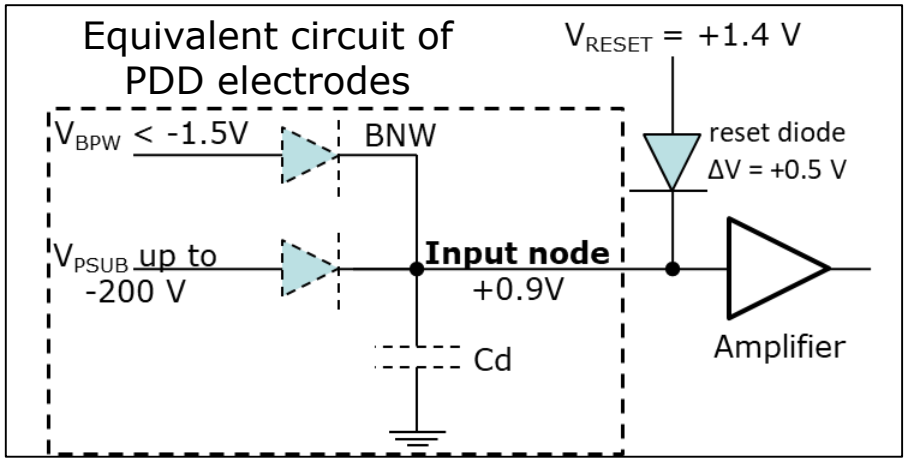


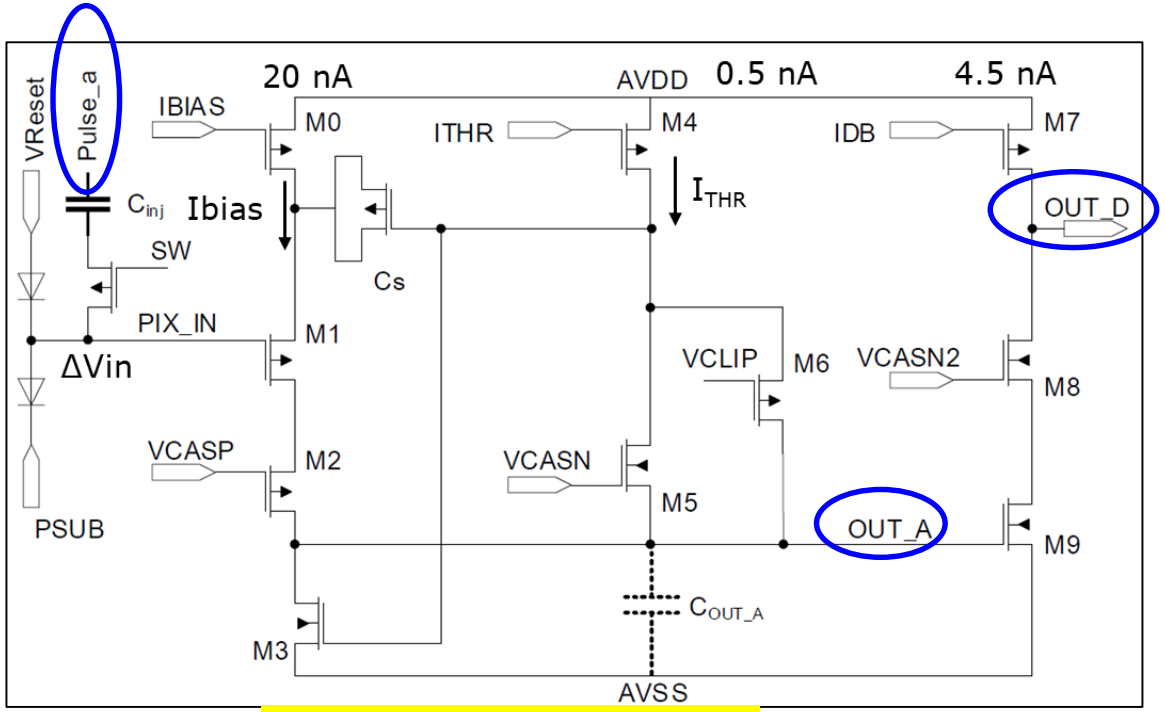
- Optimization of PDD implant dose
  - Direct comparison of different doses



Electrical Pulse Test

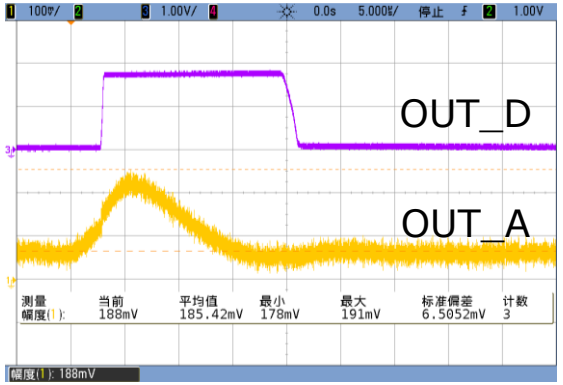
- Charge injection via C_{inj} and Pulse_a to Analog Front-end
  - Observe waveform of test pixels on oscilloscope
- Reverse bias on V_{BPW} is essential for PDD operation
  - Minimum requirement: V_{BPW} < -1.5V
  - Input node (V_{BNW}) fixed to ~ +0.9V by V_{RESET}





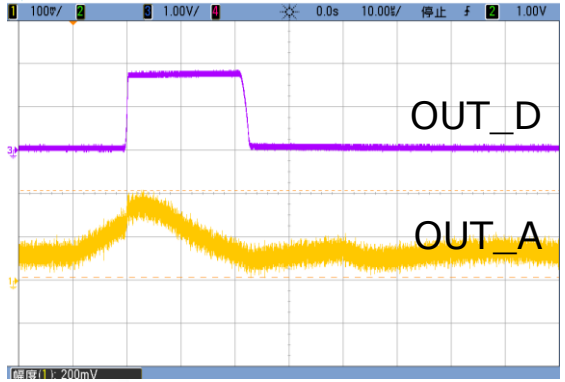
Analog Front-end in CPV-4

Ch1:100 mV / div
Ch2: 1 V / div
5 us / div



Analog frontend w/o PDD,
Test charge injected ~ 100 e^-
V_{BPW} = 0V

Ch1:100 mV / div
Ch2: 1 V / div
10 us / div



Analog frontend w/ PDD,
Test charge injected ~ 750 e^-
V_{BPW} = -1.5V

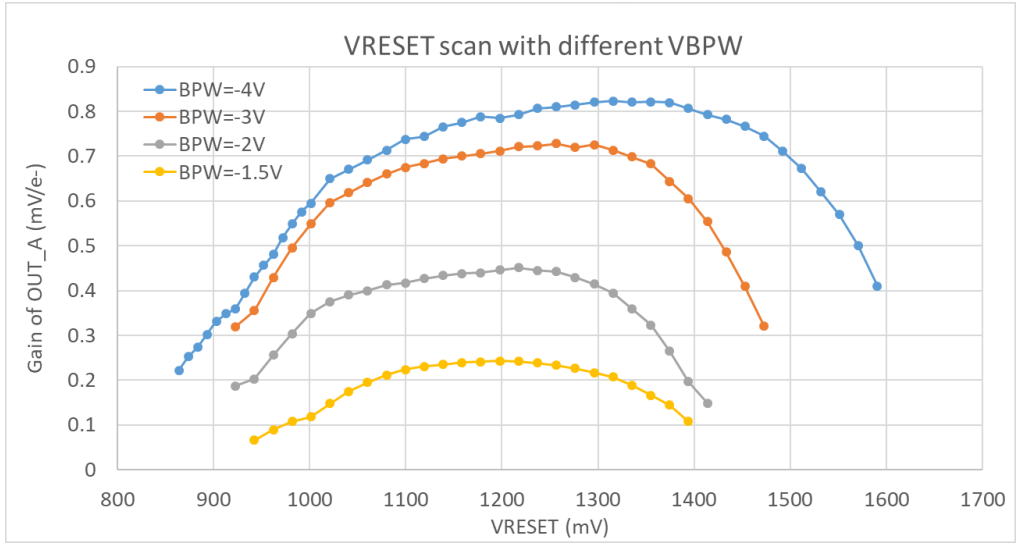
Optimization of bias condition

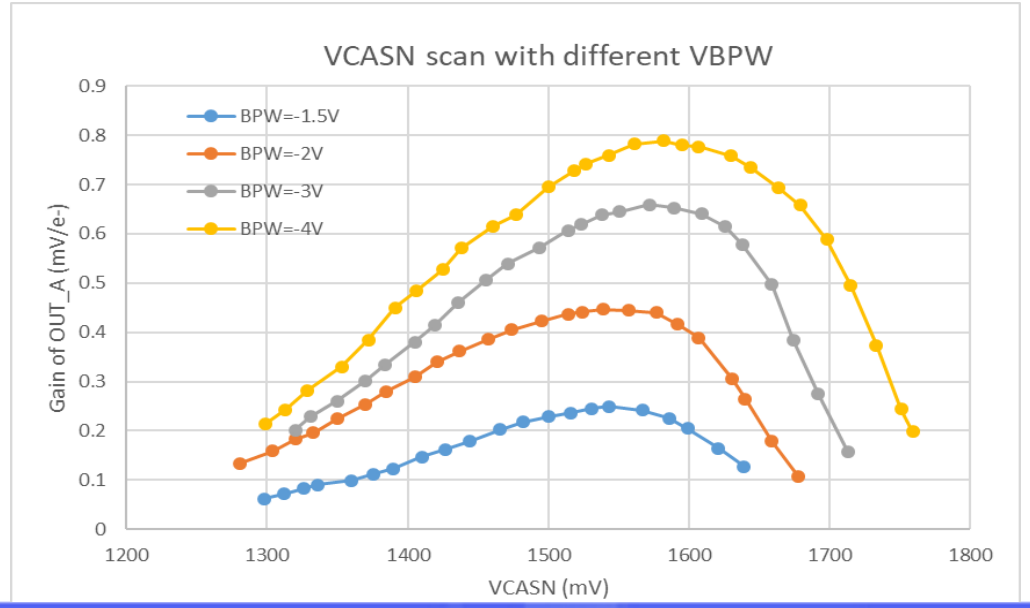
- Transistor threshold shifted due to back-gate effect
  - $\Delta Vt = k\ V_{back}$ ($k \sim 0.02$, $V_{back} = V_{BPW}$)

$$\Delta V_t = \frac{T_{GOX}}{T_{BOX} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} T_{SOI}} V_{back} = kV_{back}$$

- Circuit parameter scan with different V_{BPW}
  - V_{RESET} setting the input node
  - V_{CASN} setting the OUT_A node

- Gain of OUT_A increased with V_{BPW}
  - Gain = OUT_A_amplitude / Input charge
  - Benefitted from reduced C_d

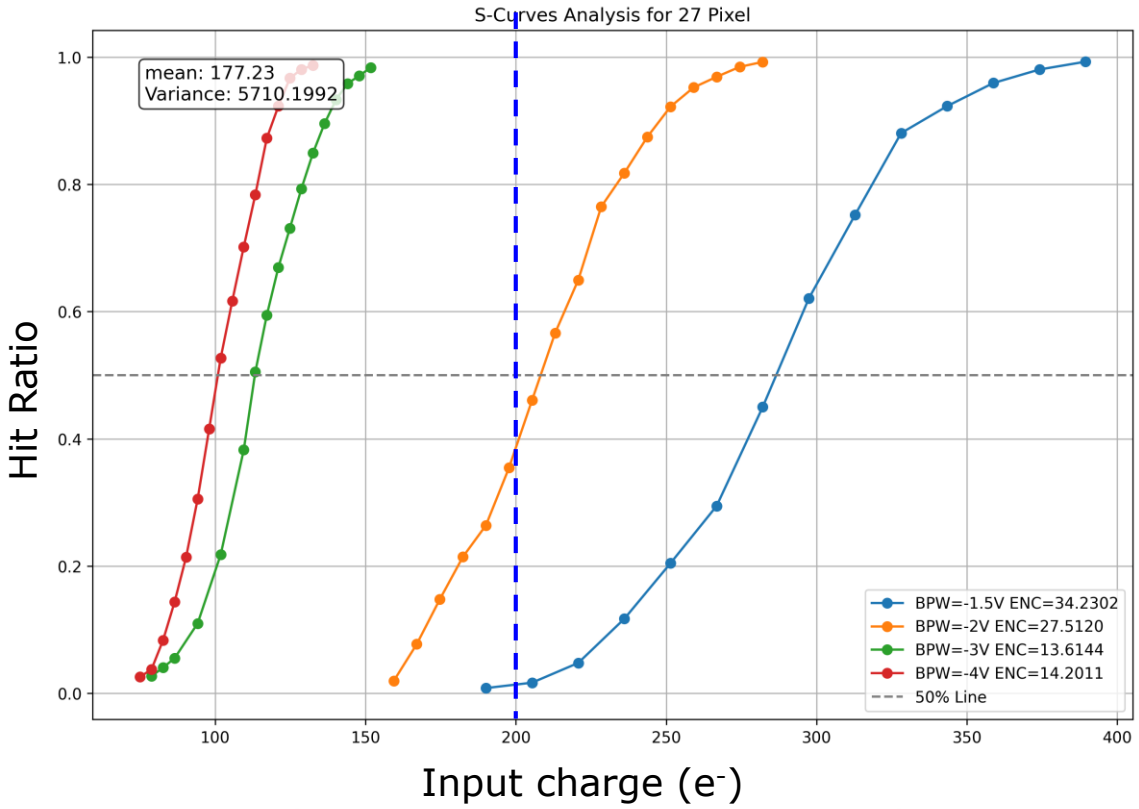




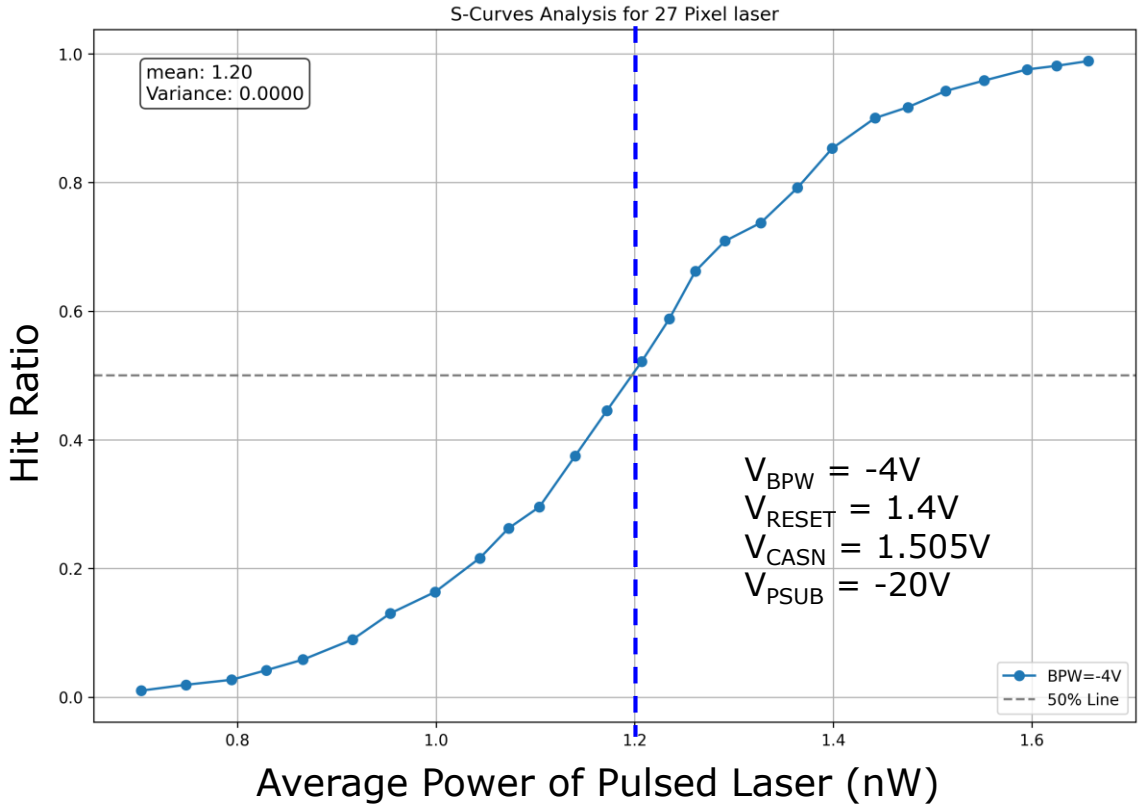
S-curve Measurement

- Electrical pulse test
  - Input-referred threshold decreased with V_{BPW}
  - ENC decreased with V_{BPW}

Targeted threshold



- Infrared laser test
  - Wavelength = 1064 nm & Pulse rate = 500 Hz
  - **Function of lower tier fully verified**



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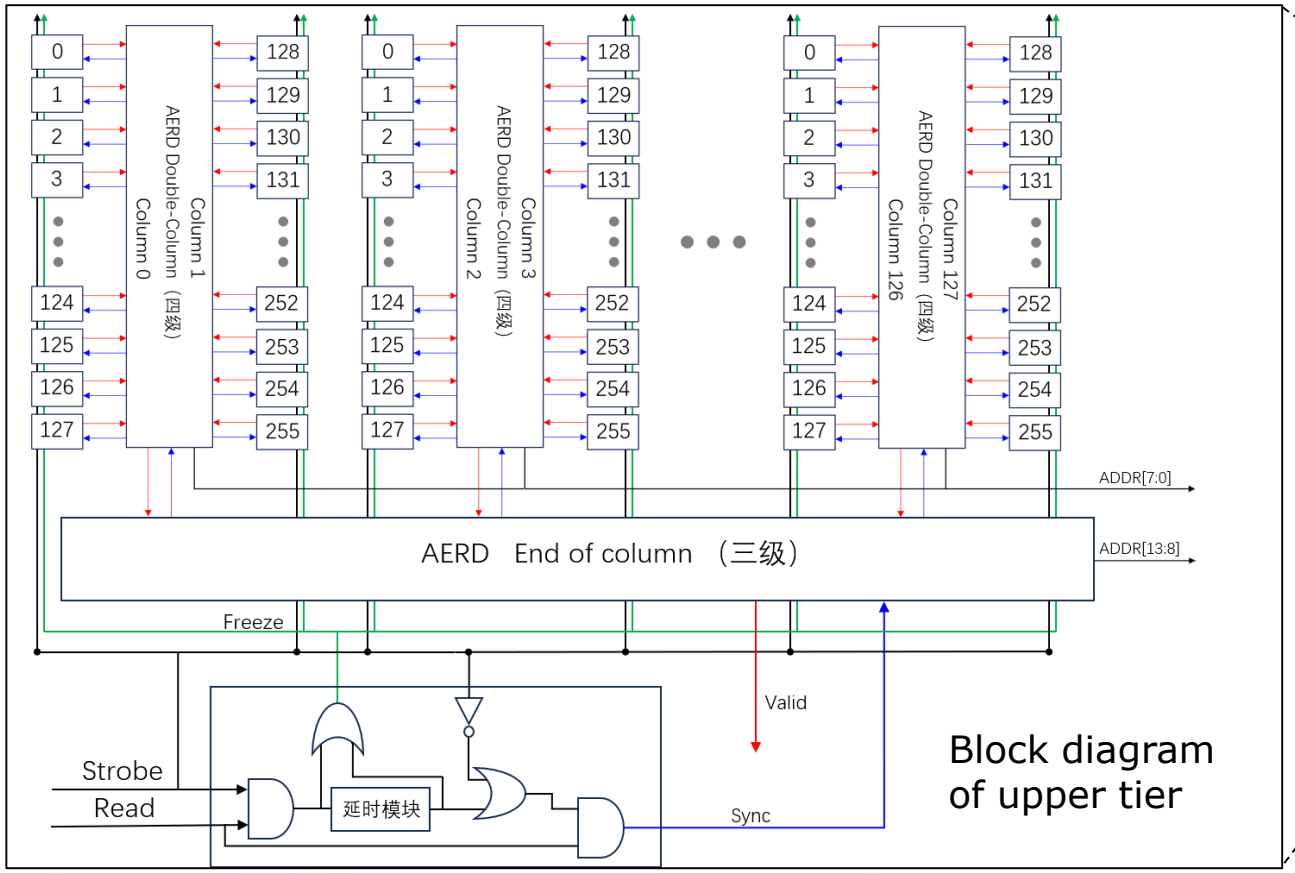
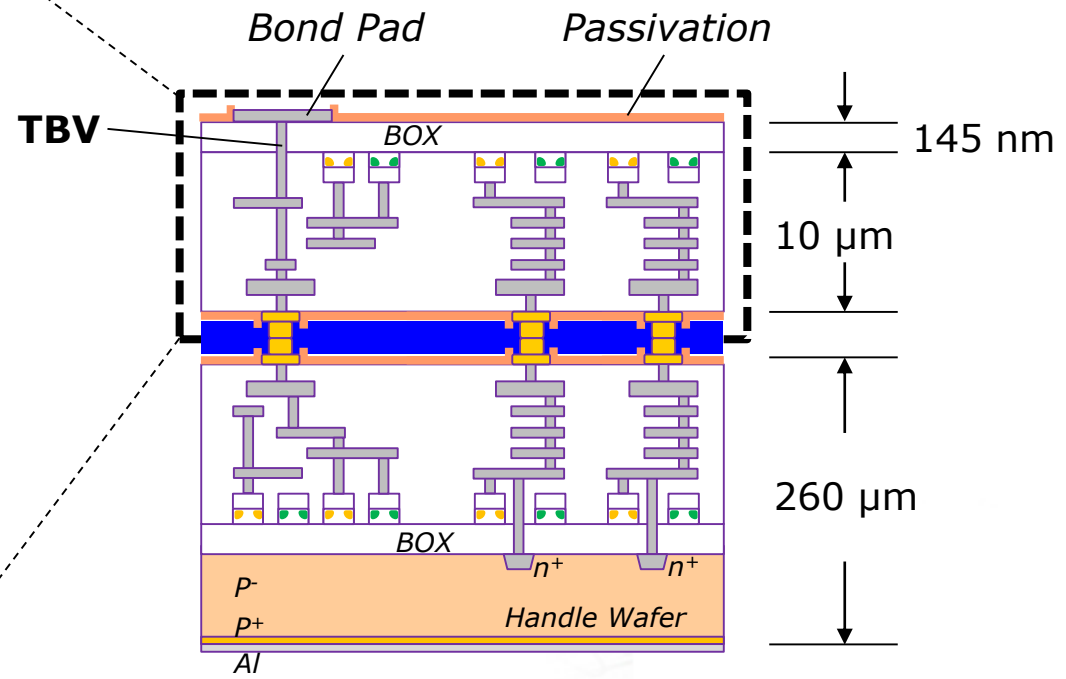
Thinning of Upper tier

- Thinning of the upper tier is very delicate
  - There is nothing but a thin BOX layer (200 nm) on top of the circuit
  - Under-etching and Over-etching must be avoided

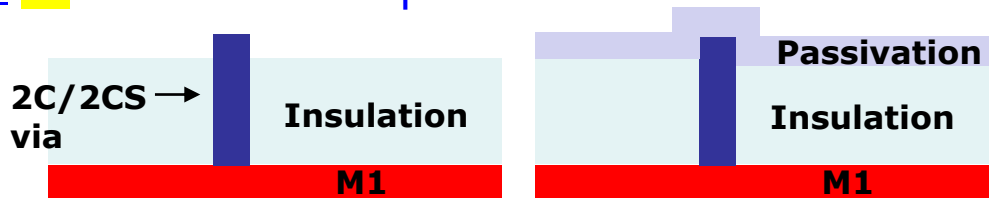


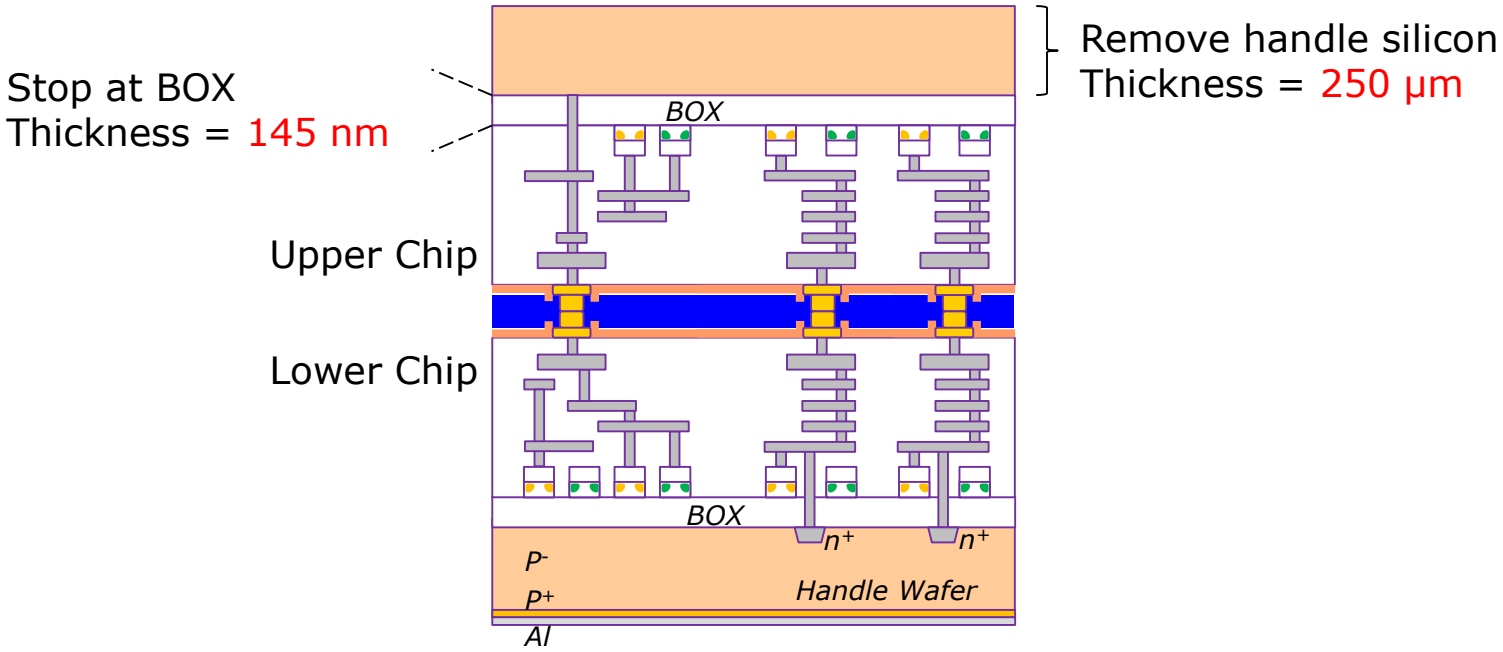
Block diagram of upper tier



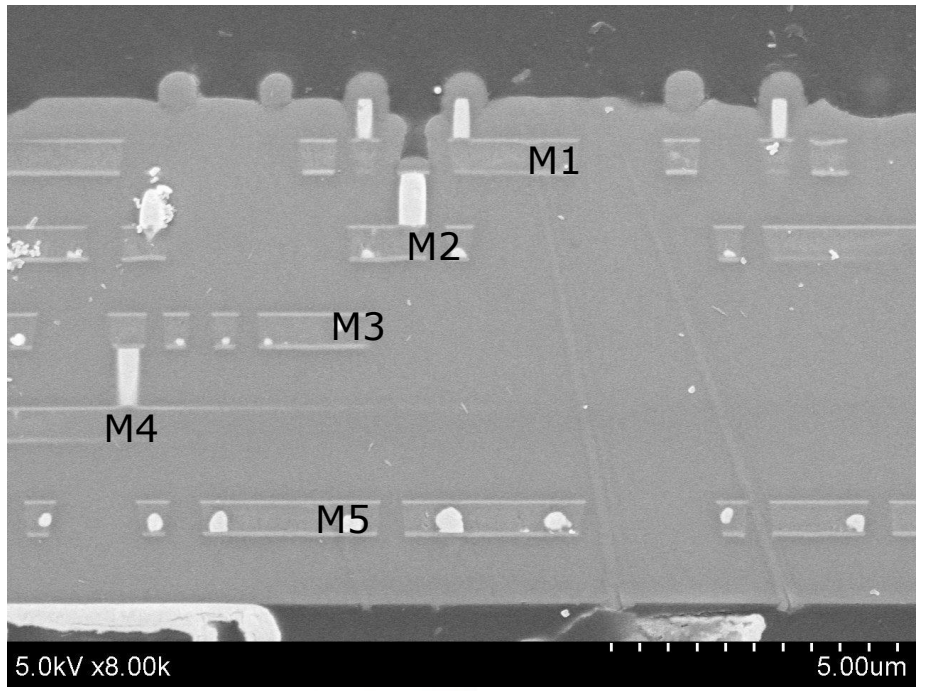
Optimization of backside etching

- Low Resistive wafer is preferred for Upper chip because it is easier for WET etching
  - But CPV-4 Upper chips are from the same High Resistive wafer ☹ as the Lower chips from
  - Grinding (down to 20 μm) + dry etching to avoid over-etching



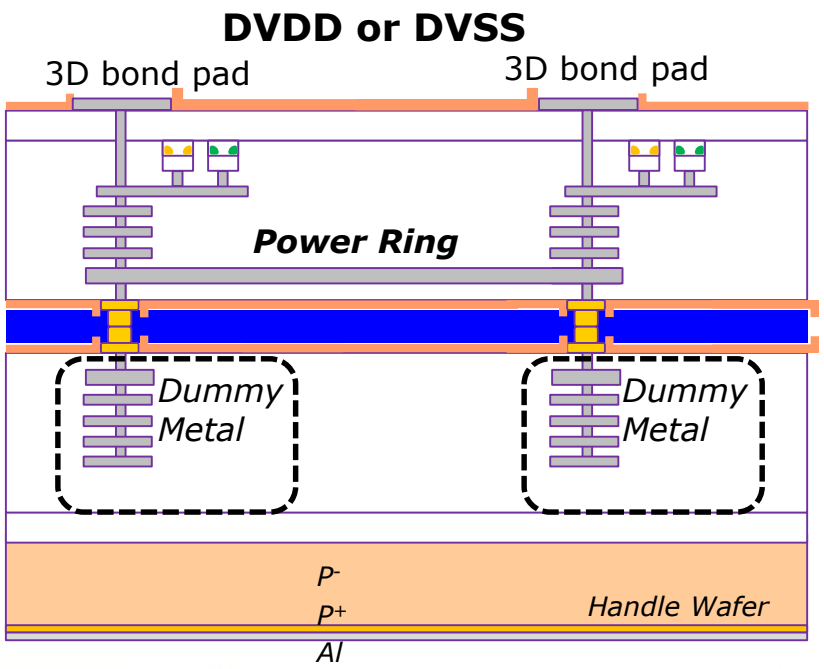


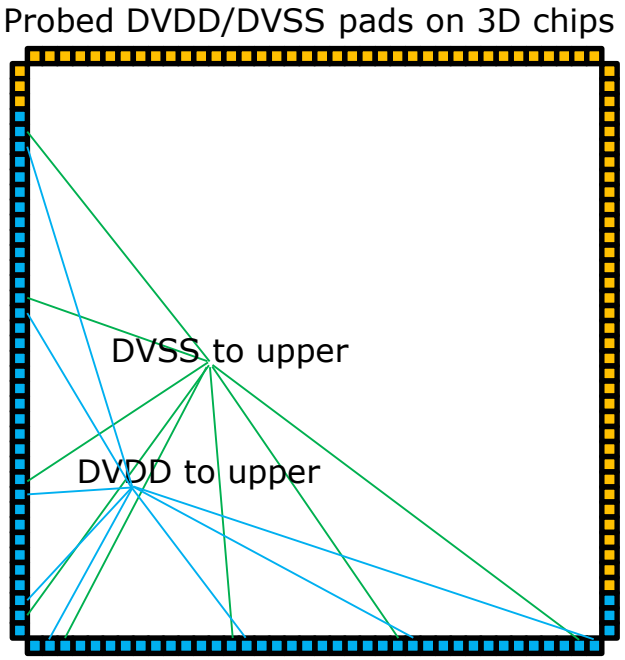
Example of over-etching.
Passivation is not flat on cross-section SEM image

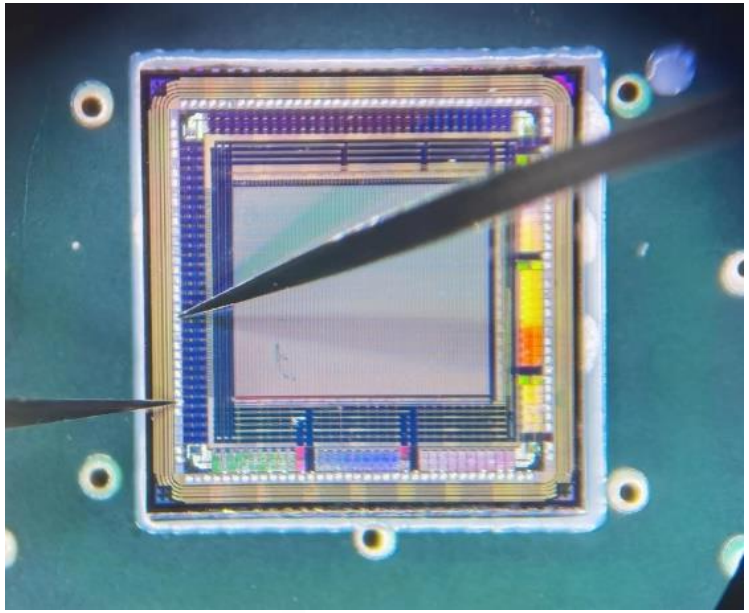


Measurement of 3D connection to upper tier

- Probe test on the 3D chips: from 3D bond pad to **the upper tier**
  - Measure the resistance between two power pads (DVDD) or two ground pads (DVSS)
  - 2 ~ 6 Ω, electrical connection established
  - Yield 100% on 3 tested chips

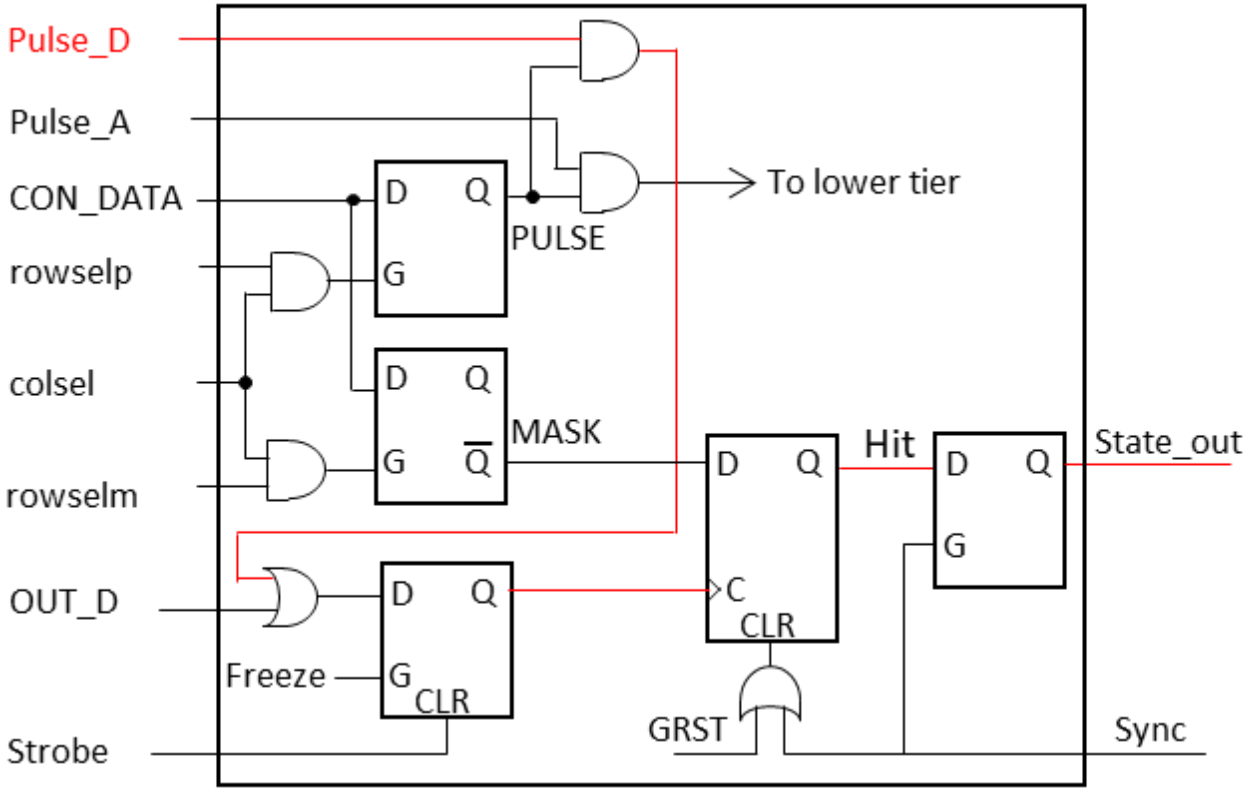




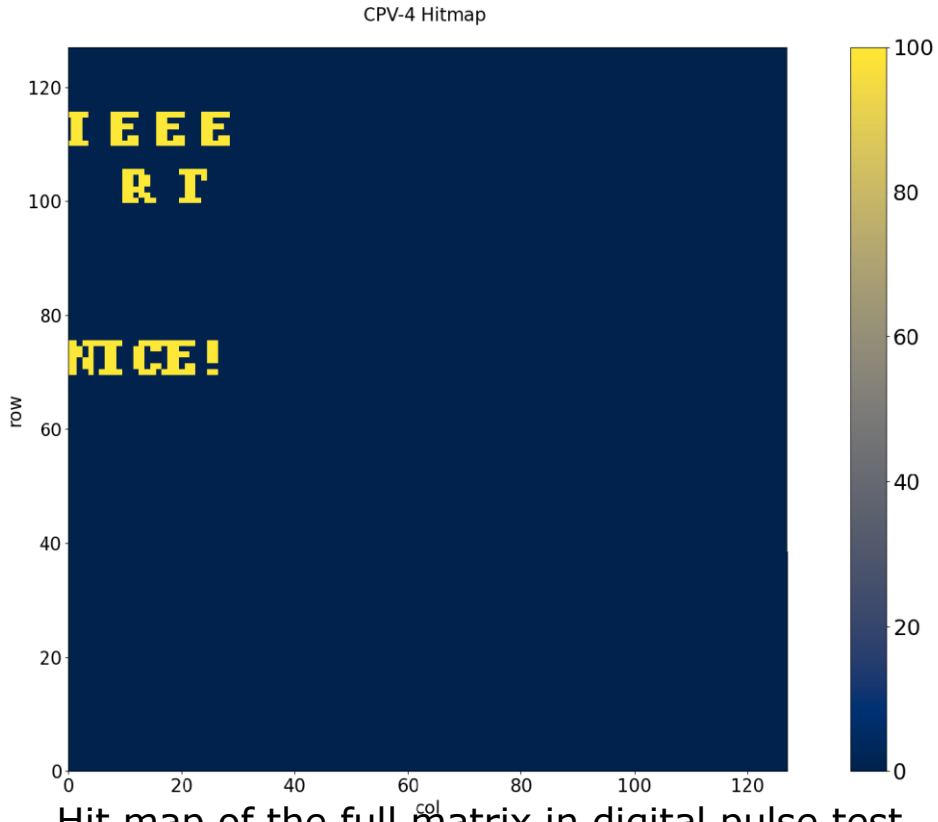


Verification of Upper Tier functionality

- Readout of pixel hit by using digital test pulse as the stimulus
  - Full matrix can be configured per pixel and readout correctly



Digital pixel logic in upper tier, with digital test pulse signal Pulse_D and Hit output signal State_out illustrated.



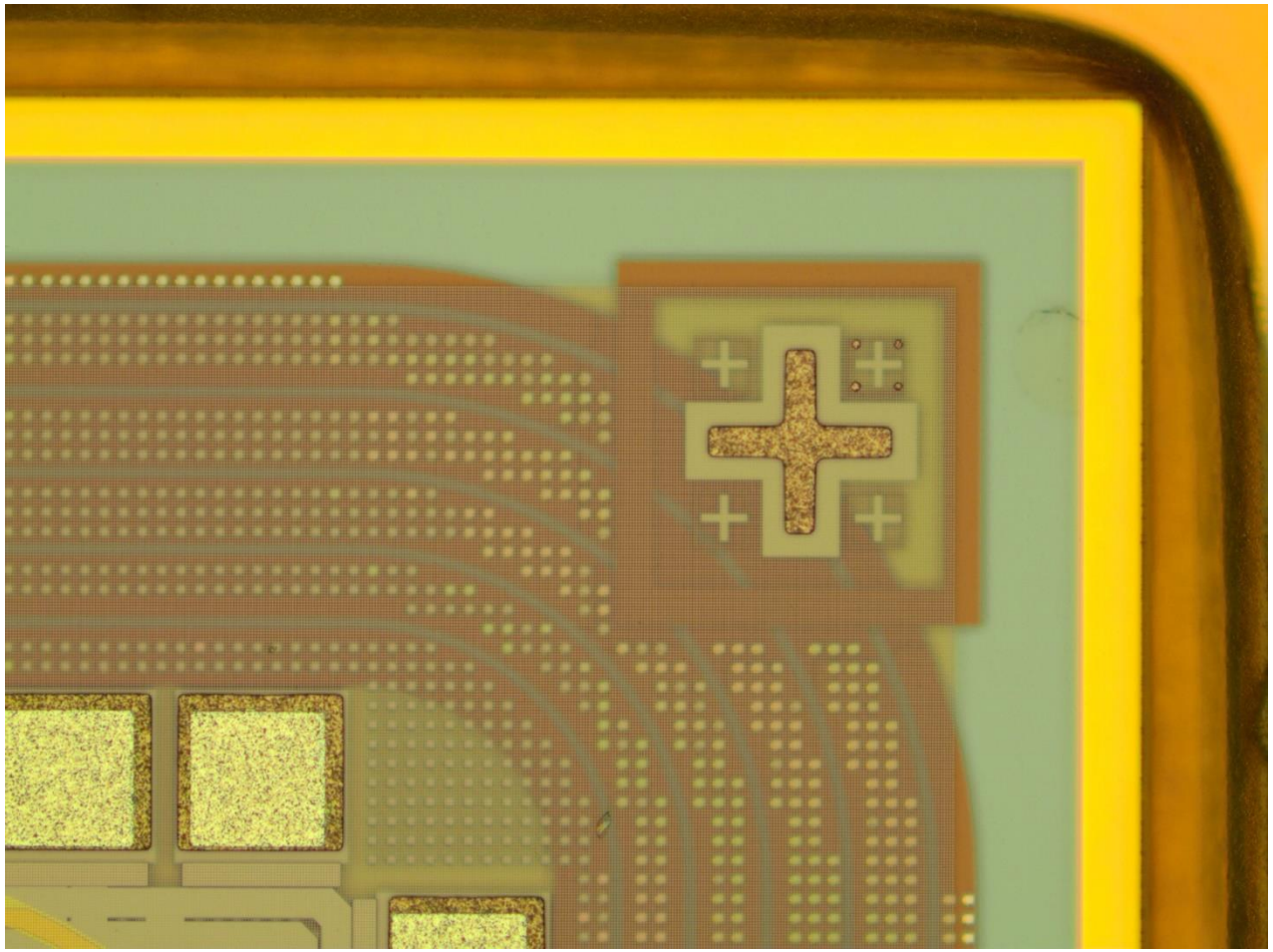
Hit map of the full matrix in digital pulse test, with character patterns illustrated.
Number of test pulses = 100

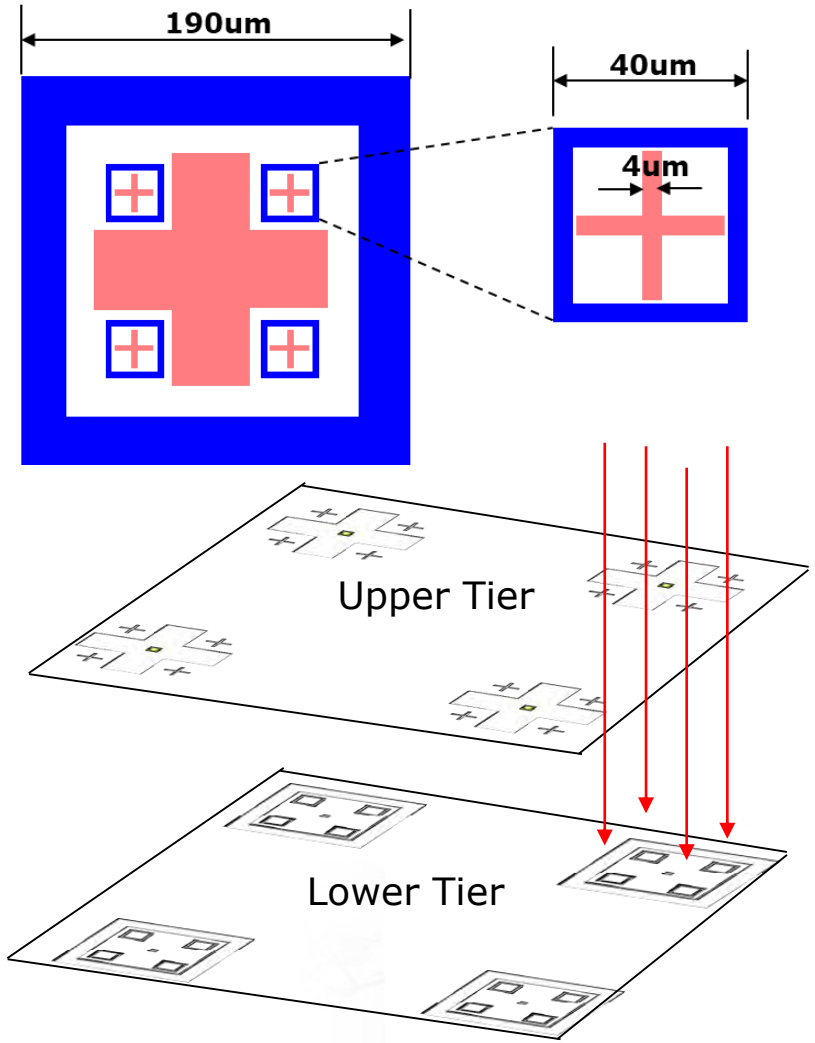
Outline

- Introduction
  - Challenges in vertex detector for future e^+e^- experiment
- Features of 3D-SOI process and CPV-4 design
  - Sensing diode
  - Analog/Digital separation
  - 3D compatibility
- Verification of lower tier
  - Reverse bias voltage
- Verification of upper tier
  - Removal of handle wafer
- Verification of 3D integration
  - connectivity
- Summary and Outlook

Visual Inspection

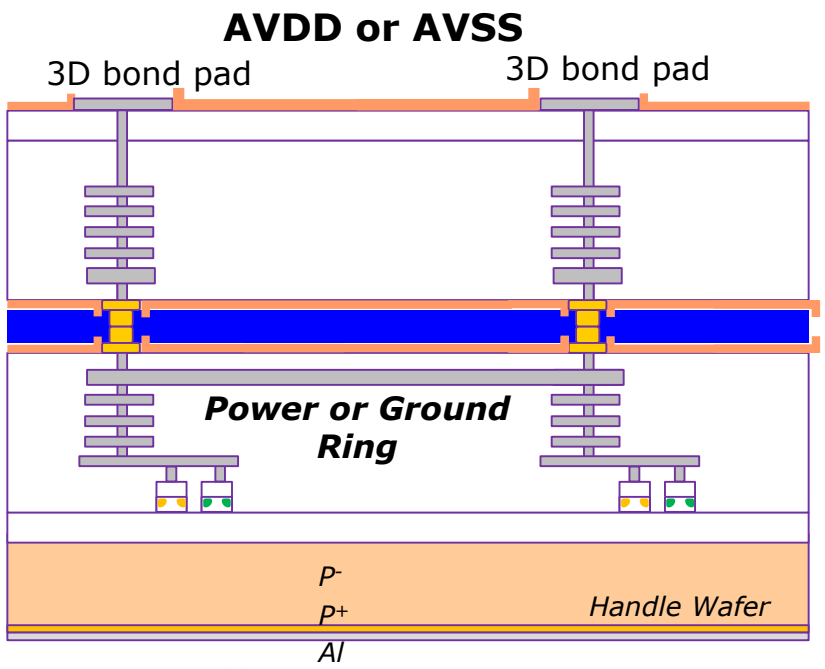
- Chip to chip alignment confirmed on the cross marks, accuracy 1~2 um
  - Dummy bumps can be seen aligned accurately

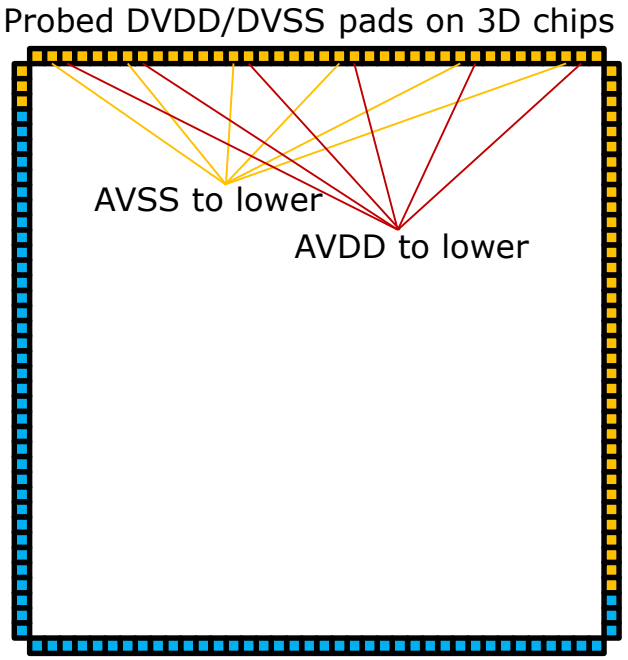


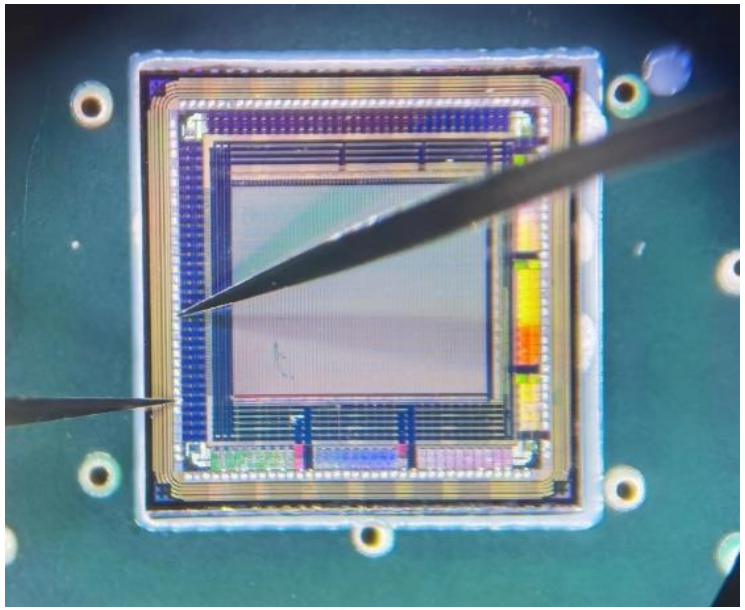


Measurement of 3D connection to Lower tier

- Probe test on the 3D chips: from 3D bond pad to **the lower tier**
  - Measure the resistance between two analog power pads (AVDD) or two analog ground pads (AVSS)
  - ~ 100 Ω, contact resistance included
  - 4 out of 6 tested chips are good

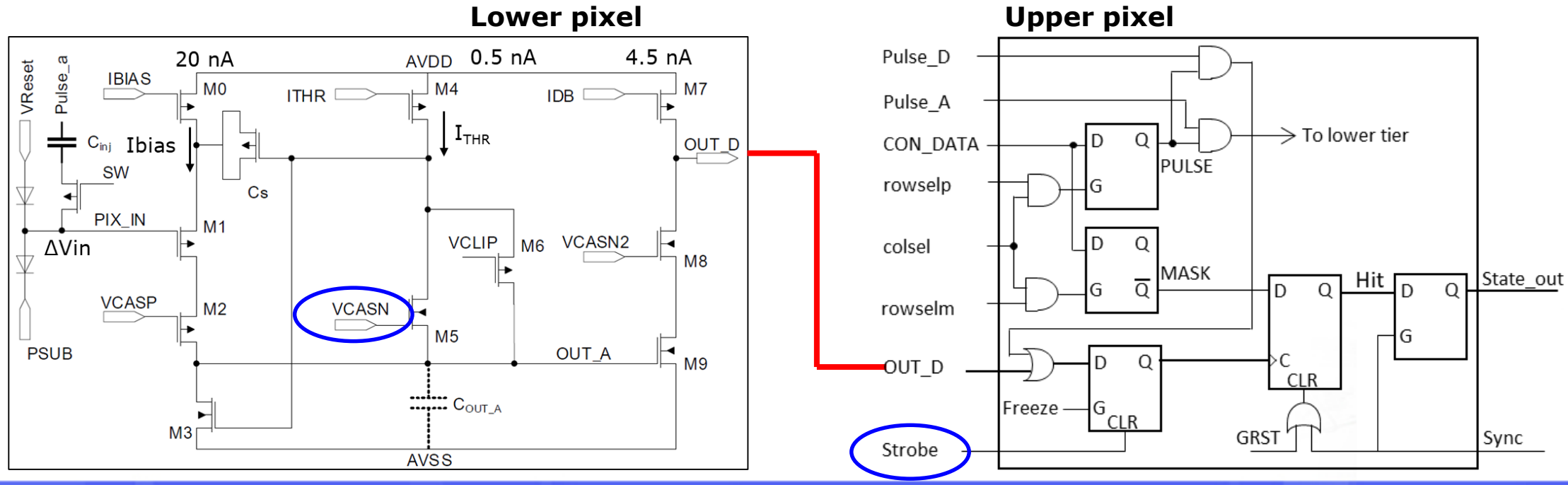






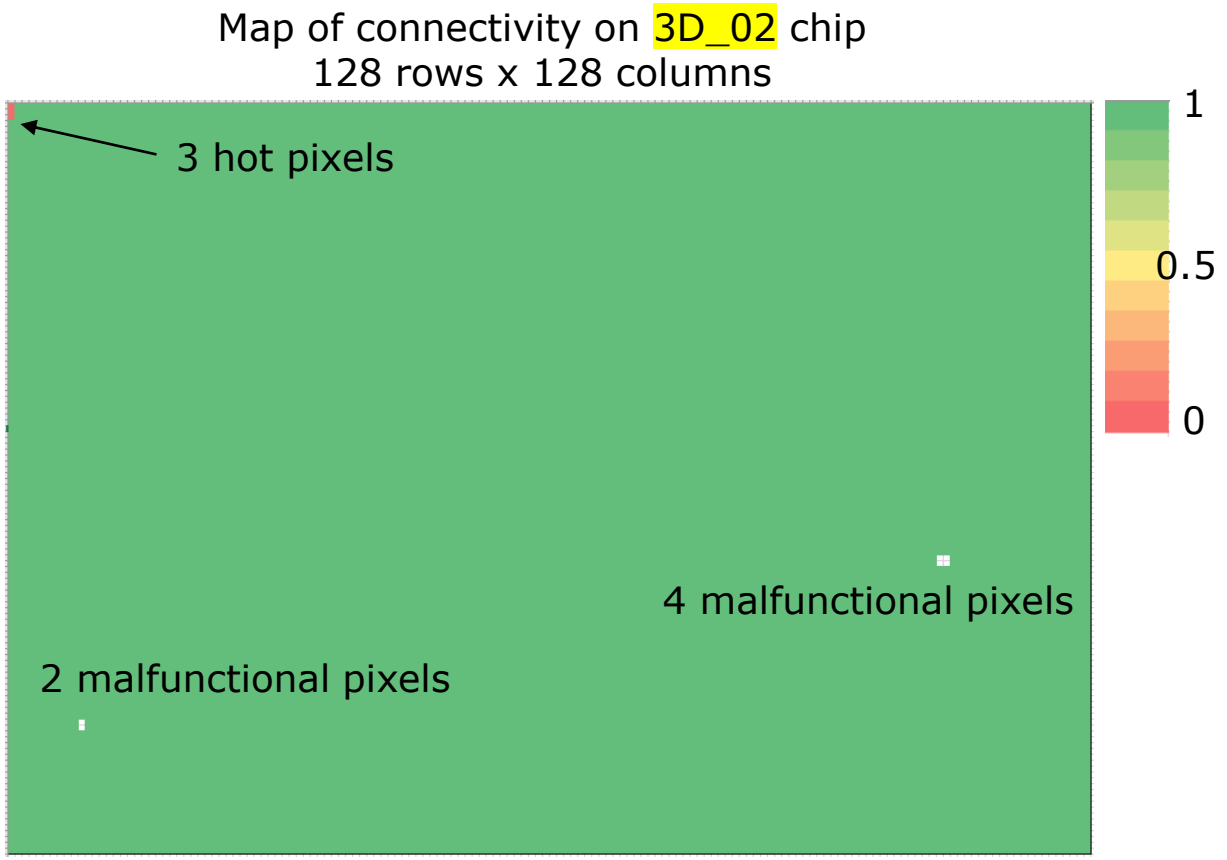
Test of pixel connection

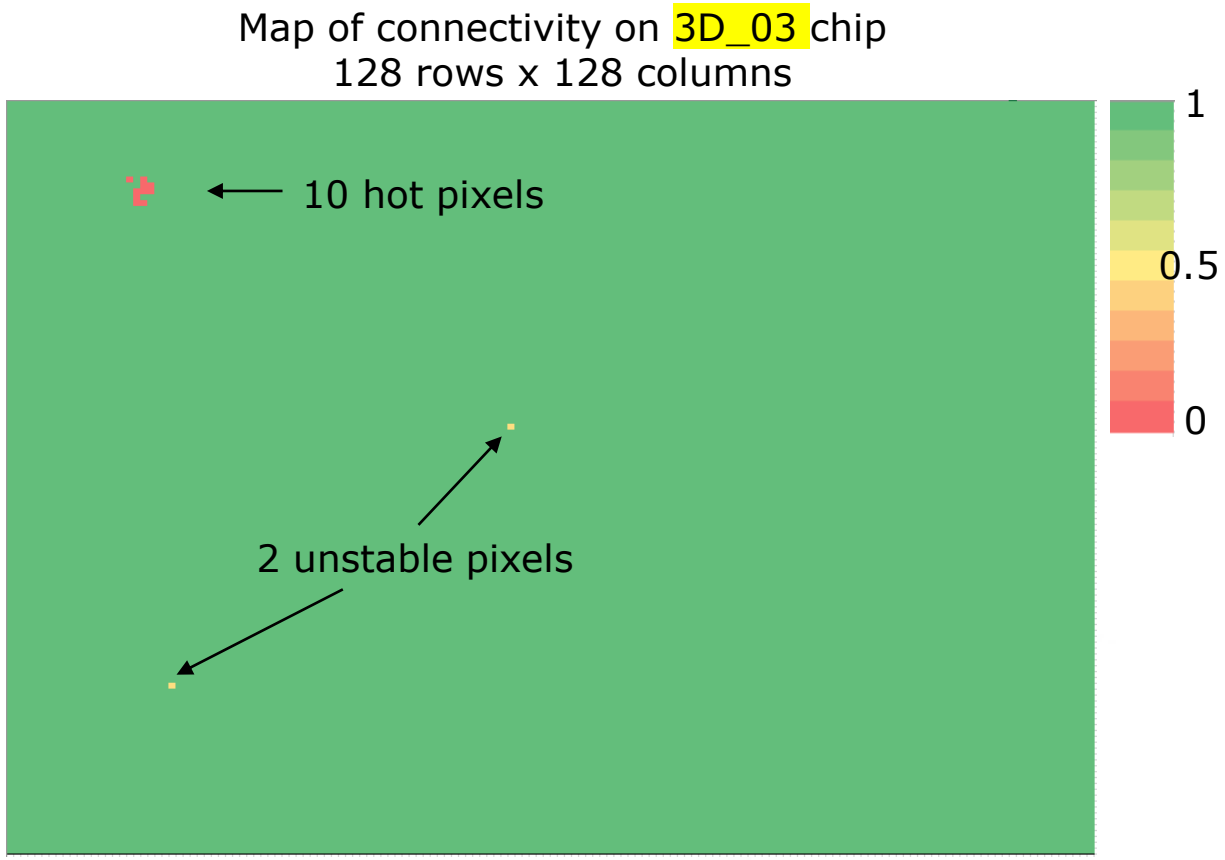
- Each pixel has an OUT_D connection between lower and upper tier
  - Tuning V_{CASN} to define the state of OUT_D (1 or 0)
  - Generate HIT = OUT_D & (!Strobe) by Strobe pulse
  - Connectivity is checked by assigning OUT_D = 1



Connectivity of pixel matrix

- Yield of pixel connection ~ 99.9%
  - Small cluster of hot pixels with HIT = 1 even when OUT_D = 0





Summary and outlook

- 3D chip-to-chip bonding being pursued for high granularity
  - Compatible with the existing SOI process
- First trial of CPV-4 finished
  - Established full chain of sensing and readout functions
- Critical points verified successfully
  - Reverse bias voltage on analog frontend
  - Thinning of handle wafer
  - Vertical connectivity with micro bump bonding
- A short-circuit issue between V_{BPW} and AVSS is found in recent 3D chips
  - Investigation is underway
  - Samples from the same wafer have been identified and will be analyzed

Acknowledgement

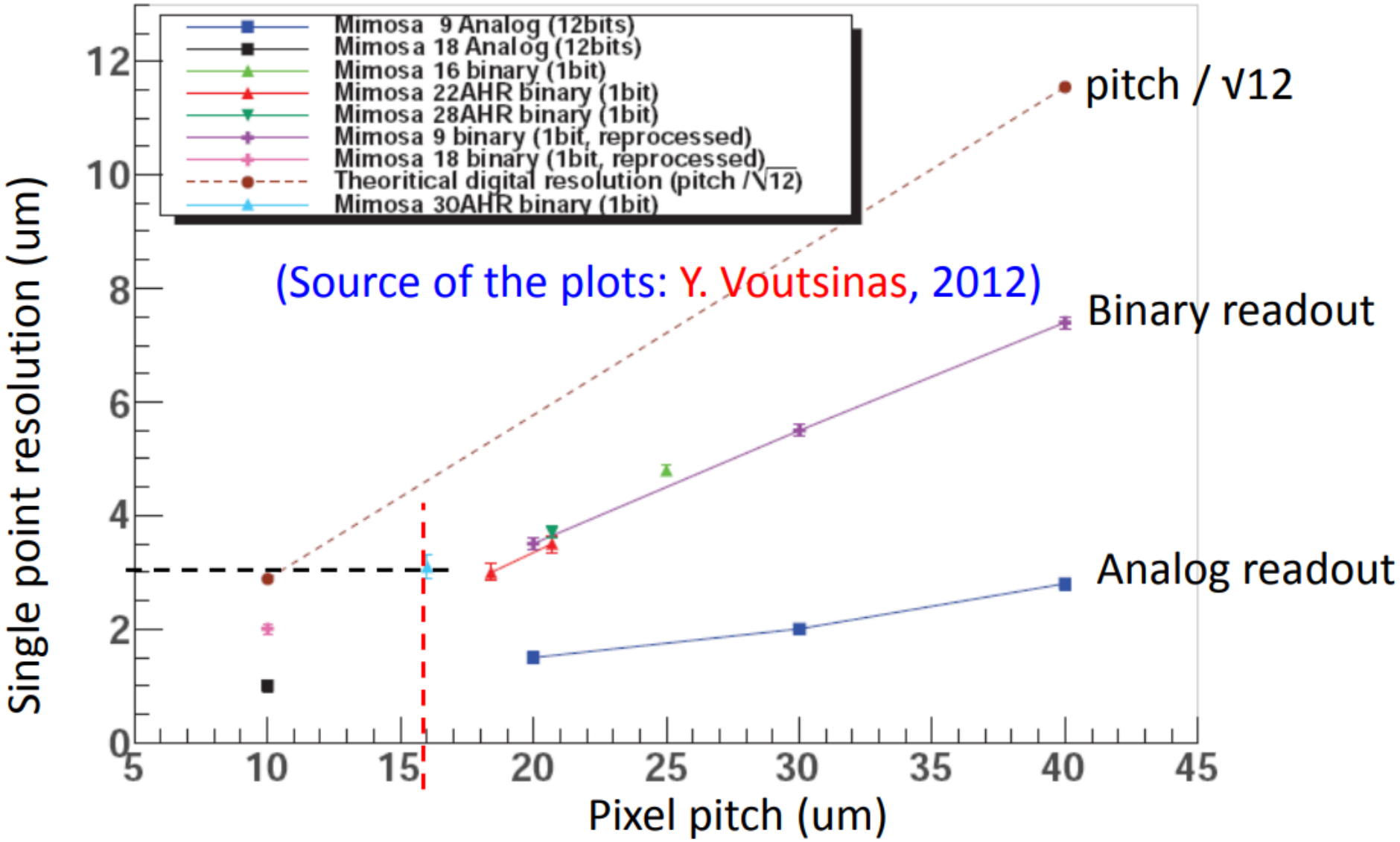
- The SOI pixel detector and 3D bonding process have been developed in the framework of SOIPIX collaboration. The authors thank all the collaborators, especially Ikuo Kurachi, Chiharu Ichitsubo , Makoto Motoyoshi, Miho Yamada and Yasuo Arai.

- This work is supported by the National Natural Science Foundation of China under grant number 11935019, 11575220.

Thanks for your time!

- Backup slides

A survey of high position resolution



Stackup of layers in SOI pixel process