Radiation tolerance and mitigation strategies for the ATLAS muon trigger at the HL-LHC

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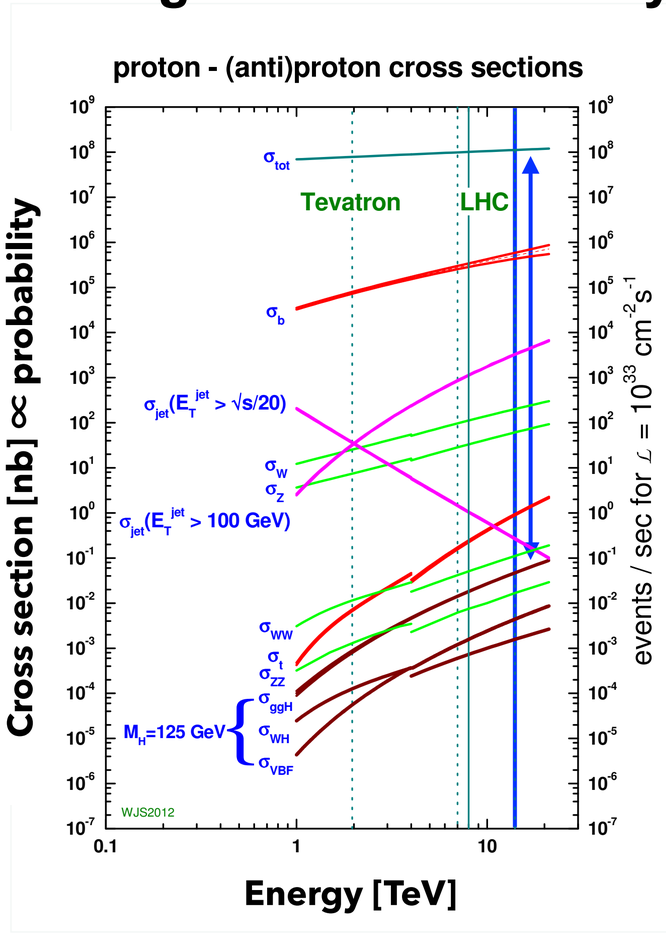
Workshop on Radiation-Tolerant Semiconductors, 22 Jan. 2026

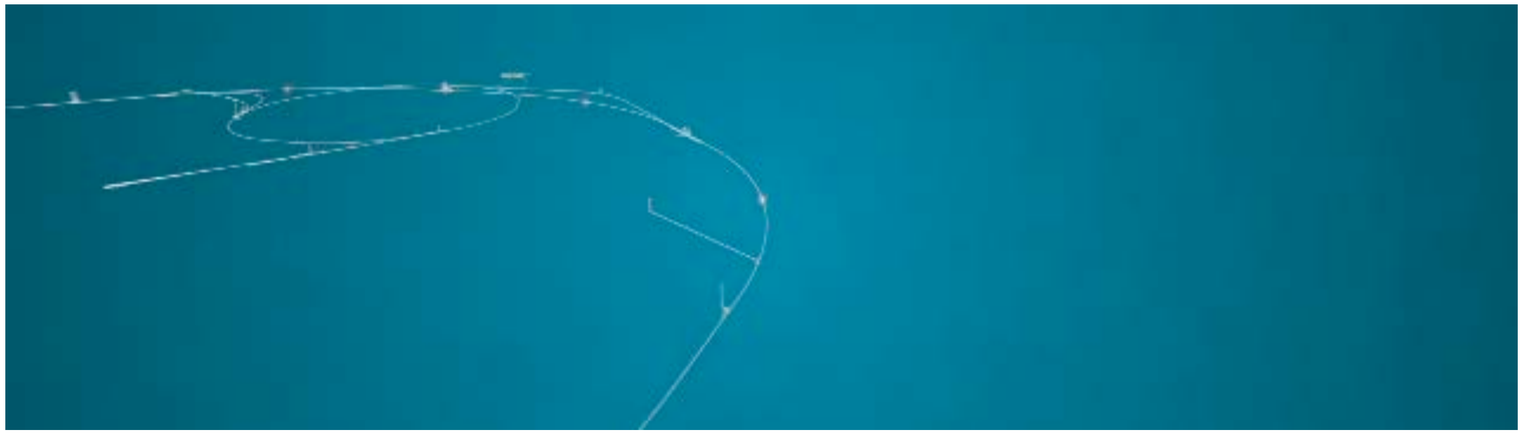
Introduction

In order to study about the Higgs boson and search for new physics,
we collide protons and select interesting collision data (“trigger”) for storage.

Interesting collisions are very rare.



The trigger is crucial for the experiments at LHC/HL-LHC.



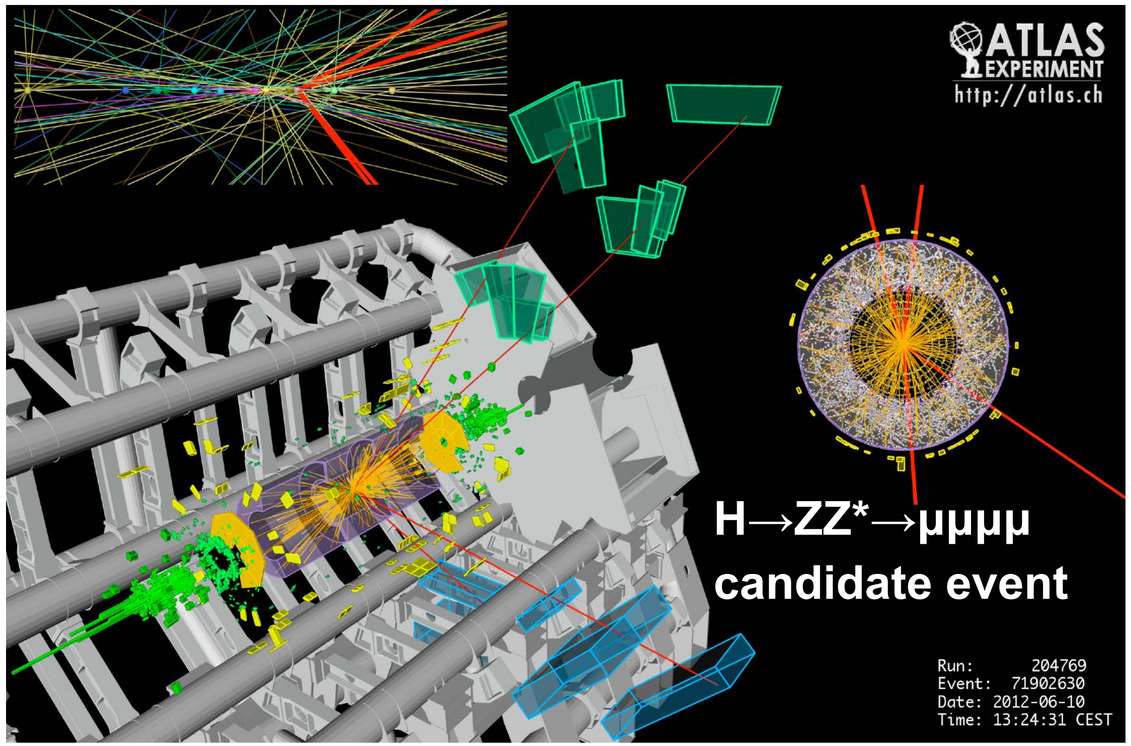
The first level trigger by electronics, with the latency 10 μs at HL-LHC.

CERN ATLAS Experiment, https://videos.cern.ch/record/1951286

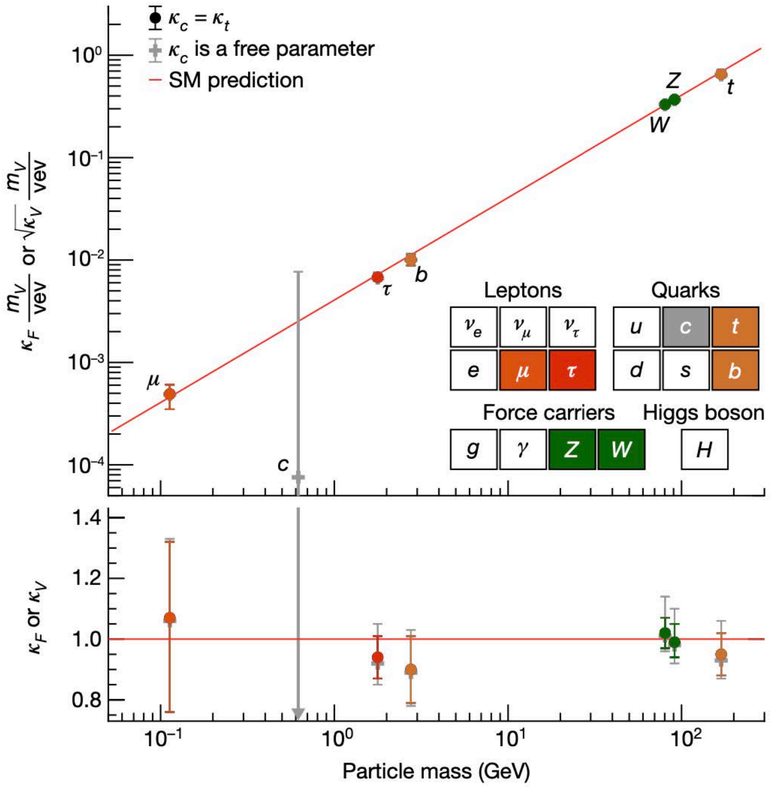
Muon Detection at the ATLAS Experiment

High-momentum muons are a clear signature of interesting proton collisions.

Essential for the Higgs boson observation in 2012!



Most Higgs measurements rely on muons.



Nature, 607, 52 (2022)

Thin Gap Chamber (TGC)

TGC plays a role of fast muon detection and momentum measurement for trigger

- Multi-wire proportional chamber operated in a saturated mode
- High voltage: 2800 V
- Gas: 55% CO_2, 45% n-pentane
- Two-dimensional position measurements using wires and strips
- Number of layers: 7
- Channel widths: O(1 cm)
- Number of channels: 320k

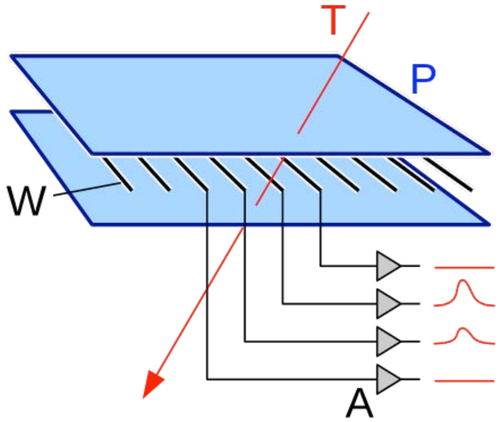
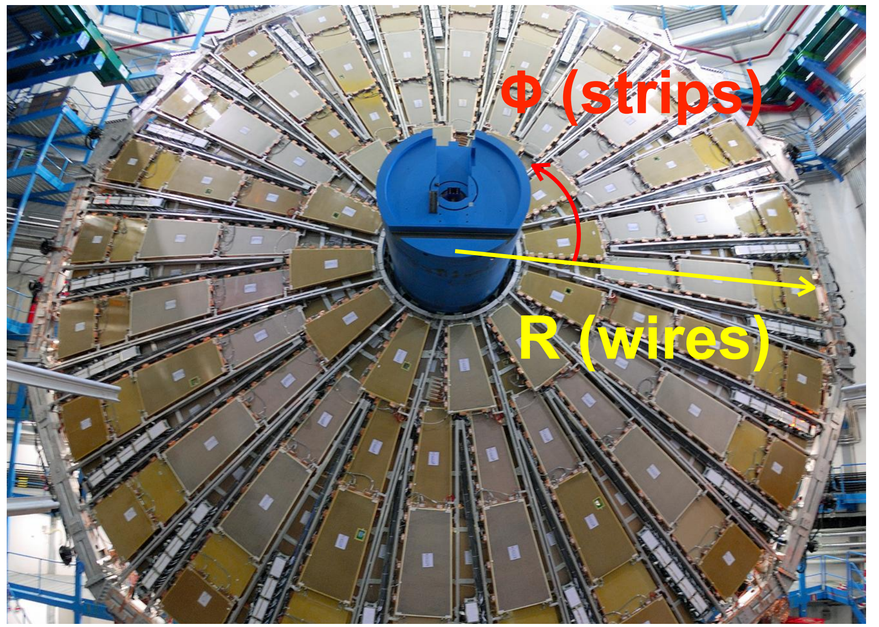


Image of wire chamber from Wikipedia (CC BY-SA 3.0)



Overview of the TGC System at HL-LHC

The TGC electronics will be upgraded toward HL-LHC.

Instantaneous luminosity:
5-7.5 x 10^{34} $cm^{-2}s^{-1}$
Integrated luminosity:
3000-4000 fb^{-1}

~1 order higher than LHC!

Concept: send all hit data to off-detector and reconstruct muons with advanced FPGA

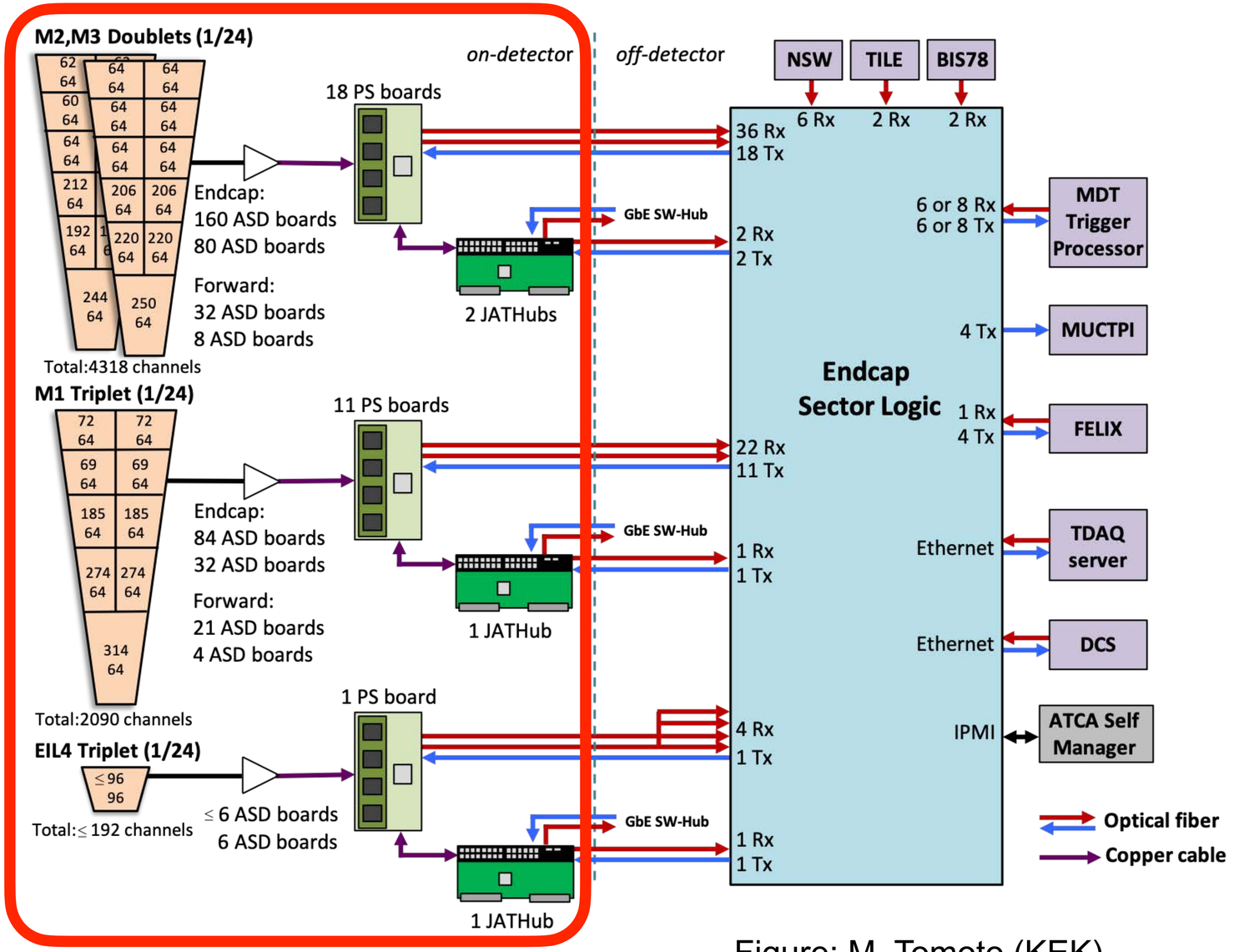


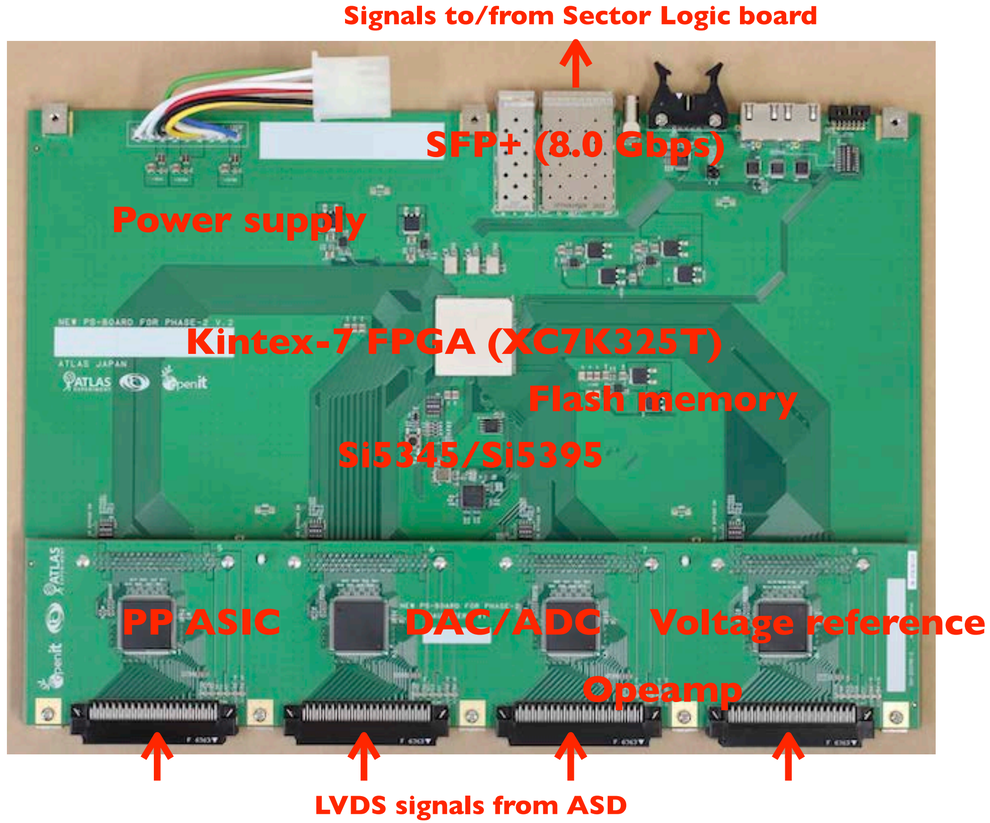
Figure: M. Tomoto (KEK)

in radiation area

TGC Boards in the Radiation Area

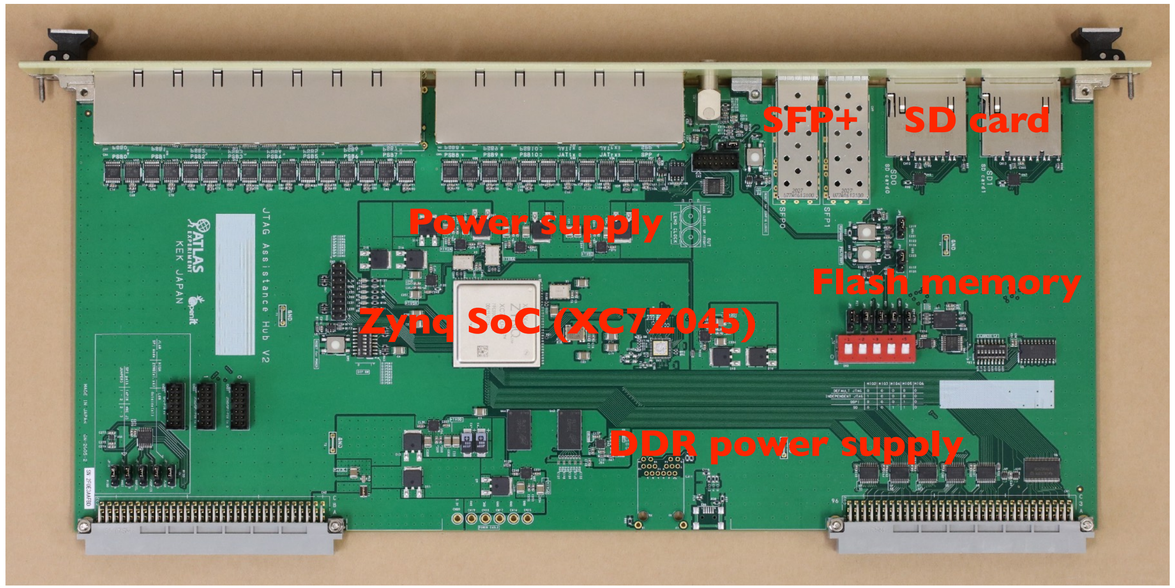
PS board

Collect the signals from ASD boards and transfer to off-detector electronics



JATHub board

Configure PS boards, measure the PS board clock timing, and recover the PS board when multi-bit SEU is observed



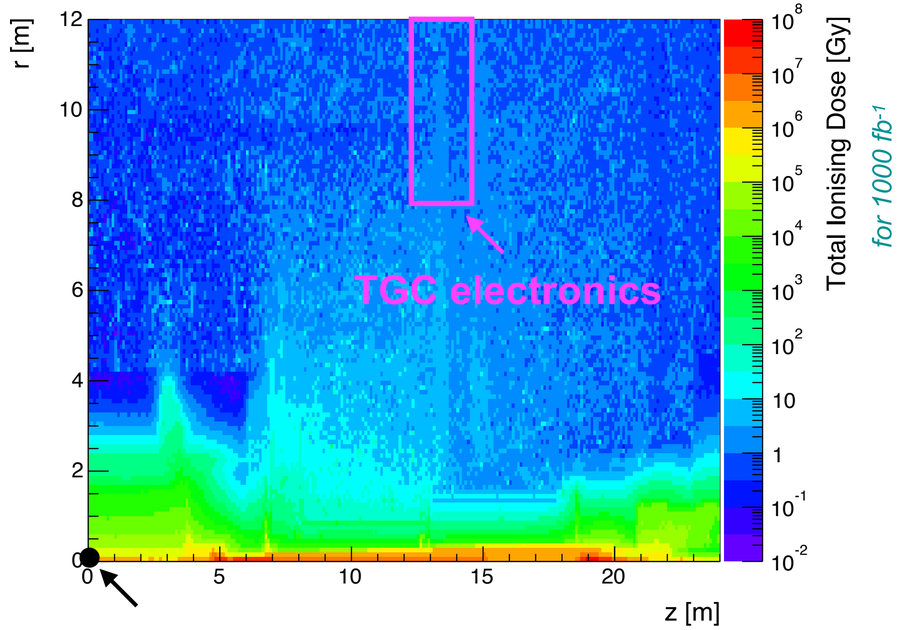
Concept: fully exploit commercial off-the-shelf (COTS) electronics components, after careful studies of the radiation tolerance

Requirements for the Radiation Tolerance

Requirements: the simulated dose/flux multiplied by three types of safety factors

Simulation (example)

Total Ionising Dose (TID)
6 Gy for PS boards at 4000 fb^{-1},
with minor updates later



Safety factors [TDR]

	SF_{sim}	SF_{test}	SF_{lot}
From 2013	1.5 (TID), 2 (NIEL/SEE)	1-5 (TID), 1 (NIEL/SEE)	1-4
From 2020	1.5	1 (TID), 1-5 (NIEL/SEE)	1-3

- SF_{sim}: safety factor for simulation uncertainty
- SF_{test}: safety factor to take into account the difference between the tests and actual radiation environments
- SF_{lot}: safety factor for the difference among the lots and individual components inside the lot

Example (FPGA, TID, before 2020 update): 1.5 x 5 x 4 = 30

SF_{lot} = 1 when multiple chips are tested for the final lot/reel

Requirements for TGC Electronics and Tests

Total Ionising Dose (TID)

Requirement: up to 180 Gy

Test: gamma irradiation

Non Ionising Energy Loss (NIEL)

Requirement: up to 1.6×10^{12} n/cm^2

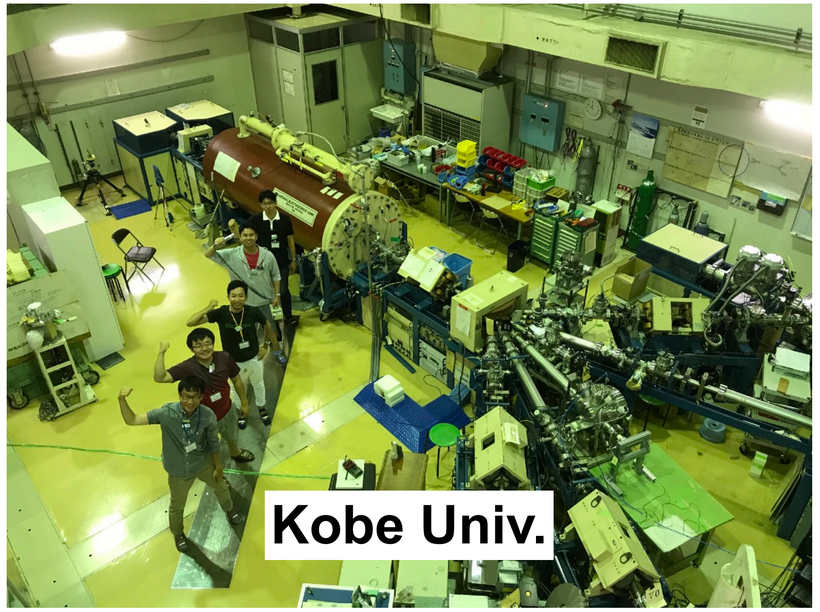
Test: neutron irradiation

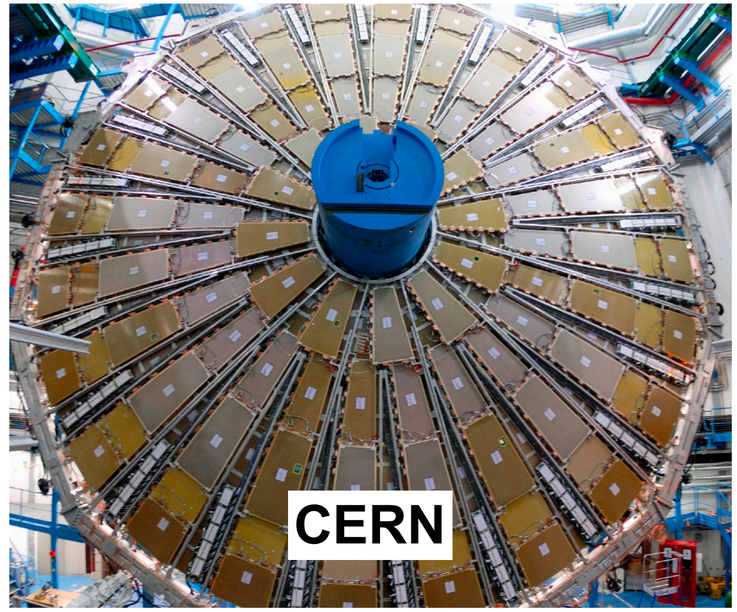
Single Event Effects (SEE)

Estimation: 9.8×10^2 /cm^{2}s ($L = 7.5 \times 10^{34}$ /cm^{2}s)

Test: hadron irradiation

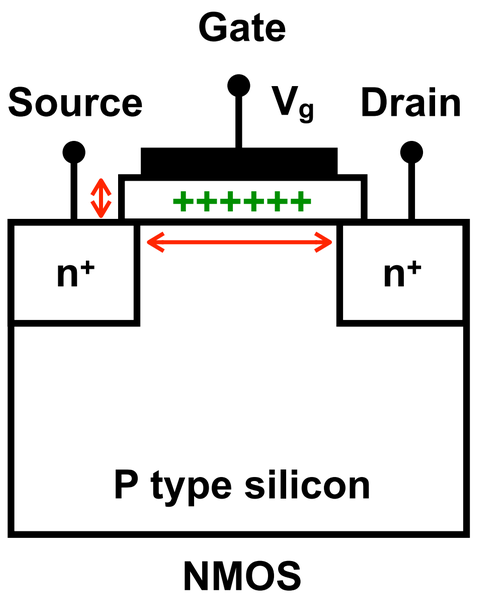
Demonstration: in the TGC detector area





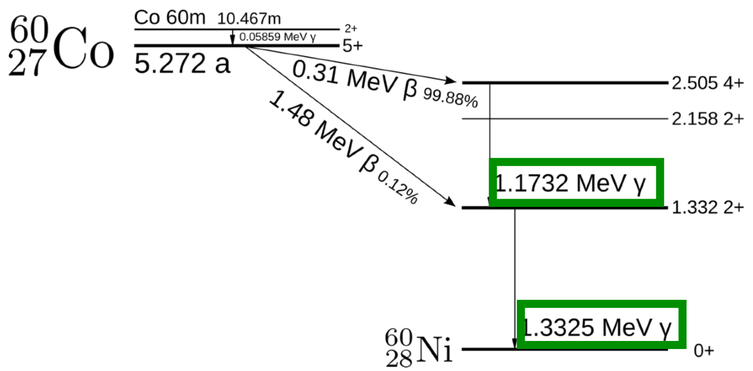
TID — Major Effects and Test Facility

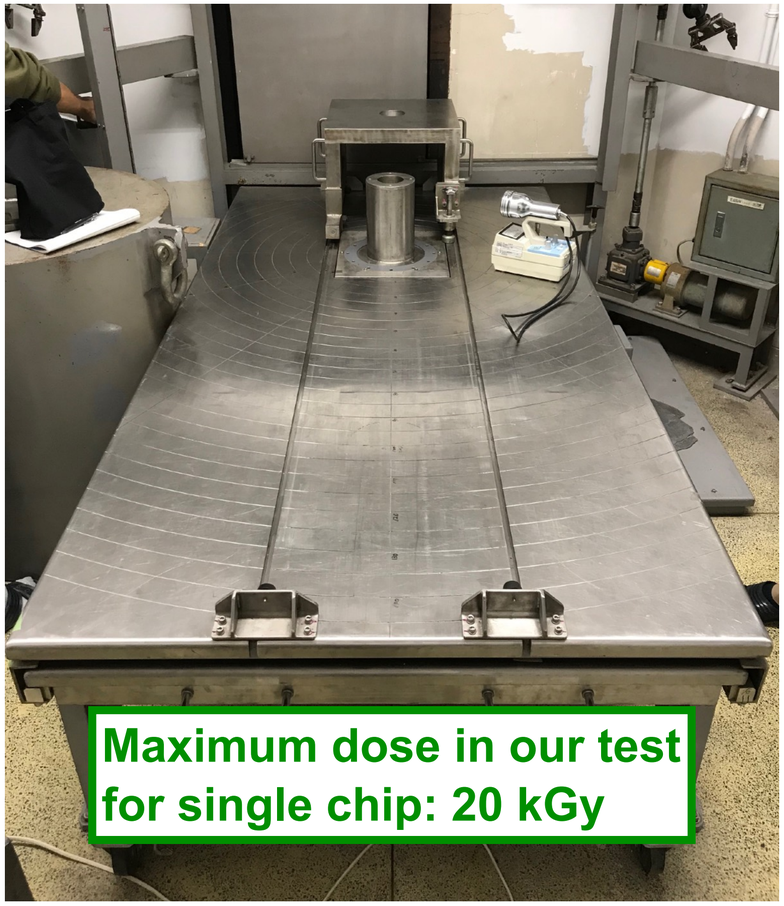
The I-V characteristics of MOSFETs affected by **charge trapping**



The ratio of gate length to gate oxide thickness crucial, strong process dependence

The effects studied at **the Cobalt-60 facility of Nagoya Univ.**

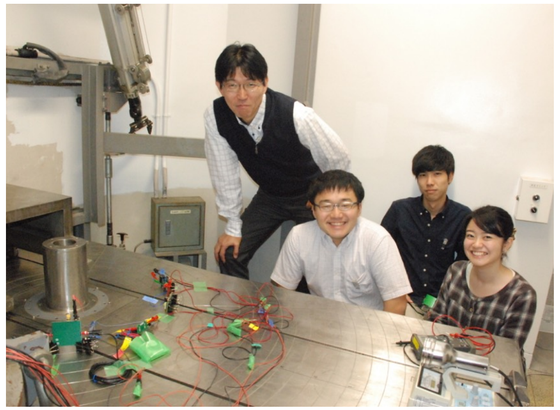




TID — History of the TID Tolerance Tests

2016 — **10 years, > 20 members** — 2025

Tests for chip selections



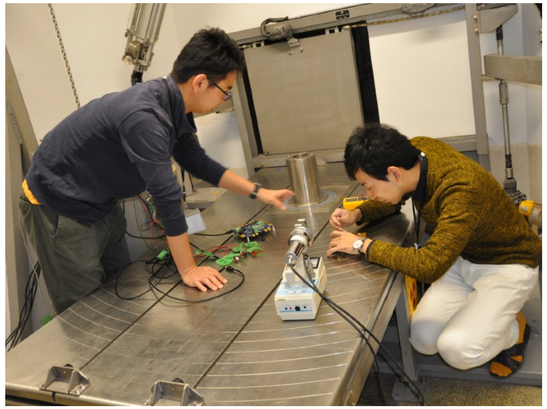
FPGA
PP ASIC
DAC
ADC
Power supply
Voltage Ref.

Study of lot-to-lot variations

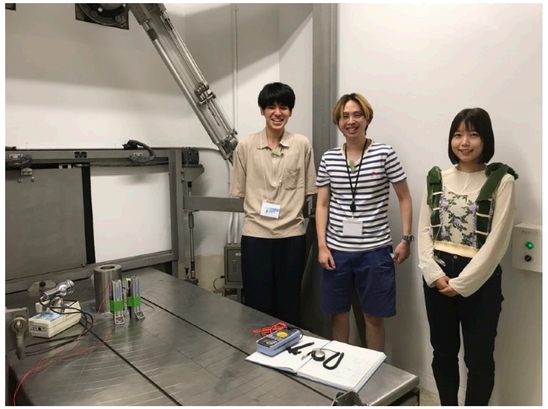
Voltage Ref.
SD card
LDO (DDR)
Opeamp

Confirmation for the final components

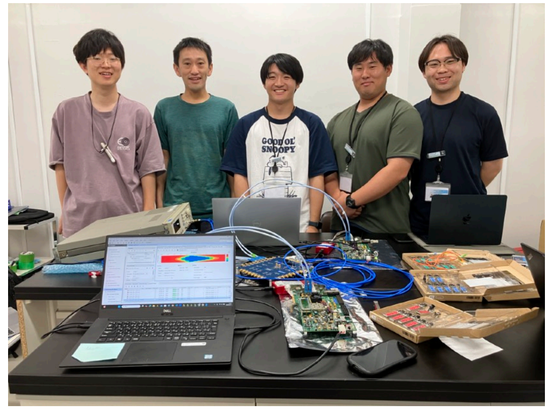
SFP+



DAC
ADC
Power supply
Voltage Ref.
Si5345
SD card
Flash memory
SFP+
LDO (DDR)



Si5395
SFP+
Fiber
Flash memory
PS board



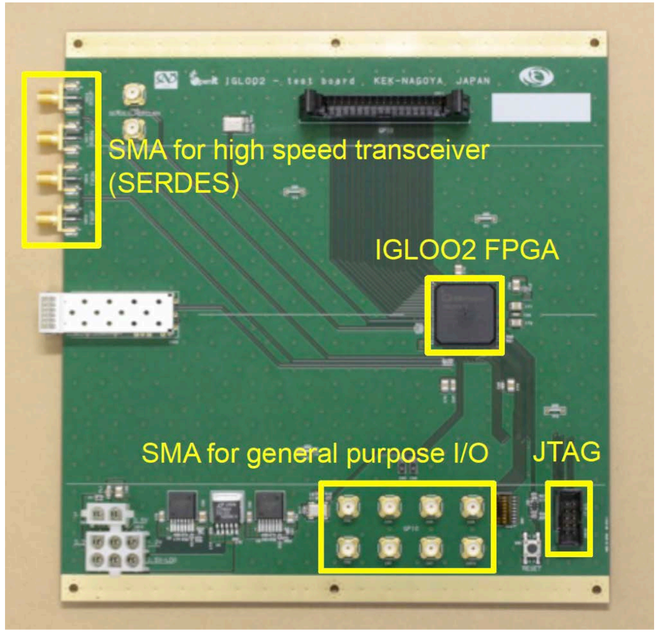
SFP+

TID — Flash-Based FPGA

FPGA with flash-based configuration memory is robust for SEU.
On the other hand, we need to carefully check the TID tolerance.

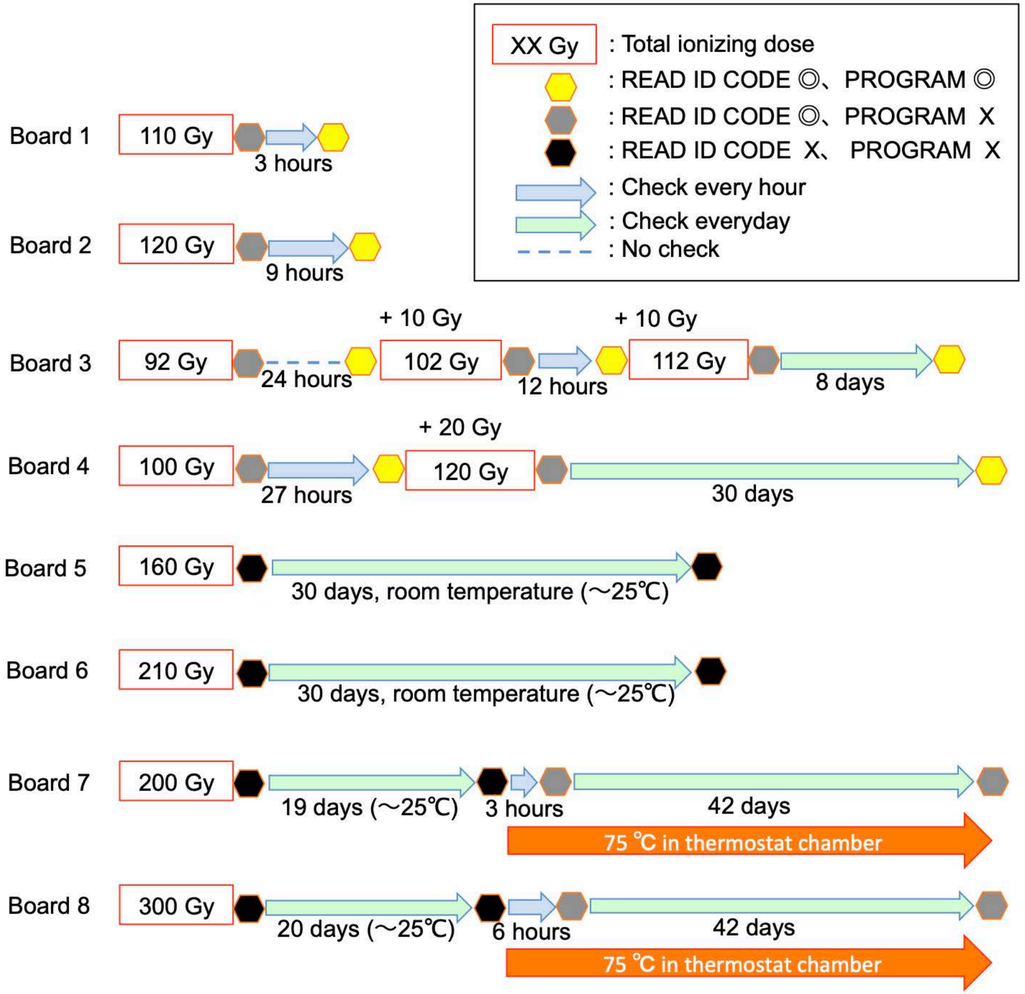
We focused on **Microsemi IGLOO2 FPGA**.
We evaluated performance with evaluation kit.

We developed TID test boards
with **minimal components on board.**



TID — Flash-Based FPGA

Configuration failed at ~100 Gy



All functionalities fine until configuration failure

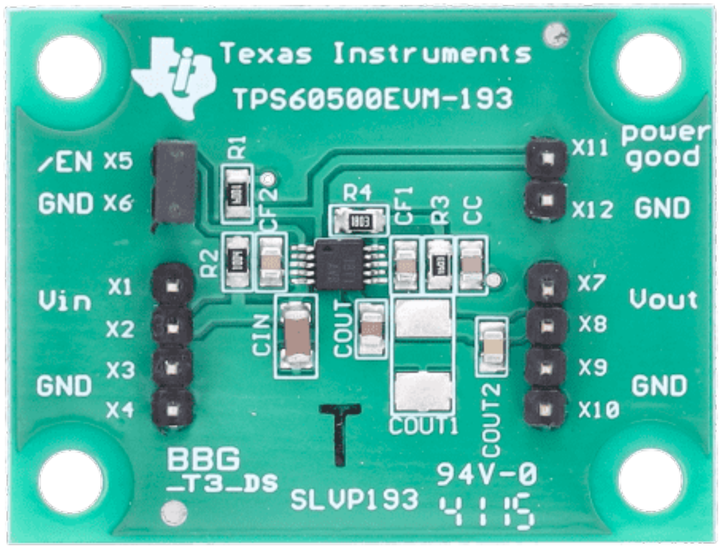
- Power consumption: unchanged
- Transceivers: working well (4 Gbps)
- Ring oscillator with NAND gates: frequency change only by ±1%

Due to lower TID tolerance of IGLOO2 FPGA (and lower data transfer rate of transceiver), we decided to use AMD SRAM-based Kintex-7 FPGA — SEU discussed later

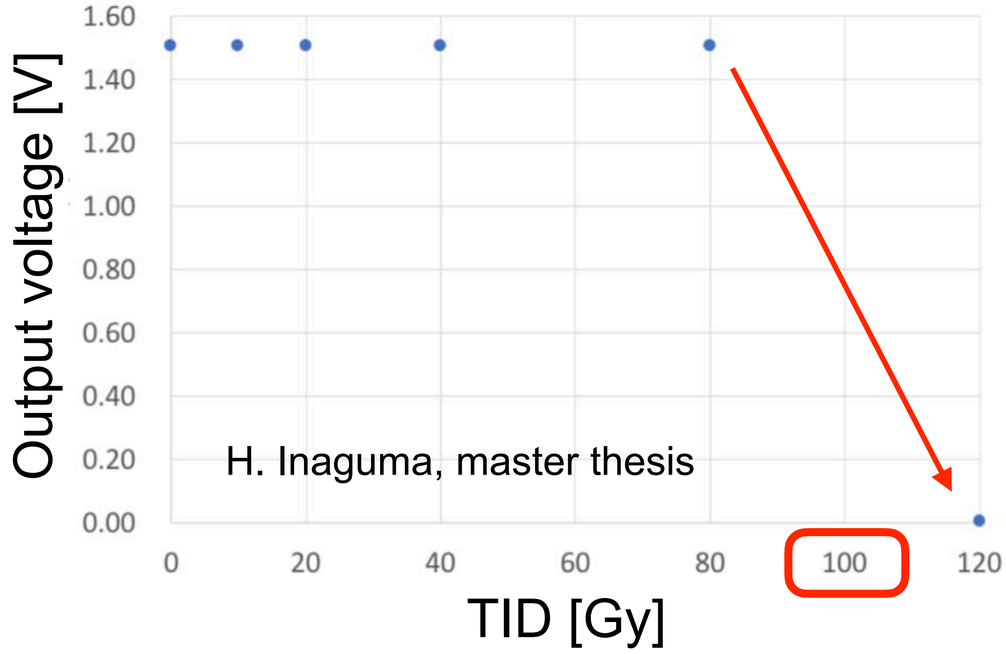
TID — Power Supply Chips

DC/DC convertors has relatively high power conversion efficiency.
On the other hand, they are generally sensitive to TID.

We tested TPS60500 DC/DC convertors on the evaluation kit.



Output voltage dropped at ~100 Gy



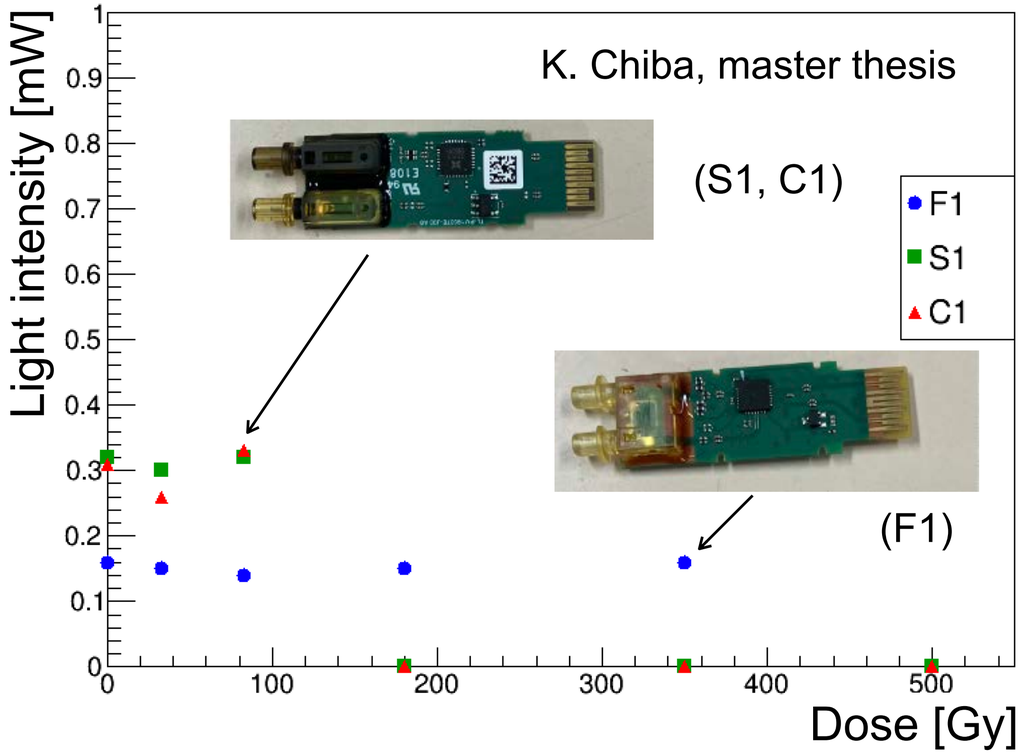
We decided to use voltage regulator TPS7A85 (TID tolerance >240 Gy).

TID — SFP+ Transceiver

For SFP+, we observed significant difference for different manufacturers and lots.

Example is shown for SFP-10GSR-85.

- **Outside the same**
- **Inside and tolerance different**

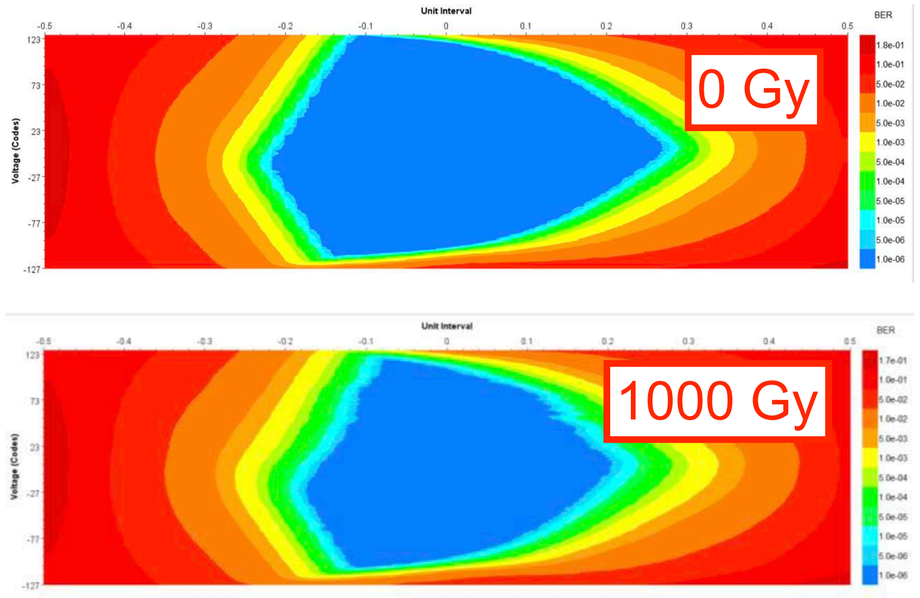


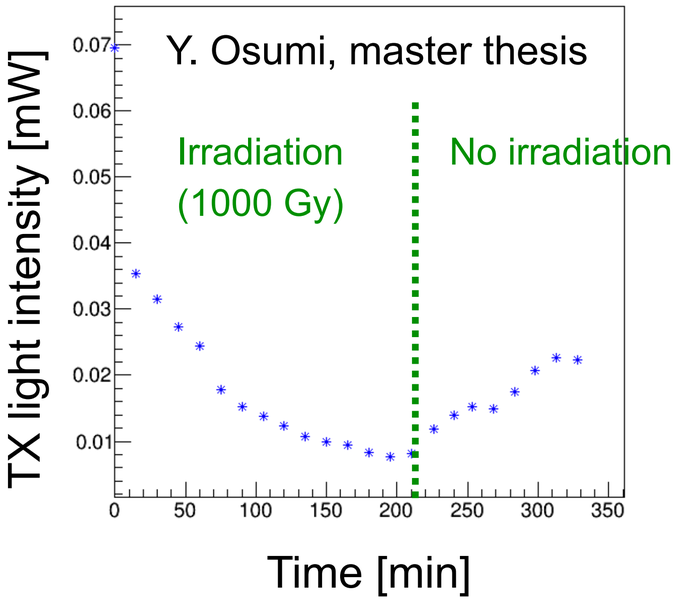
We purchased all (4000) modules from single lot to better control the TID tolerance!

TID — Optical Fibre

The optical fibres generally have higher TID tolerance.

As the optical fibres are the core of our system, we performed TID tests.





The loopback data transfer worked even after irradiation of 1000 Gy.

We observed **attenuation** and (continuous) **recovery** [S. Girard et al., Reviews in Physics], **negligible impact for our system** (~6 Gy expected at 4000 fb^{-1}).

TID — Summary of Component Tests

Type	Model	Number of tested	Requirement [Gy]	Confirmed [Gy]
Voltage reference	REF2025	10	11	800
Voltage reference	REF5040	10	33	240
Voltage reference	REF5025	10	33	240
SD card	SDSDAF3-008G-I	10	18	400
Operational amplifier	LM7322MM/NOPB	20	11	2600
Clock jitter cleaner	Si5344	5	33	240
Clock jitter cleaner	Si5395	3	33	100
QSPI flash memory	MX25L12845GM2I-08G	11	11	100
SFP+ transcivier	Broadcom AFBR-709SMZ	11	33	490
SFP+ transceiver	Coherent FTLX8574D3BCV	10	33	250
SFP+ transceiver	Coherent FTLX8573D3BTL	1	33	240
SFP+ transcivier	Ficer FSPP-H7-M85-X3D	10	33	200
SFP+ transcivier	FS SFP-10GSR-85	17	11	83
Optical fiber	1-LC.P-LC.P-GI(PE-A10G)-DF-N-500	2	33	1200
LDO	TPS7A85	10	33	240
LDO for DDR	TPS51200	7	18	240
ADC	ADS7953	10	33	180
DAC	DAC7678	10	33	180

For the requirement, the latest values, updated after most of the tests, are shown.

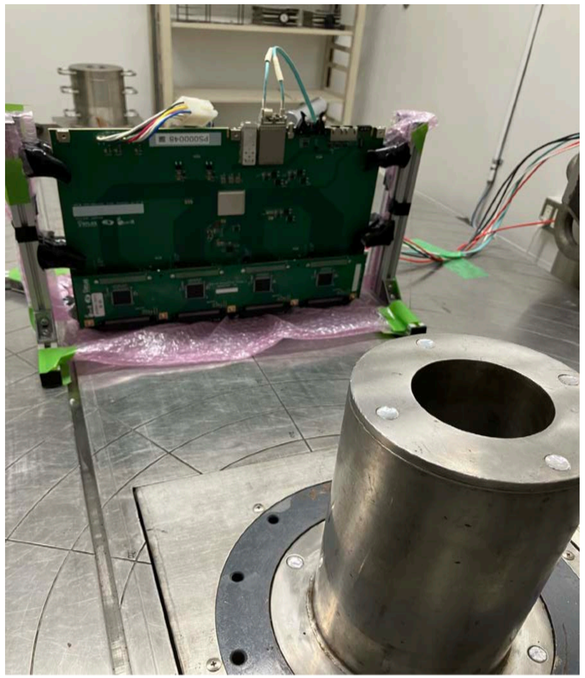
For the confirmed, the highest dose for which no failure was observed is shown for the worst tested components.

We conducted intensive testing on various electronics components and identified those that meet the requirements!

TID — Test for the Final Board

For the confirmation of the TID tolerance of **all components from the final lots/reels**, **an entire board was irradiated** (33 Gy).

The configuration, reconfiguration, interfaces, clocking, and functionalities were **fully confirmed with the QC system**.



NIEL — Major Effects and Test Facility

Displacement damage from nuclear interactions can lead to reduced gain and increased leakage current in bipolar transistors.

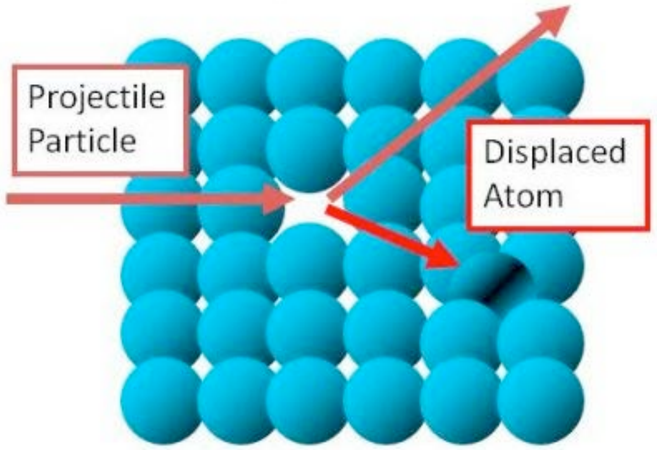
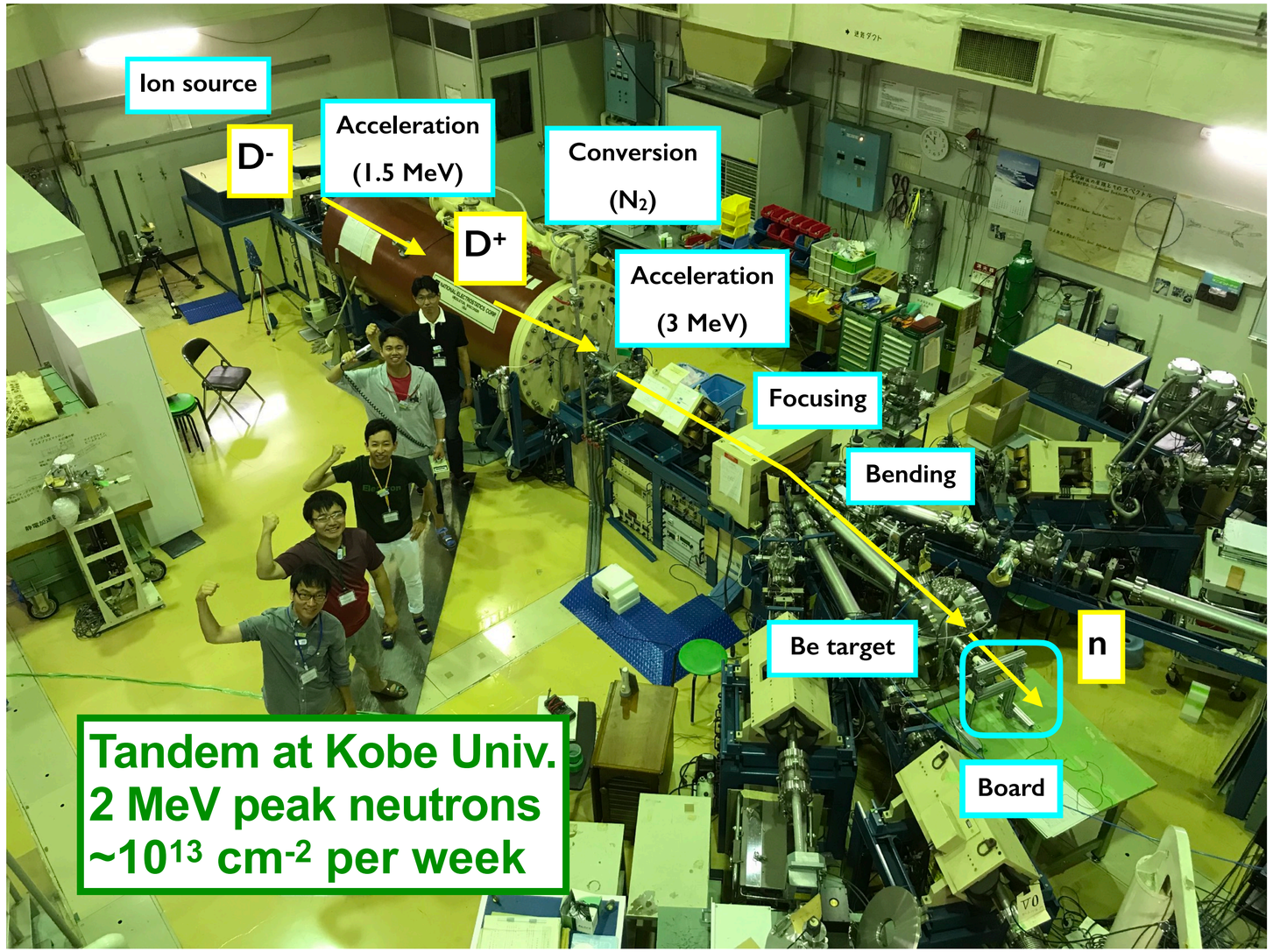
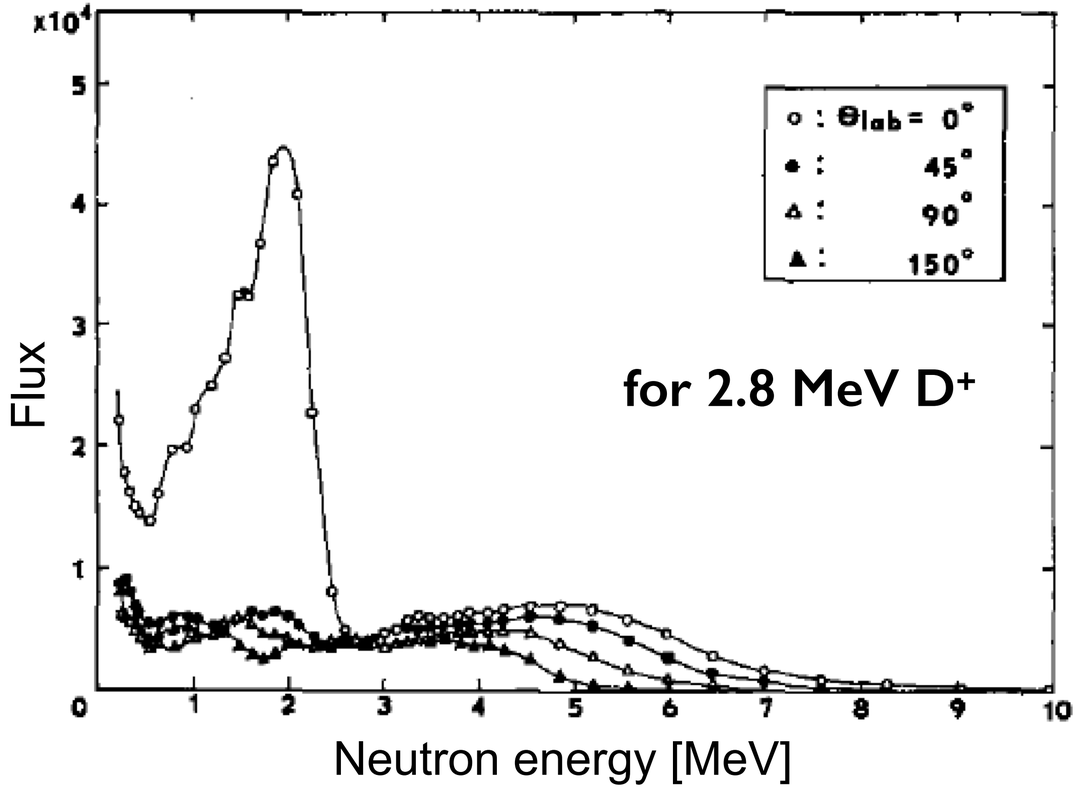


Image from https://semiconductor.altertechnology.com/radiation-testing/displacement-damage-testing-and-mechanisms/



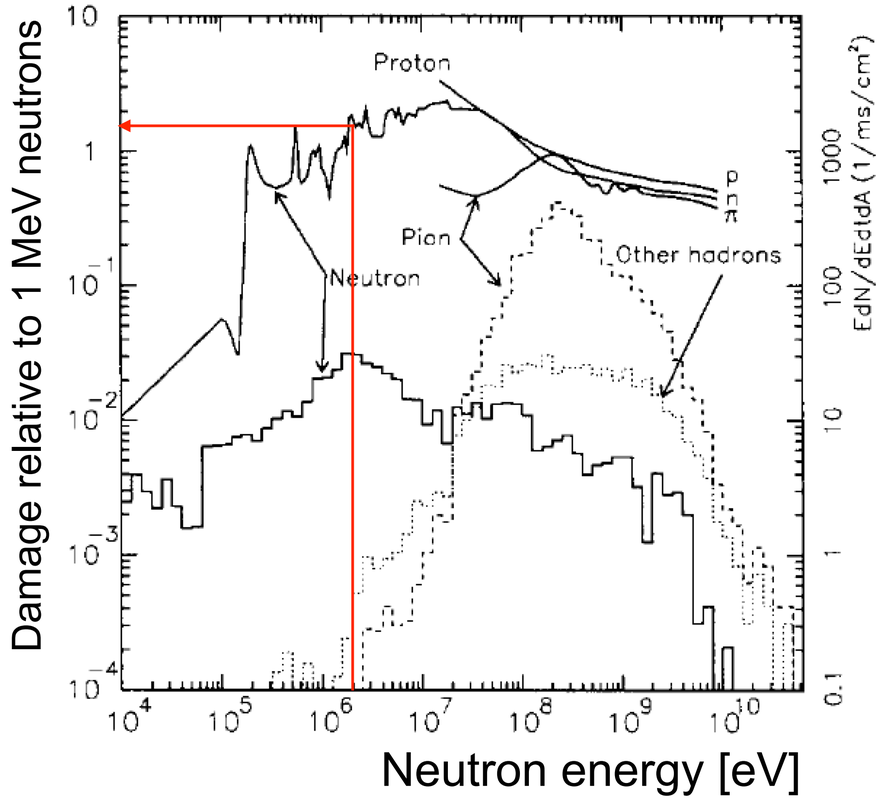
NIEL — Tandem Neutron Energy and Damages

Journal of Nuclear Science and Technology 5, 22 (1968)



Peak at around 2 MeV

NIMA 335 (1993) 580-582

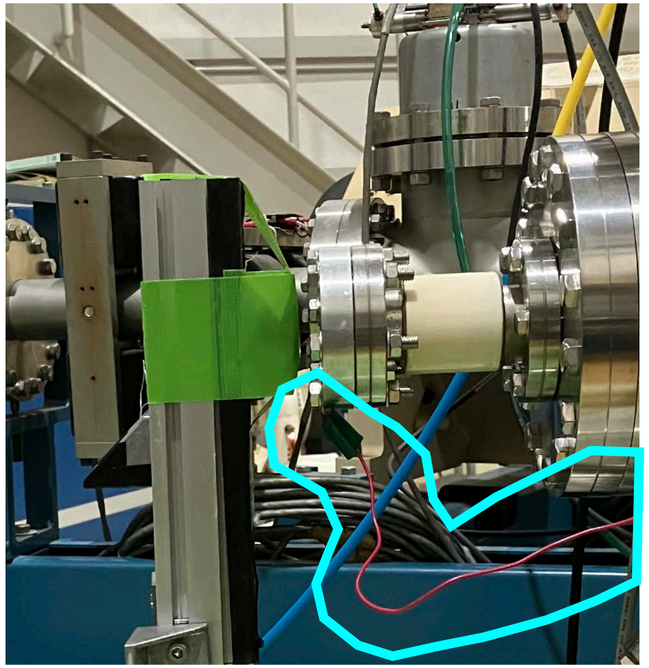


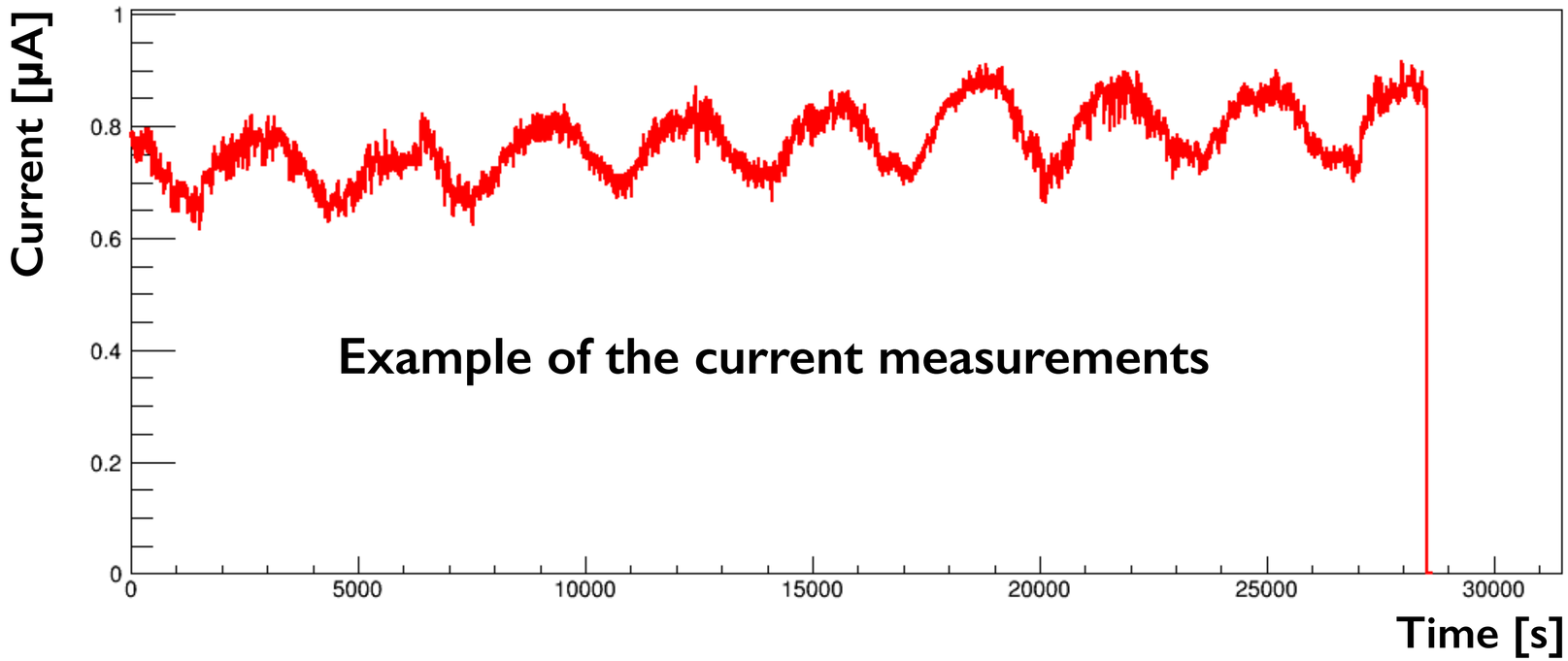
2 MeV has O(10)% higher effect than 1 MeV

The neutron flux at Tandem was assumed to be 1 MeV equivalent flux.

NIEL — Estimation of the Neutron Flux

The neutron flux was evaluated from the current in the reaction $^{9}Be + D^{+} (+ e) \rightarrow {}^{10}B + n$ integrated over the time assuming (4.9 ± 1.5) MHz/cm²/μA at 10 cm from the Be target on the beam axis [Y. Nakazawa et al., NIMA, 2019].





NIEL — Summary Table

We tested the bipolar components, voltage reference and operational amplifier, from the final reels, as well as other selected components.

Type	Model	Number of tested	Requirement [$\times 10^{12}$ n_{1MeV} cm^{-2}]	Confirmed [$\times 10^{12}$ n_{1MeV} cm^{-2}]
Voltage reference	REF2025	10	0.4	1.1–2.2
Operational amplifier	LM7322MM/NOPB	10	0.4	1.3–3.0
QSPI flash memory	MX25L12845GM2I-08G	9	0.4	3.6–11
SFP+ transceiver	Broadcom AFBR-709SMZ	2	1.3	4.6–12
SFP+ transceiver	Coherent FTLX8574D3BCV	1	1.3	4.6
SFP+ transceiver	Coherent FTLX8573D3BTL	1	1.3	11
SFP+ transceiver	Ficer FSPP-H7-M85-X3D	10	1.3	0.8–11
SFP+ transceiver	FS SFP-10GSR-85	4	0.4	6–20
DAC	DAC7678	1	1.3	5.3
LDO	TPS7A85	1	1.3	5.3
LDO for DDR	TPS51200	3	0.7	1.9–3.9

For the confirmed, the flux at which no failure was observed is shown.

The range is for all tested components.

Only one SFP+ FTLX8573D3BTL failed (13 x 10^{12}).

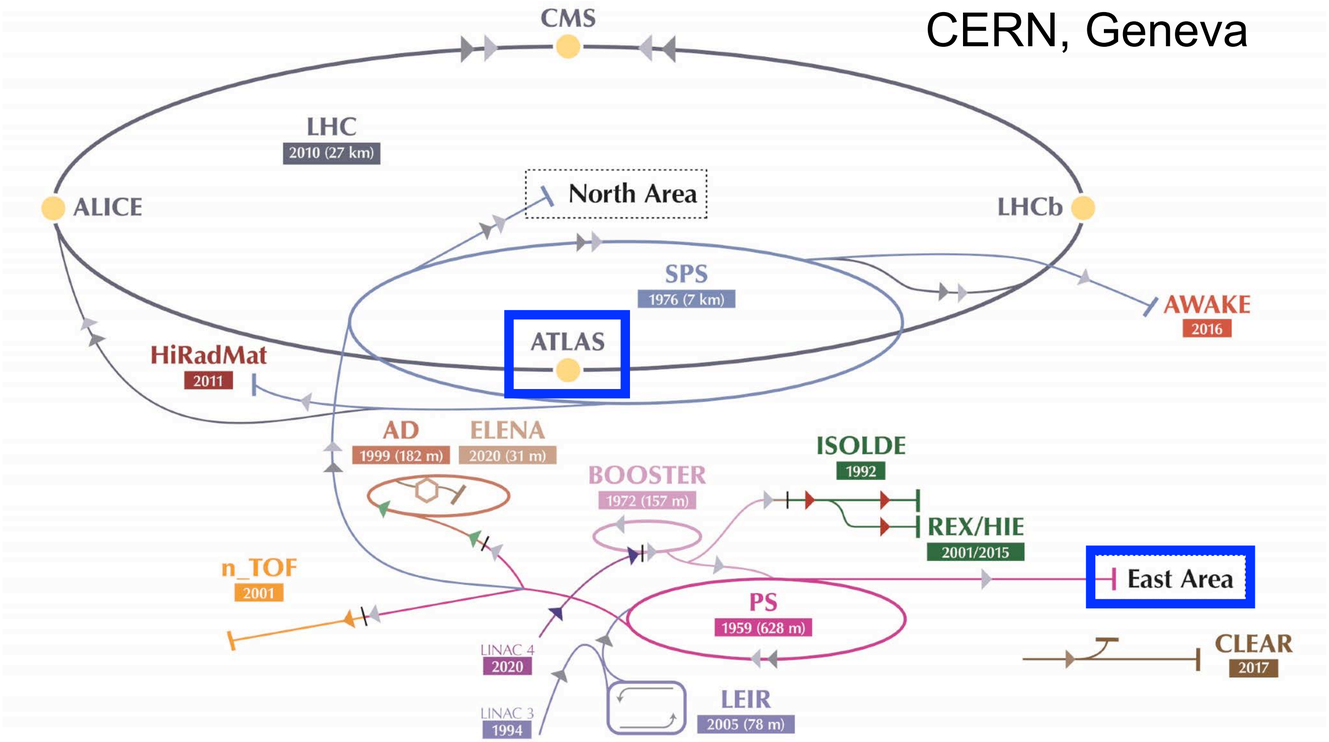
All the tested components satisfy our NIEL requirements.

SEE — Effects and Test Facilities

Single Event Effect (SEE):
temporary or permanent change
of the behaviour of electronics
due to a burst of charge
from single high-energy particle

Among several types of SEE,
our devices are affected mostly by
Single Event Upset (SEU),
a bit flip in memory or logic

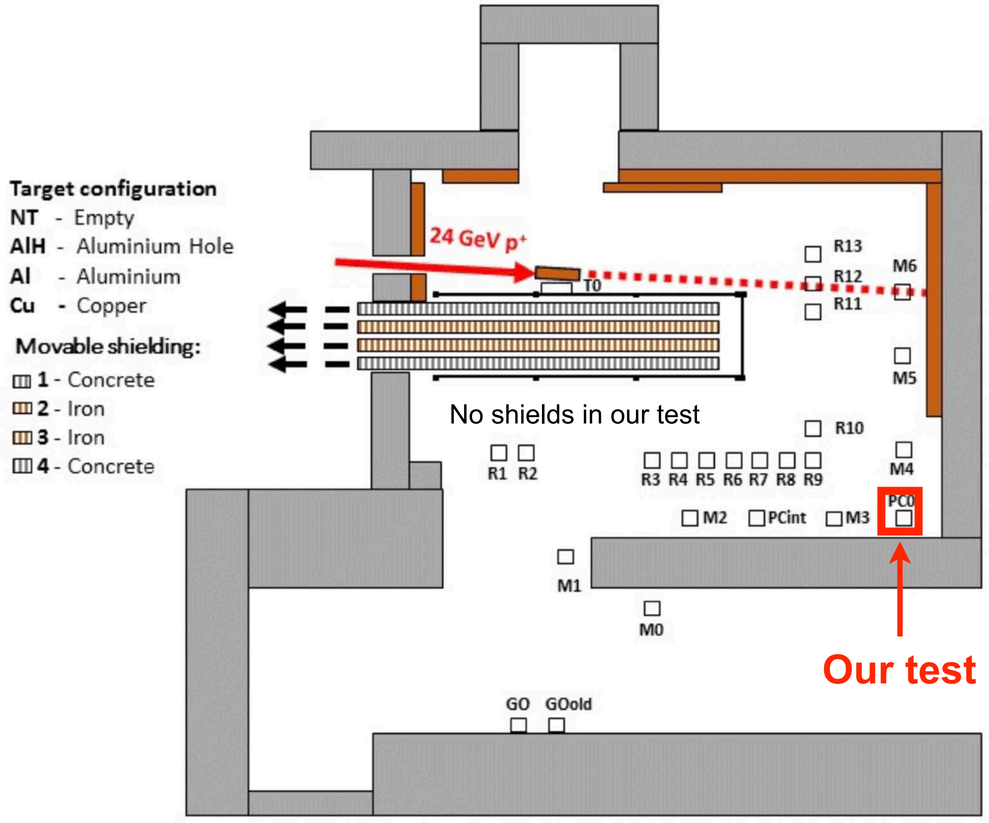
We tested the devices at ATLAS and East Area.

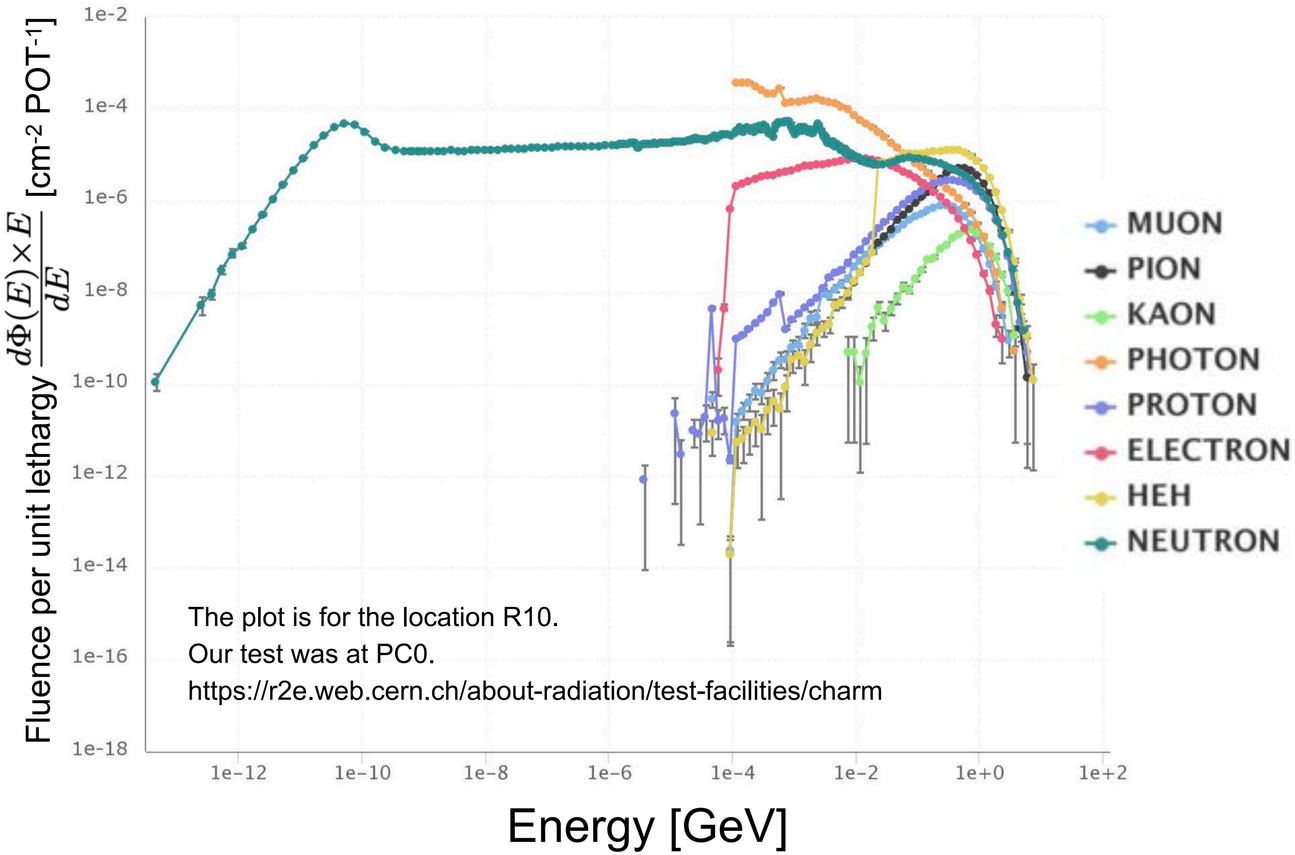


SEE — CHARM Facility in the East Area of CERN

Protons (24 GeV) from Proton Synchrotron impinges on a target (copper in our test).

Flux of hadrons with an energy > 20 MeV is employed as a reference for **SEE**.
TID and **NIEL** also exist.

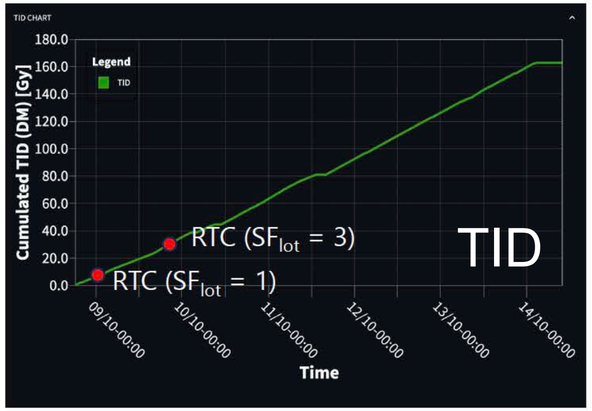


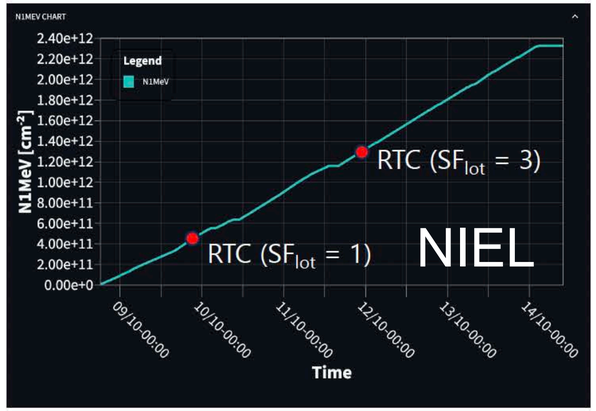


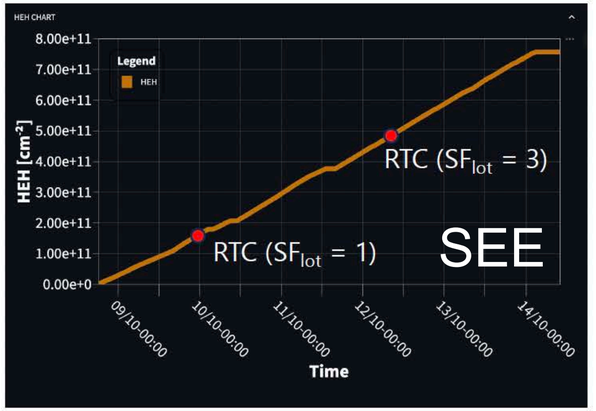
SEE — SFP+ Test at the CHARM Facility

SFP+ transceiver was tested at the CHARM facility.

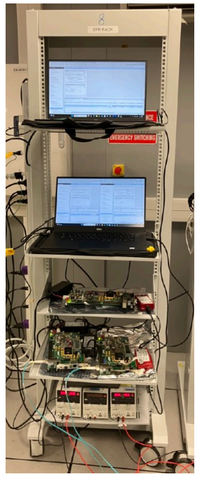
- **SF_{lot} = 1** applied
  as we tested the modules
  from the final selected lot
- **Radiation Tolerance Criteria (RTC)** reached by **~1 day**





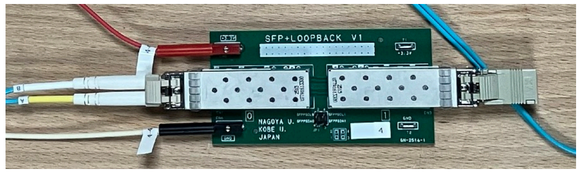


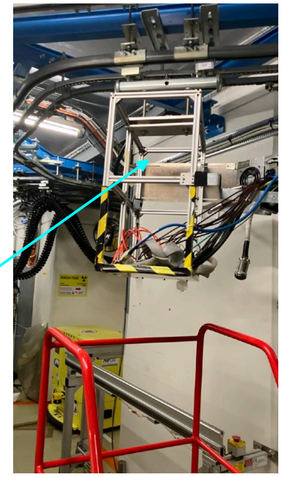
Laptop, **KC705 (SFP+)**,
and power supply
in the counting room



- **Loopback data transfer**
  during irradiation
- **Power cycle**
  sometimes

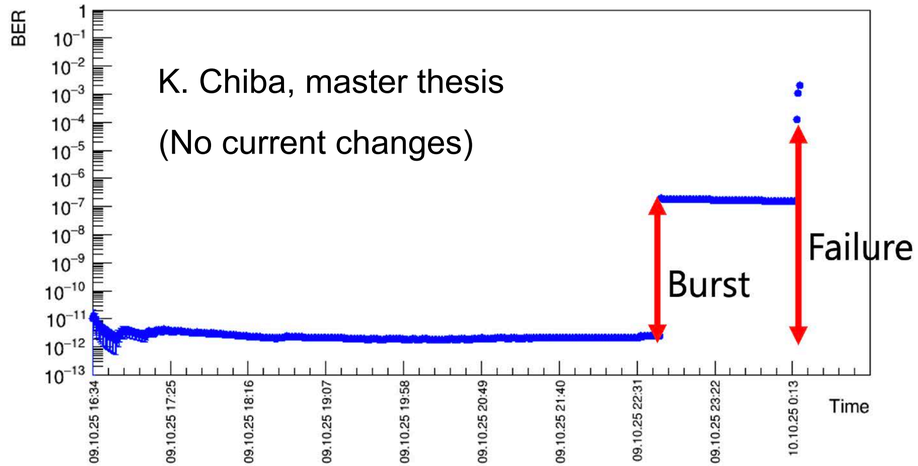
Test board with SFP+
attached to the Al frame
in the irradiation area

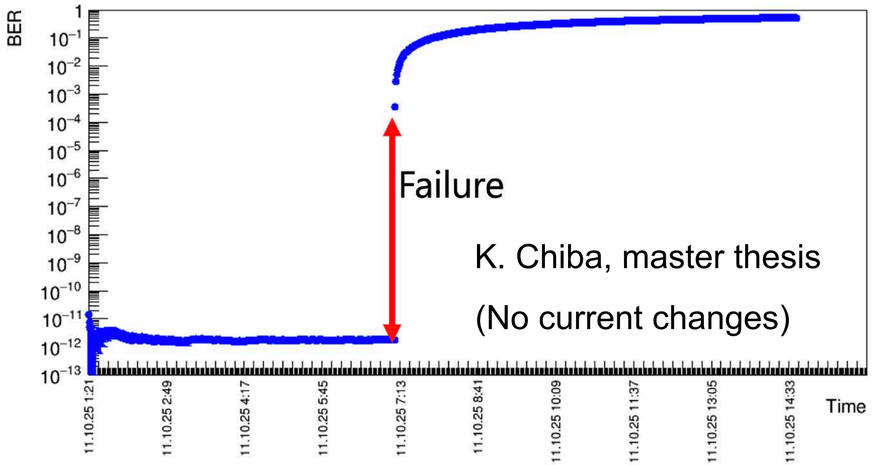




SEE — SFP+ Test at the CHARM Facility

- After the power cycle at 78 Gy, **no links** were established. They were fine at 57 Gy.
  - We assume that this was due to **TID**, as we observed no links at a similar dose in the gamma irradiation test for exactly the same lot.
- We observed **burst of bit errors, which would be due to SEU** (before 78 Gy).
  - “Burst” (5 times for 10 SFP+): BER < 10^{-3}, link status fine
  - “Failure” (4 times for 10 SFP+): BER > 10^{-3}, no link, **recovered only by power cycle**





Failure cross section: ~4 x 10^{-13} cm^2, ~10 power cycles for the TGC system per year (250 fb^{-1})

SEE — FPGA SEU

SEU in Kintex-7 FPGA needs careful study and recovery strategy.

Most of the errors in CRAM are **automatically recovered** by **the SEM controller** provided from AMD.

Enhanced Repair: ECC and CRC algorithm-based correction. This method supports correction of configuration memory frames with single-bit errors or double-bit adjacent errors. This covers correction of all single-bit upset events and all double-bit adjacent upset events. This also covers correction of multi-bit upset events when errors are distributed one or two adjacent per frame as a result of configuration memory interleaving.

For the errors that cannot be recovered by the SEM controller, **FPGA reconfiguration** is initiated from **the external boards,** i.e. JATHub.

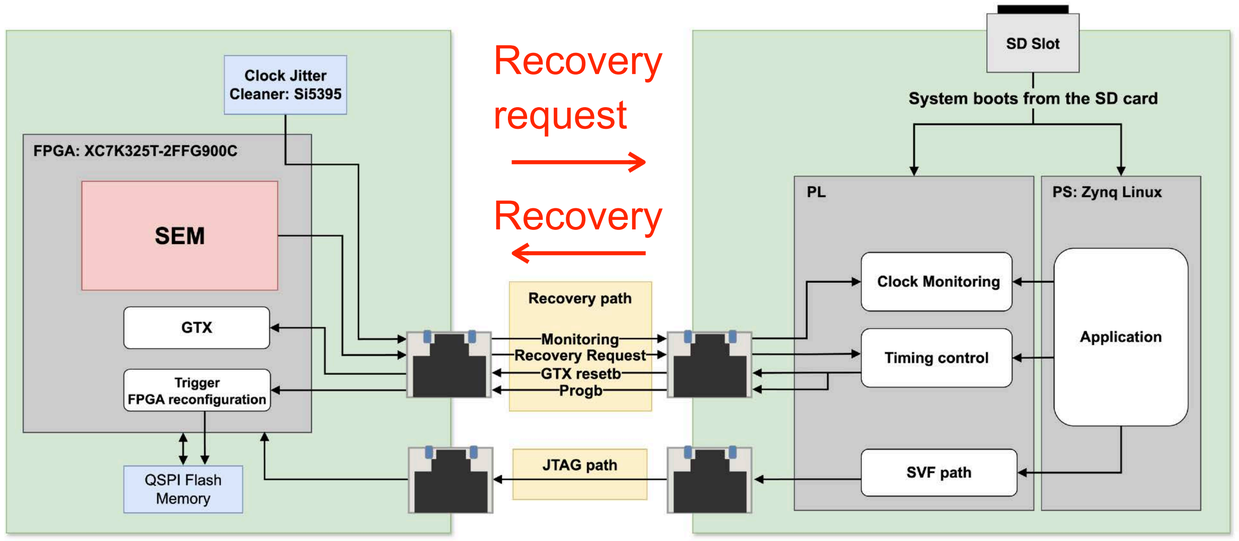


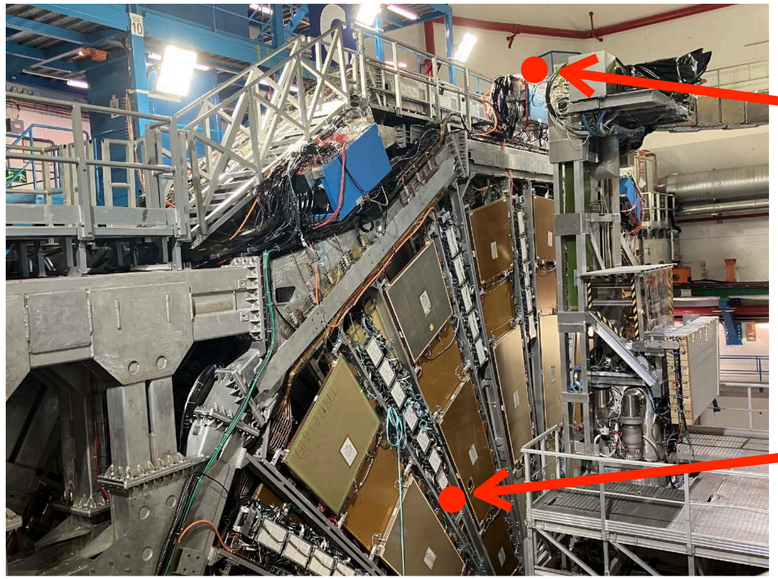
Figure: D. Hashimoto

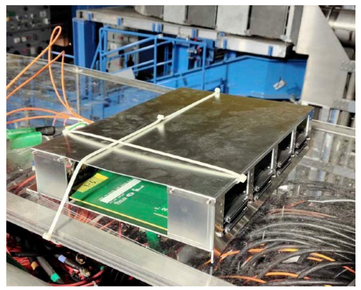
PS board with Kintex-7 FPGA

JATHub board with Zynq-7000 SoC

SEE — FPGA SEU Studies

The boards were installed in the ATLAS experimental area,
and the SEU rate measurement and recovery tests were performed.

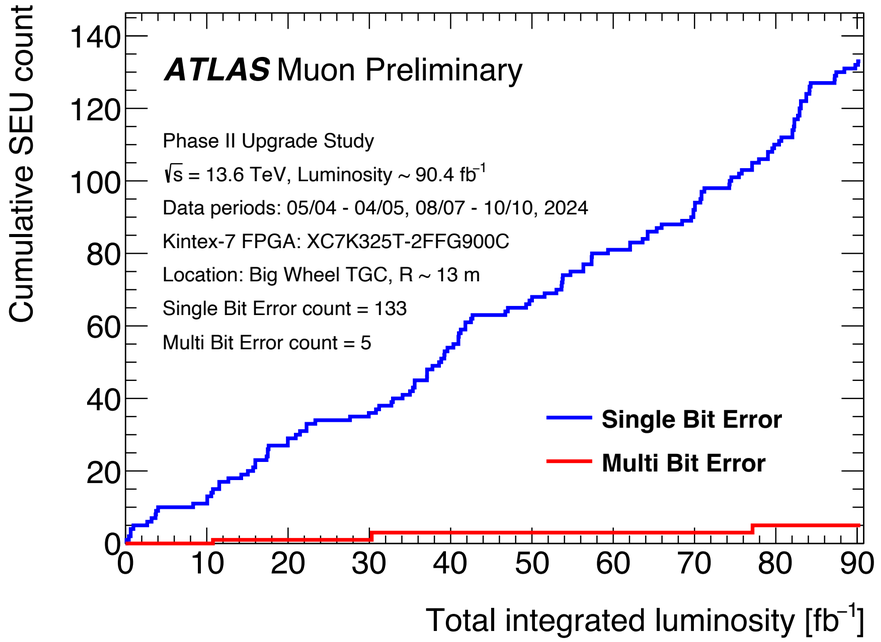


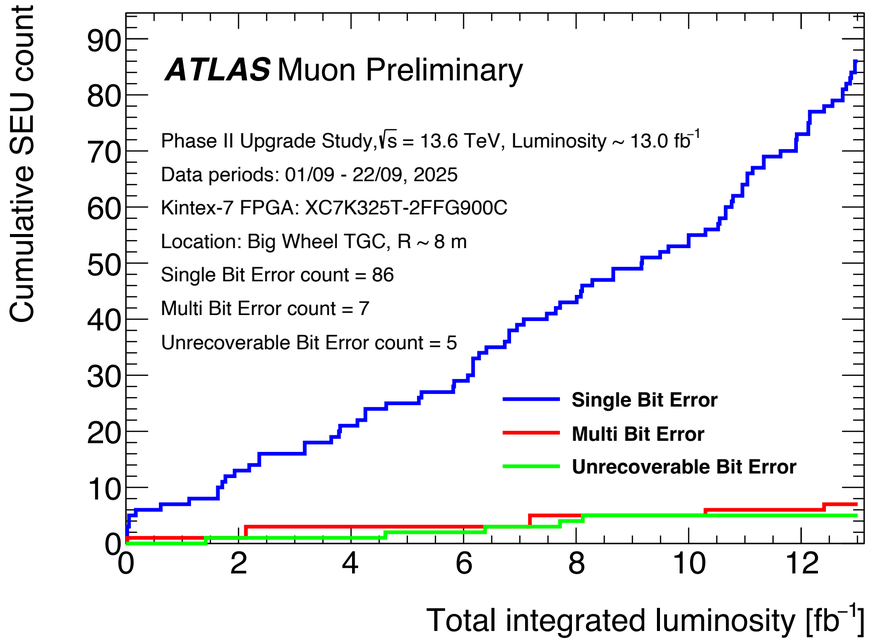


2018 and **2024**
- Located at **13 m** from beam axis
- Board surface **parallel** to beam axis
- Without JATHub board

2025
- **The actual location and angle**
  for the experiment
  (**8 m** and **perpendicular** to beam axis)
- With JATHub for **reconfiguration tests**

SEE — FPGA SEU Results





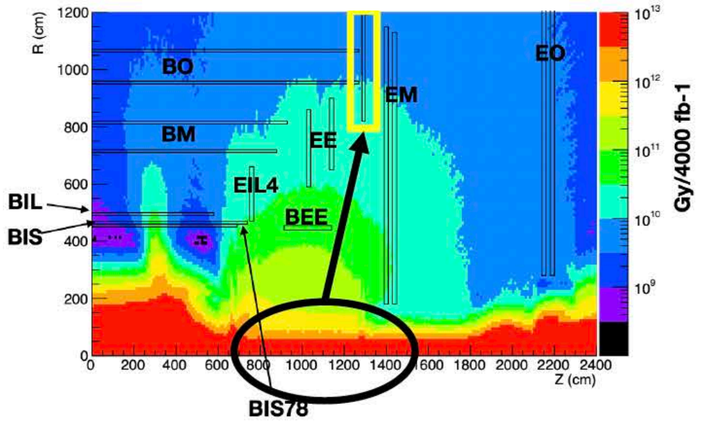
- **133 single-bit** and **5 multi-bit** errors for integrated luminosity of **90 fb^{-1}**
- Cross section: **~2 x 10^{-15} cm^2/bit**
- All errors recovered by **the SEM controller**.

- **86 single-bit** and **12 multi-bit** errors for **13 fb^{-1}**
- Cross section: **~7 x 10^{-15} cm^2/bit**
- All single-bit and 7 multi-bit errors recovered by **the SEM controller**, **5 multi-bit errors recovered by reconfiguration**

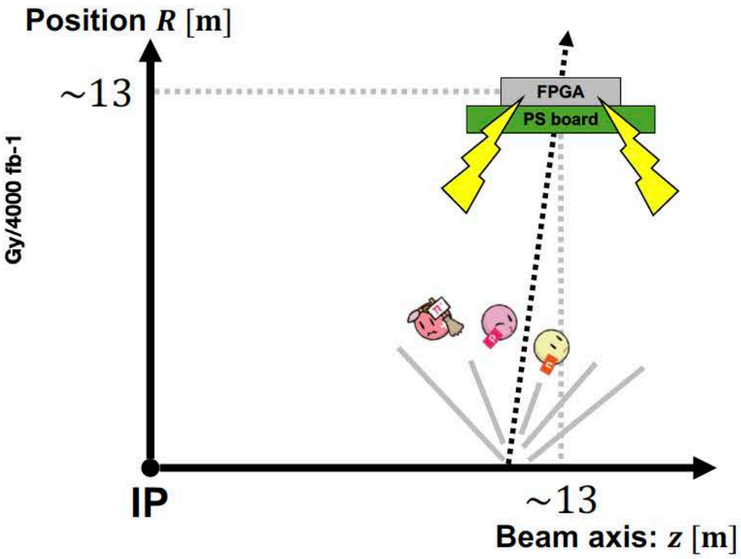
Note: cross section calculated without considering about different incident angles

SEE — FPGA SEU Considerations

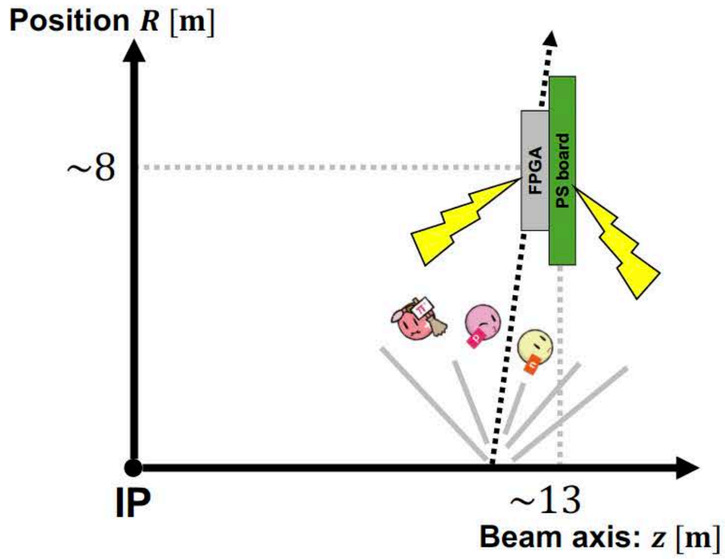
The difference of the number of upsets per luminosity and the fraction of multi-bit upsets would be due to not only **the number of incident hadrons** but also **the incident angles**.



Locations in 2018 and 2024



Locations in 2025



Each FPGA in the TGC system would have **O(0.0001) upset events per second** in CRAM.
Most of them recovered by the SEM controller (**< 100 ms**), <1/10 needs reconfiguration (**~5 s**)

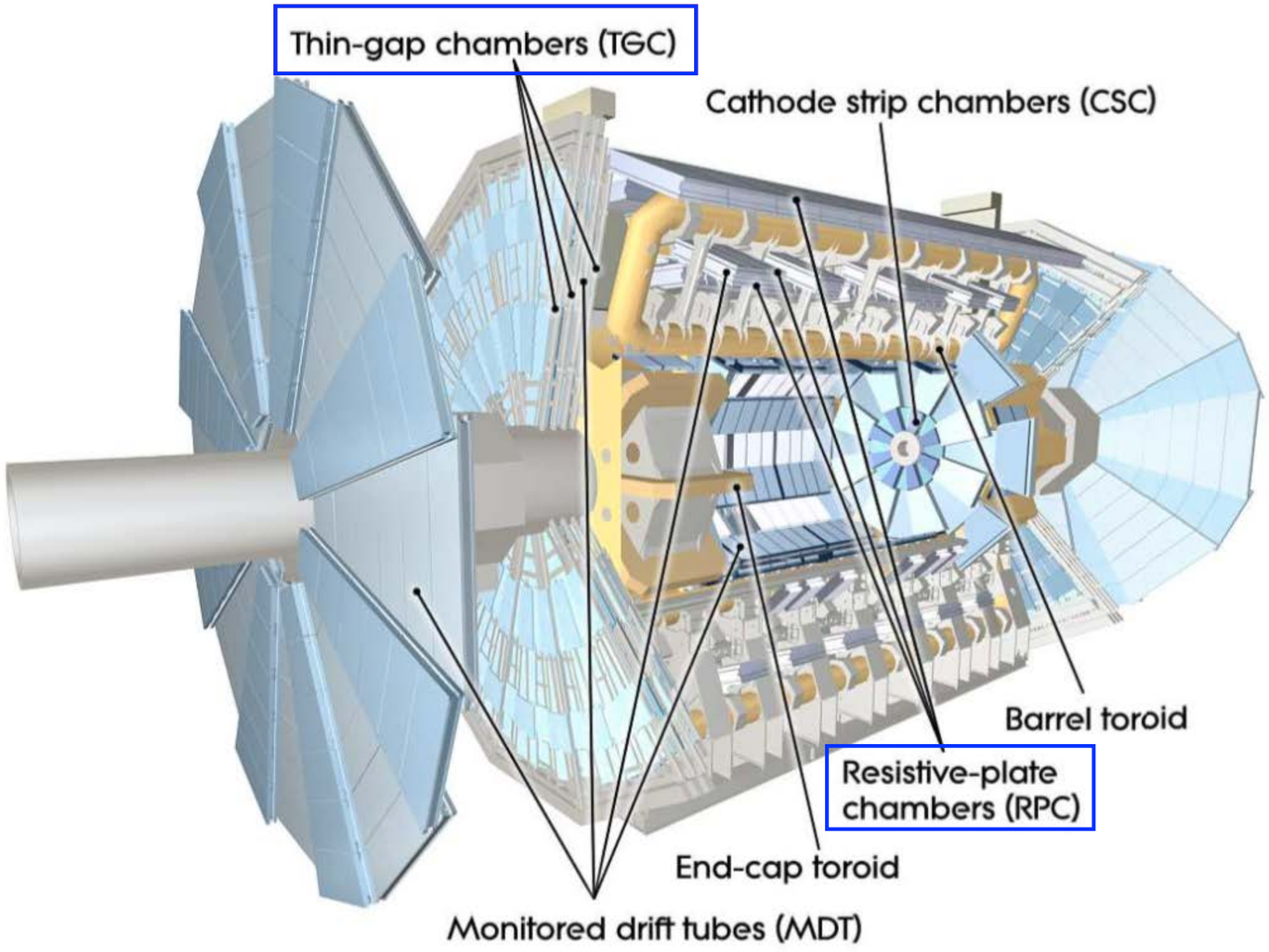
Limited impact on the inefficiency, good to have experiences in the actual experimental area!

Conclusion

- In order to upgrade the TGC electronics of the ATLAS experiment, we have been conducting radiation tolerance tests for TID, NIEL, and SEE on various electronics components.
- Although some components did not meet the requirements, suitable alternatives were identified. We implement the system almost entirely with commercial off-the-shelf components.
- The FPGA SEU rate was measured in the actual experimental hall, and the operation of automatic recovery mechanism was verified.

More Slides

The ATLAS Muon Spectrometer Overview



η: pseudorapidity

MDT

- Precise tracking
- $|\eta| < 2.7$ (inner station: $|\eta| < 2.0$)

CSC

- Precise tracking
- $2.0 < |\eta| < 2.7$ (inner station only)

RPC

- Trigger, second coordinate measurement for precise tracking
- $|\eta| < 1.05$

TGC

- Trigger, second coordinate measurement for precise tracking
- $1.05 < |\eta| < 2.7$ (trigger: < 2.4)

Japan

Note: the detectors in the inner station in $1.3 < |\eta| < 2.7$ replaced by New Small Wheel (NSW) in 2021.

NIEL — Tandem Accelerator Operation

The Tandem operation is fun and provides good experiences for students.
When the terminal voltage was unstable, we reduced the voltage from the nominal value 1.5 MV to 1.4 MV or lower.