Q-RadSemi2026

Analog ASIC Development at KEK and Its Applications to Measurements in High-Radiation Environments

2026/1/23

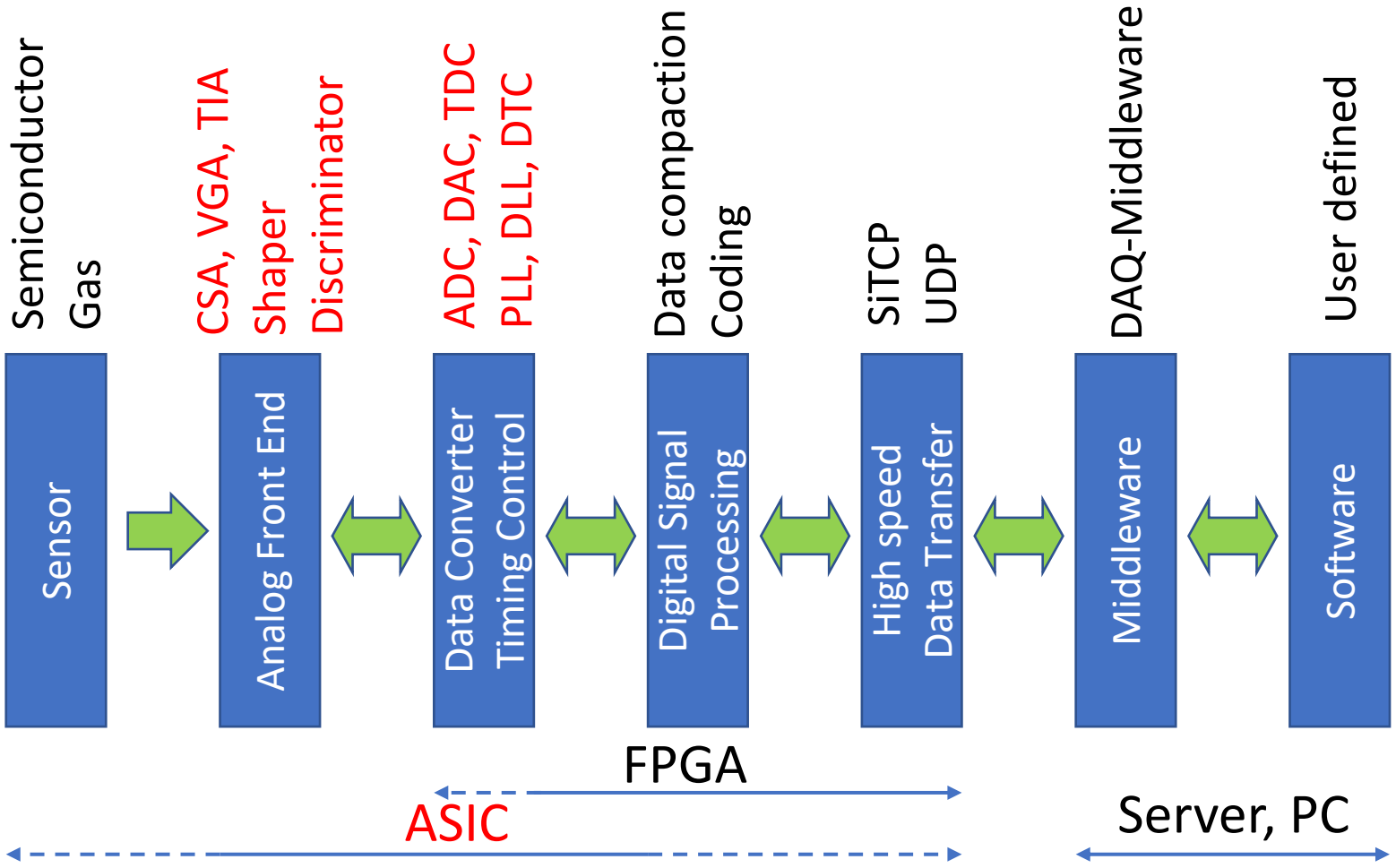
Masaya MIYAHARA

QUP and IPNS, KEK

Contents

ASIC development at KEK

Electronics in particle and nuclear physics and accelerator science, with a focus on ASIC development and its technological applications to related fields.

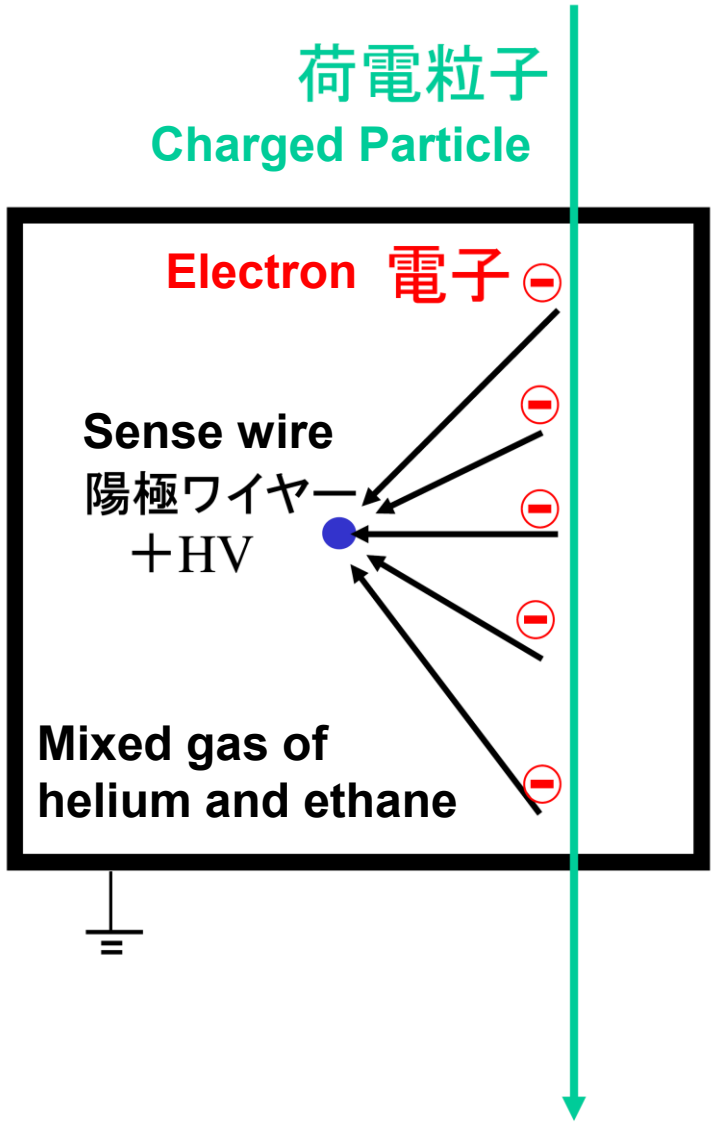


1) Develop ASICs for collider experiments
2) Technology transfer technologies to non-collider experiments
3) Apply these technologies to contribute to society
   - Rad-hard
   - Cryo CMOS

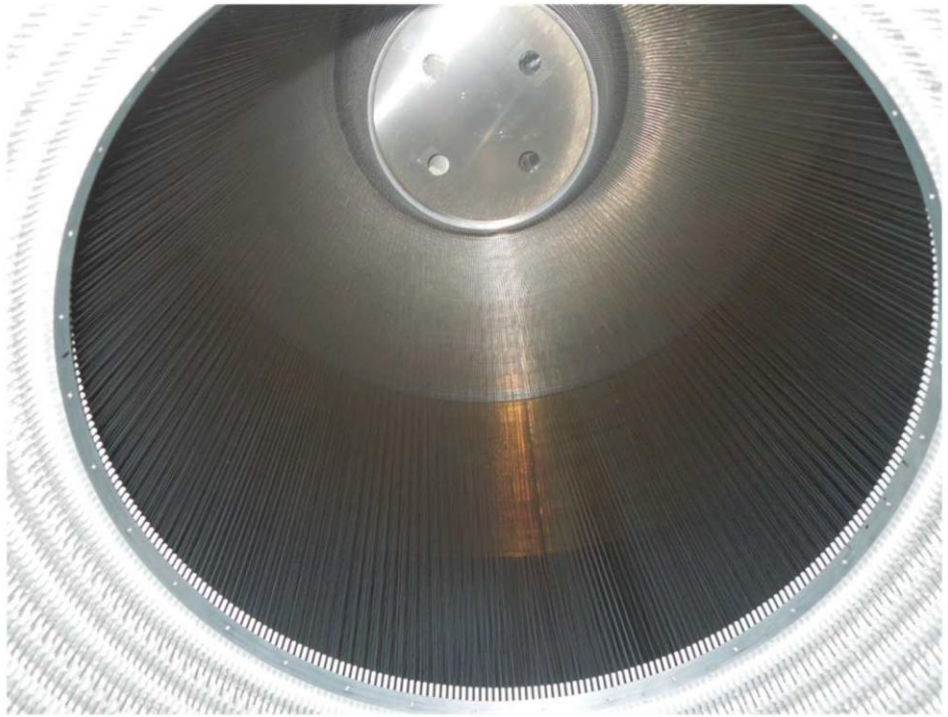
ASICs for particle physics experiments and applications

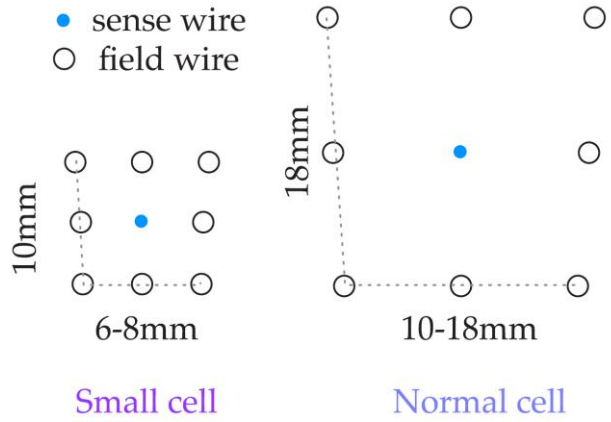
Name	Function	Purpose	Experiments, Applications
PP-ASIC	32ch, Sub-ns timing control with 40ns dynamic range	Timing correction and tagging for the TGC	Trigger system upgrade for the HL-LHC)ATLAS experiment
RAPID	8ch, Reconfigurable Amp-shaper-Discriminator+ADC	High-speed waveform readout for drift chambers	Belle II (CDC), AR test beamline, read-out test for semiconductor detectors (CIGS, GaN), etc.
YAENAMI	8ch, Variable Gain Amplifier +ADC with bias control DAC	High-speed SiPM/MPPC waveform readout	T2K, J-PARC NINJA, Λ–p scattering experiment, etc.
FGATI	16ch, BW>1GHz Trans-Impedance Amplifier	High-speed signal processing for SiPM/APD	TRIUMF μSR spectroscopy, IMONY astronomical observations
AGASA	32/16ch, Reconfigurable ASD	ASD front-end for gas detectors	J-PARC Hadron experiment, RCNP, RIKEN
QPIX_NEO	64ch, Full-Pixel Continuous ADC Readout	Continuous waveform readout for pixel detectors	Gas detectors (TPC), Compton cameras, direct CIGS deposition, etc.
SCIBER	16ch, ADC with Mid-Range Data Transmission	ASD and ADC readout for SiC detectors	J-PARC COMET (Under development)

Central Drift Chamber (CDC)



- When charged particles pass through a gas, electrons and ions are generated by collisions between the charged particles and the electrons in the gas molecules.
- The number of electrons generated is proportional to the amount of energy loss.
- Relatively cheap and can be easily scaled up.



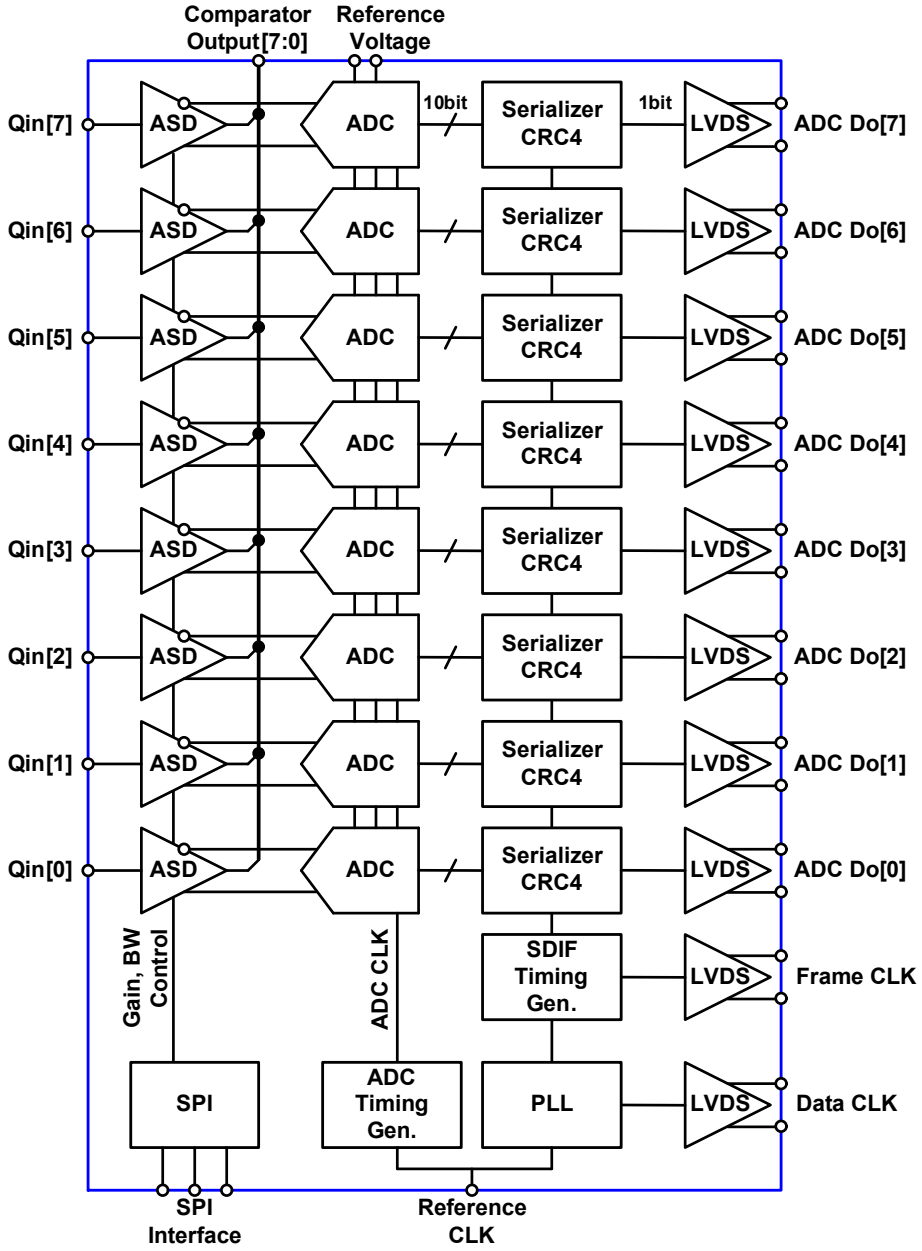


Sense wire : 14,336
Field wire : 42,240

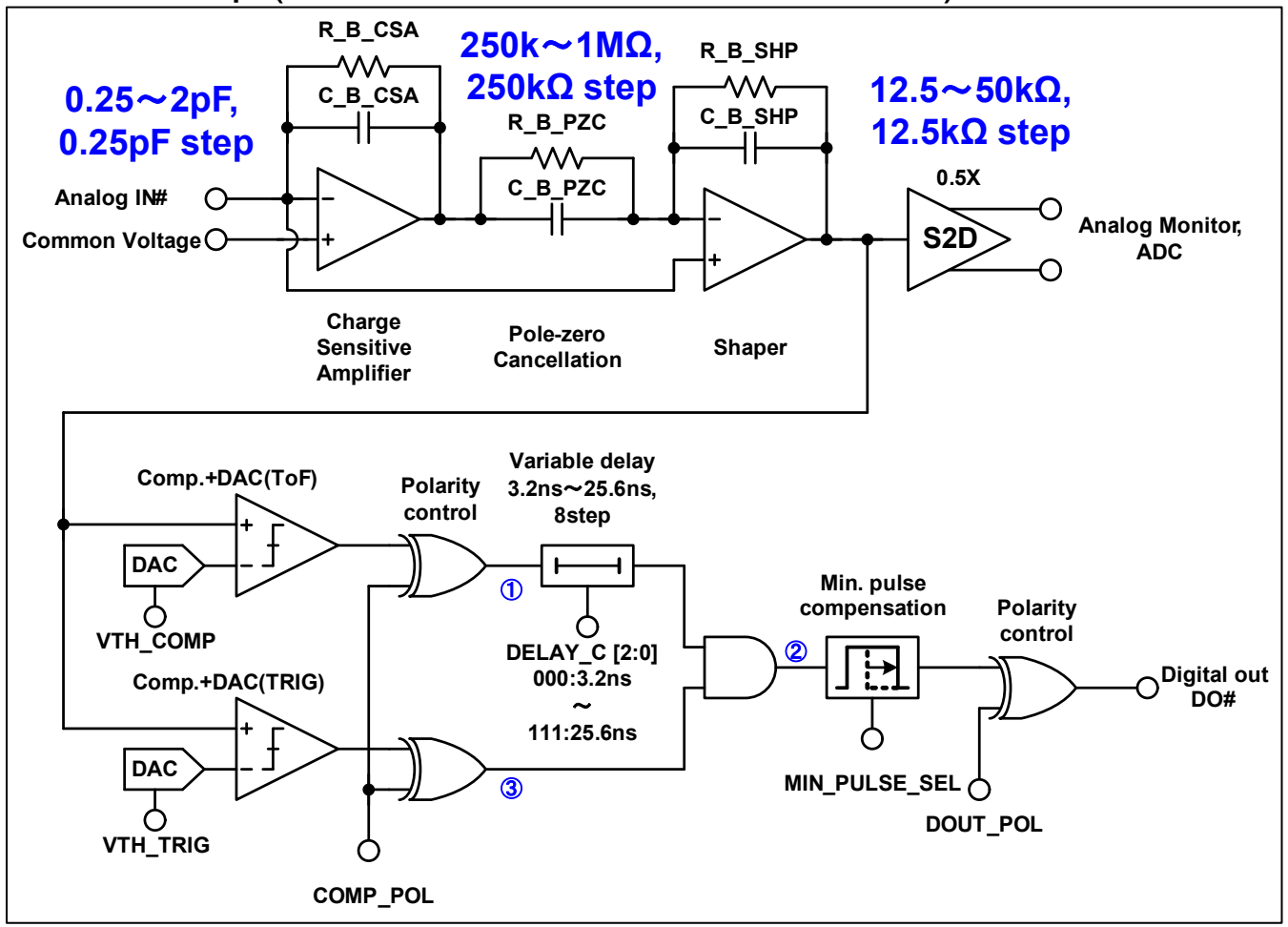
Structure of Belle II CDC

S. Uno, Advanced DAQ Seminar 2021

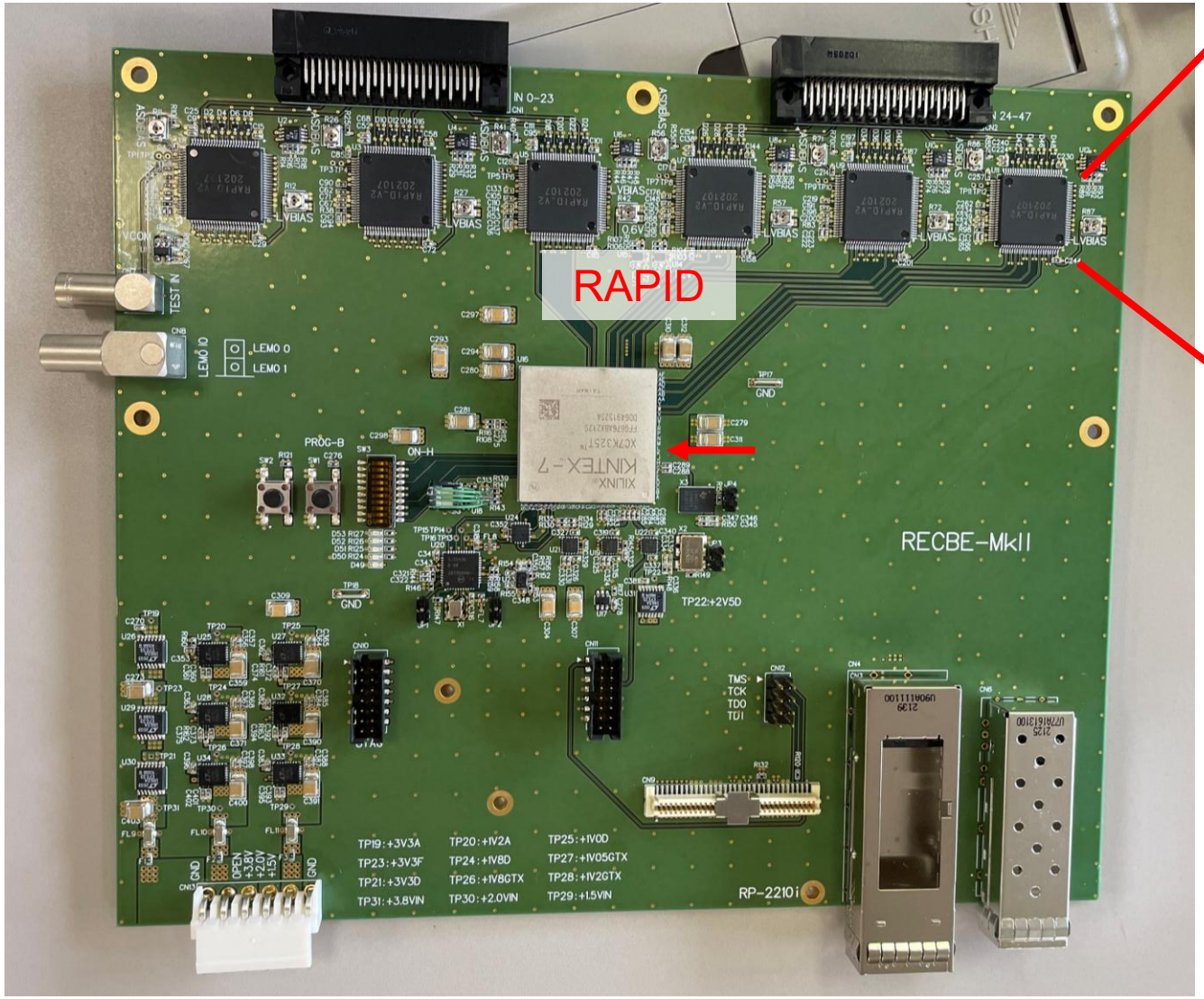
Reconfigurable ASD-ADC for Paticle Detector (RAPID)



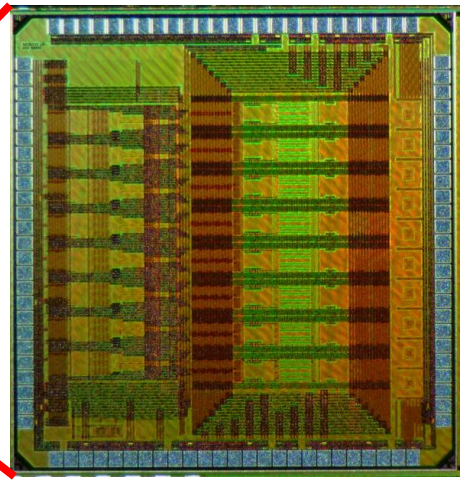
- Read-out ASIC for central drift chamber(CDC) in Belle II
- Reconfigurable Amp-Shaper-Discriminator
- 10bit 100MS/s ADC for real time analog signal monitoring
- 8Gbps data transfer
- 300mW/chip (half is I/O circuit, LVDS standard)



Development of Readout Board for CDC



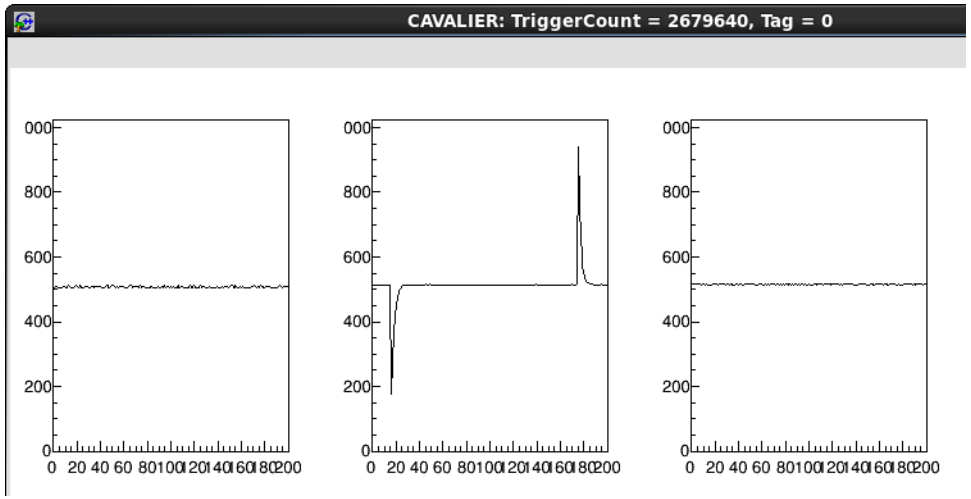
New Readout Board using RAPID (RECBE -Mk II)



TSMC 65nm, 4mm^2

Supply : 1.2V / 3.3V
Pd : ~300mW@100MS/s

2x Performance,
3x Power efficiency
(Current standards)



Real time monitoring by
10bit, 100MS/s ADC

Applying and extending RAPID technology

Implemented through communities (SPADI-A, Open-It)

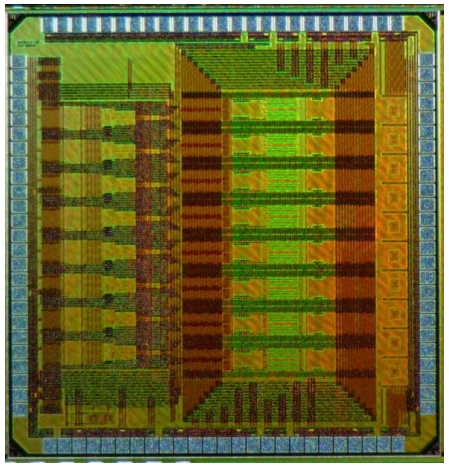
General-purpose readout for SiPMs

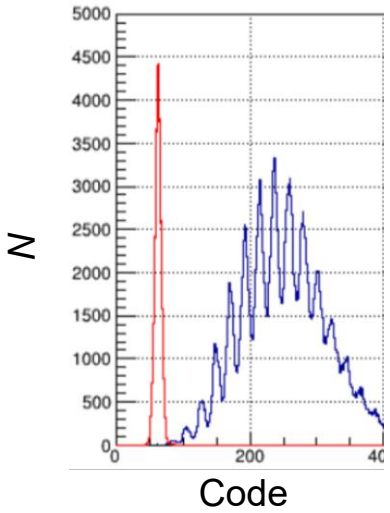
RAPID

YAENAMI

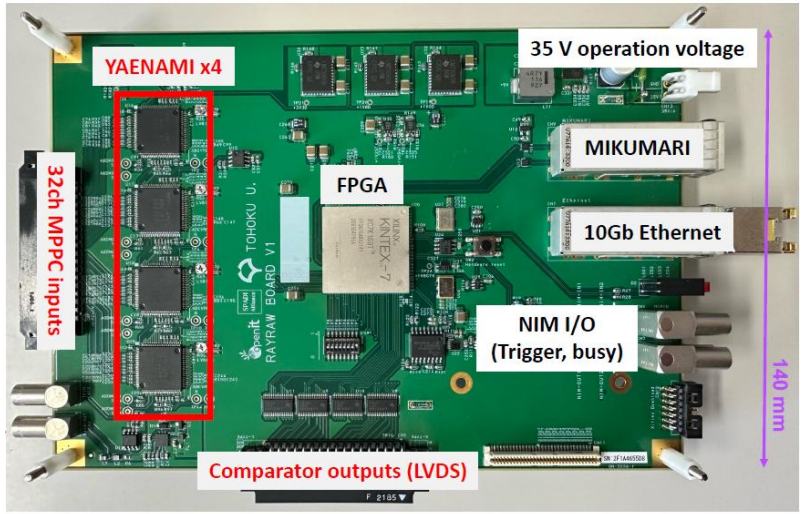
AGASA

General-purpose readout for gas chamber

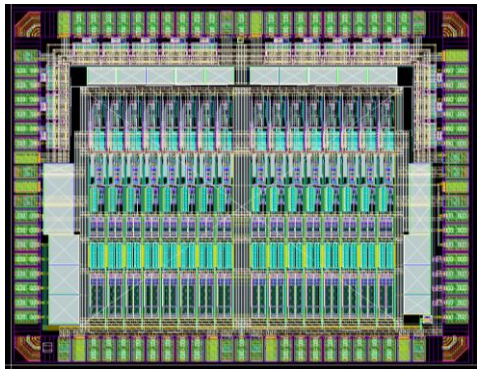


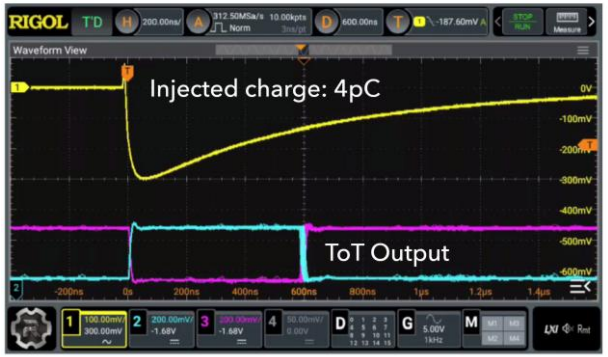


8ch VGA+ADC,
Includes a DAC for adjusting SiPM gain

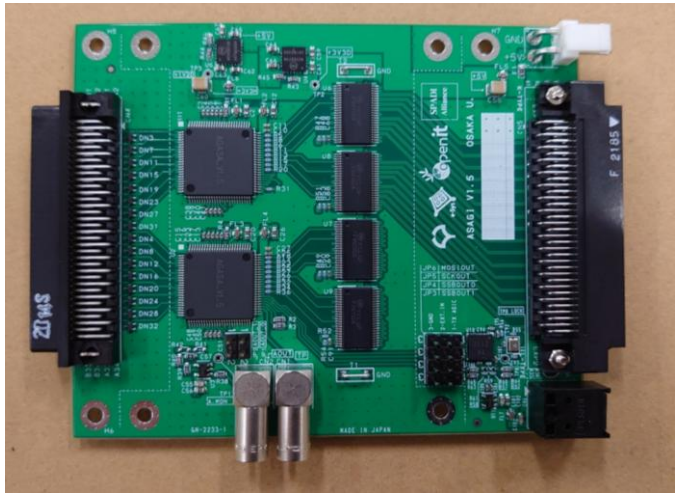


RAYRAW board
https://spadi-alliance.github.io/ug-rayraw/





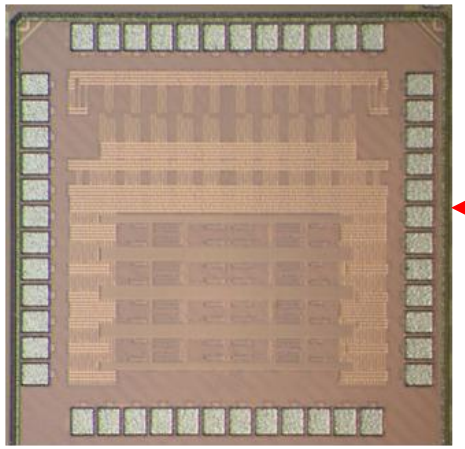
16ch Amp-Shaper-Discriminator (LVDS out)
Adjustable gain and time constant



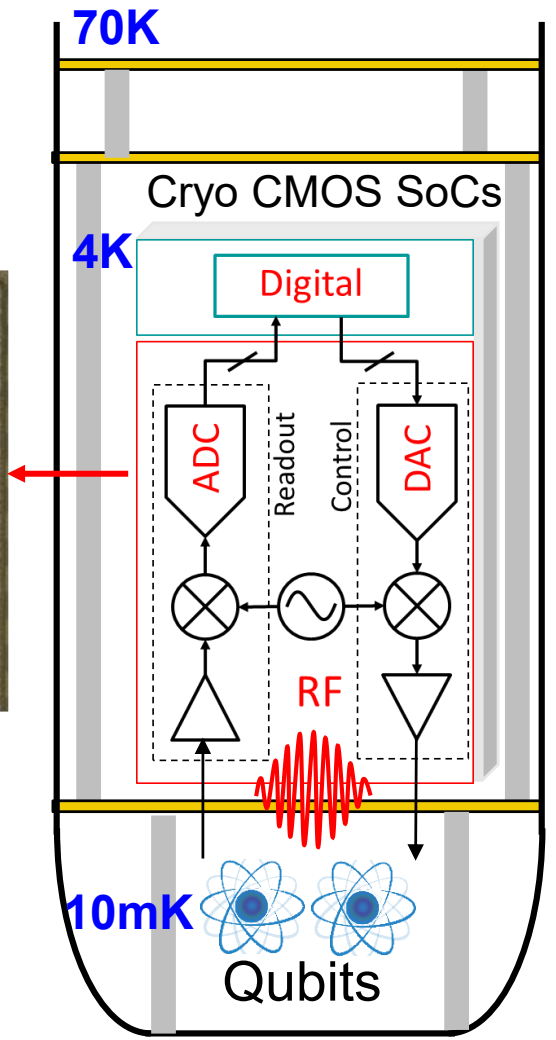
ASAGI card

Cryo-CMOS Project

- Project: Fault-tolerant universal QC, Moonshot Research and Development Program Goal 6 (MS6), JST
  - ✓ Development of a scalable, highly Integrated quantum error correction system including cryogenic CMOS circuits
- Sub goal: Implementing ASICs operating at a cryogenic temperature (~4K) to control Qubits for Quantum Computers and Quantum Sensing
- Contribution: Development of ADCs and cryogenic testing environment for system-on-chip (SoC)



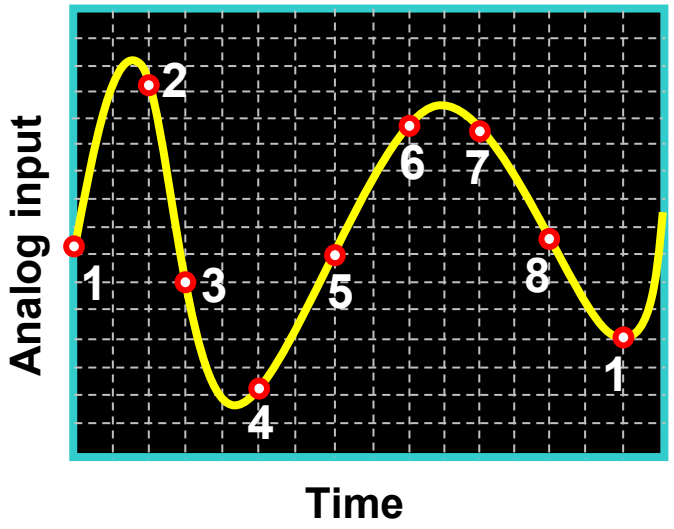
Cryo-CMOS ADC



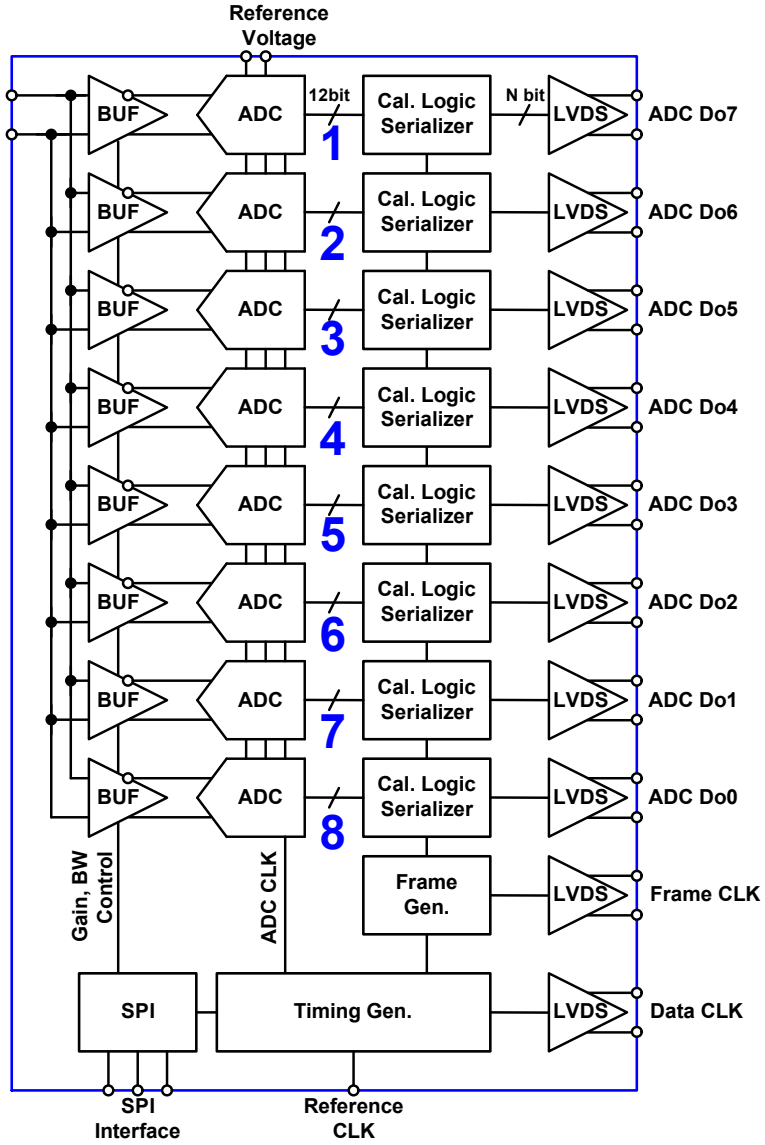
Cryo-CMOS for Qubit Control

Target of Cryo-ADC Development

- Target specification
  - Resolution: 8~12bit
  - Sampling rate: 1~6GS/s
  - Temperature: 300~4K
    - Target performance will be tuned to cooling capacity and qubit observability.



- Challenges
  - Development of scalable ADC architecture suitable for interleaved operation
  - Implementation of performance compensation mechanisms for circuits operating at cryogenic temperatures.



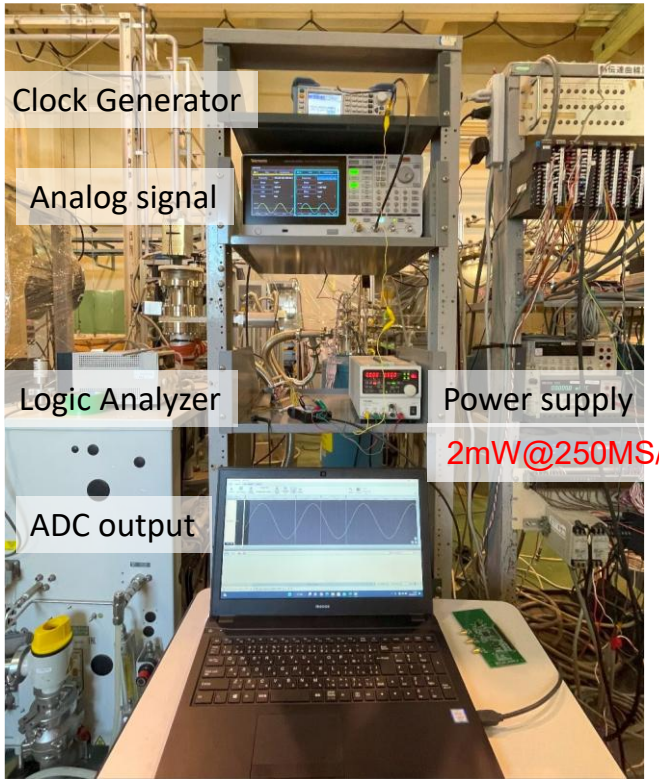
Time-interleaved ADC (8x)

Measurement result of single ADC

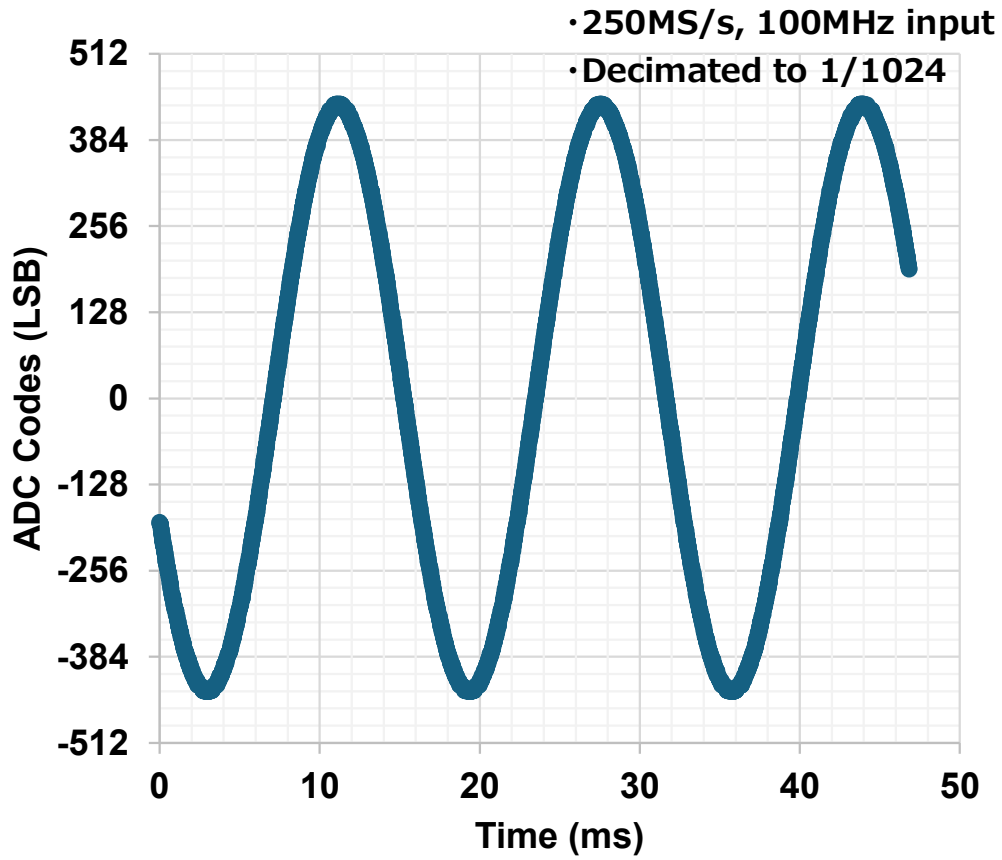
- Developed a 10-bit, 250 MS/s ADC using a 22 nm bulk CMOS process.
- Proposed ADC has been confirmed to operate normally both room temperature and 4.2K.

Dewar

Insert



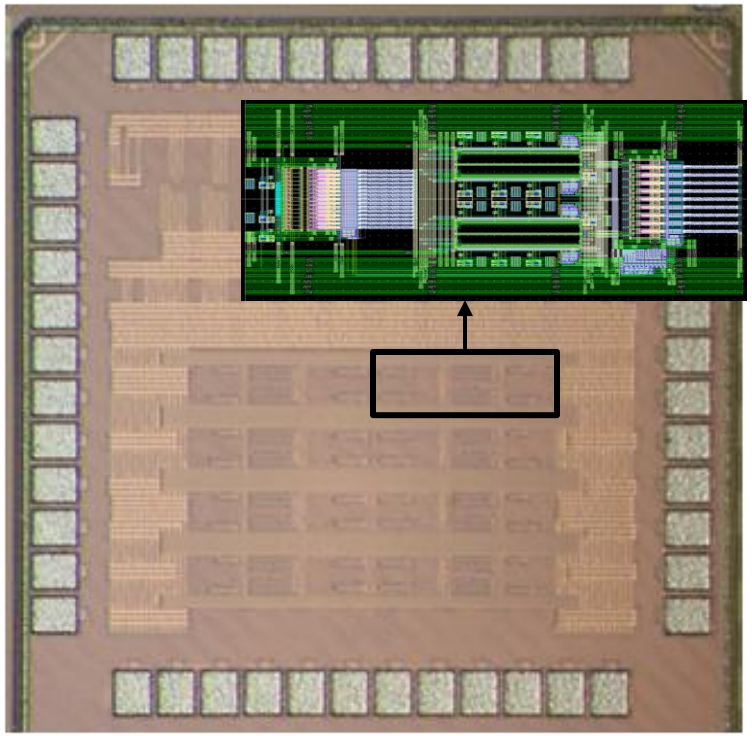
Cryogenic measurement setup for the ADC
(Supported by cryogenic group in ITDC, KEK)



Sine wave input test of ADC @4.2K

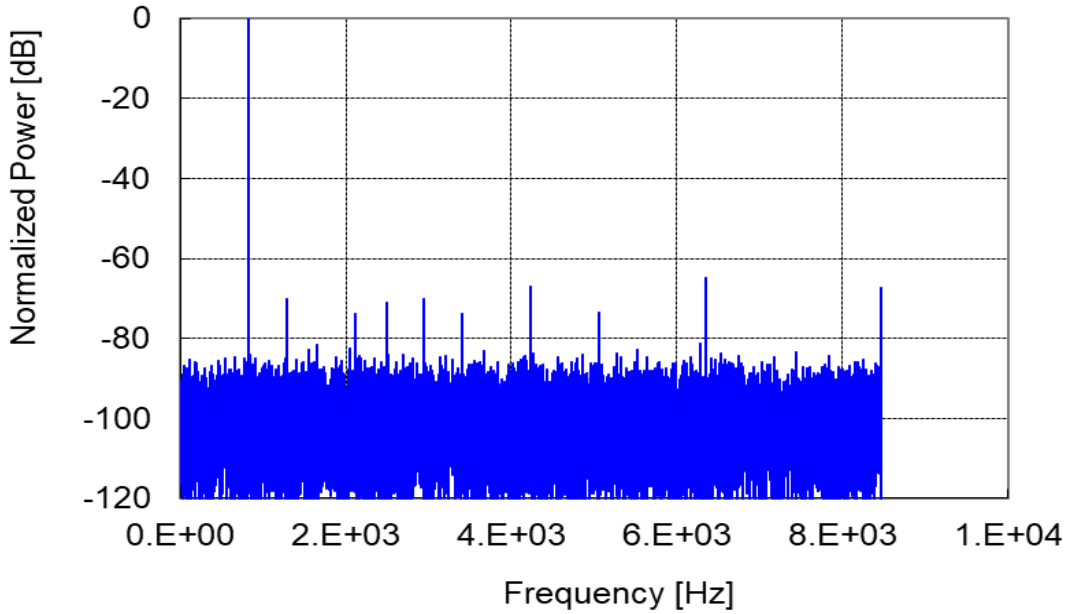
8x Time-interleaving ADC

- A 10-bit, 2 GS/s ADC consuming 13 mW was successfully operated at both room temperature and 4.2 K.



Chip phot of an interleaving ADC

SNR	SFDR	SNDR	ENOB
53.1dB	65.0dB	52.9dB	8.5bit

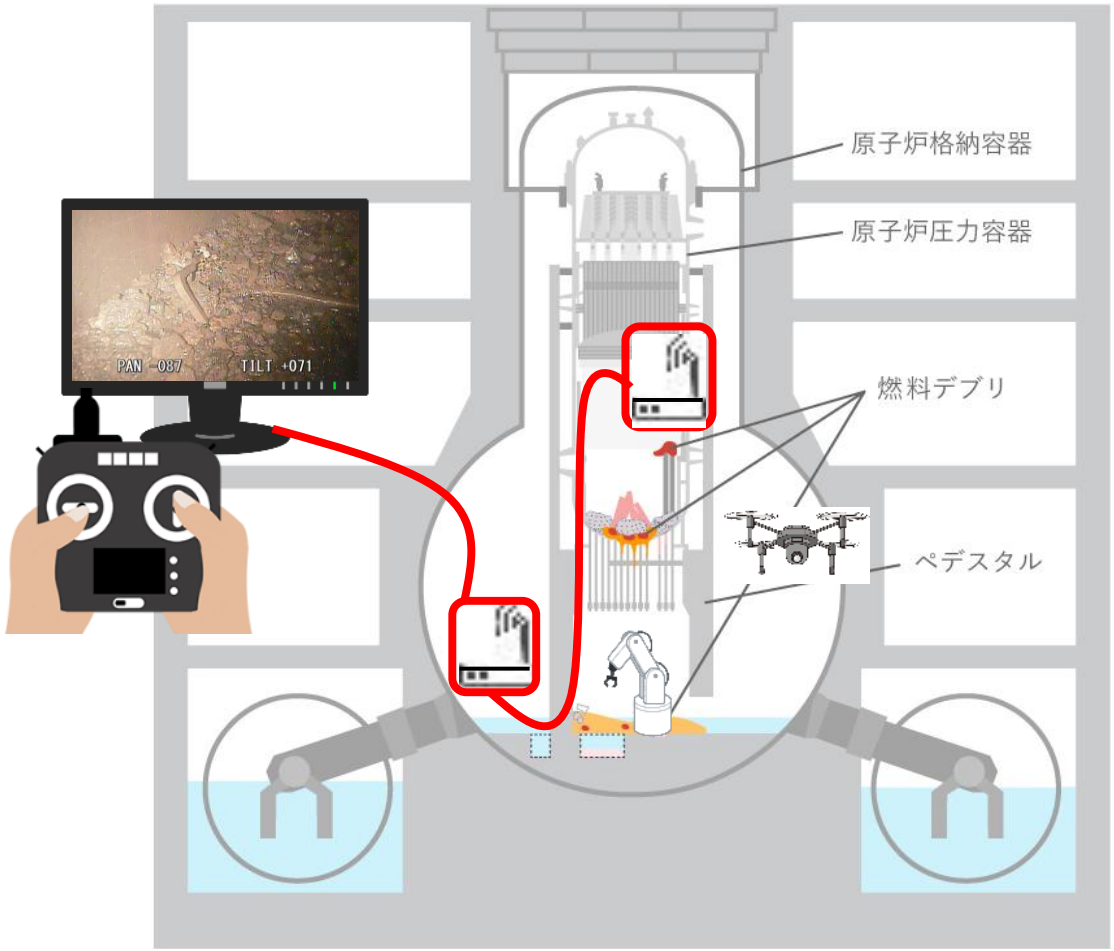


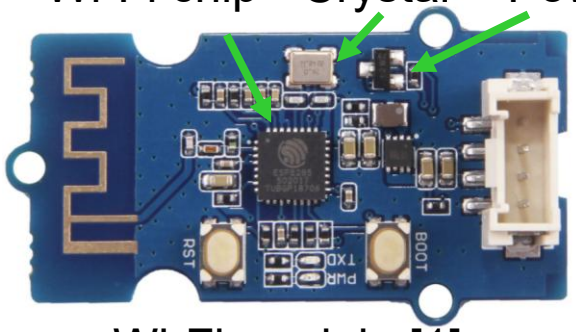
FFT analysis with a sinusoidal input

Contents

Wireless system development for reactor decommissioning

In collaboration between two coordinated proposals (KEK and Science Tokyo), we will develop radiation-tolerant RF/ABB/DBB chipsets required for wireless operation inside a reactor containment vessel.





Wi-Fi module [1]

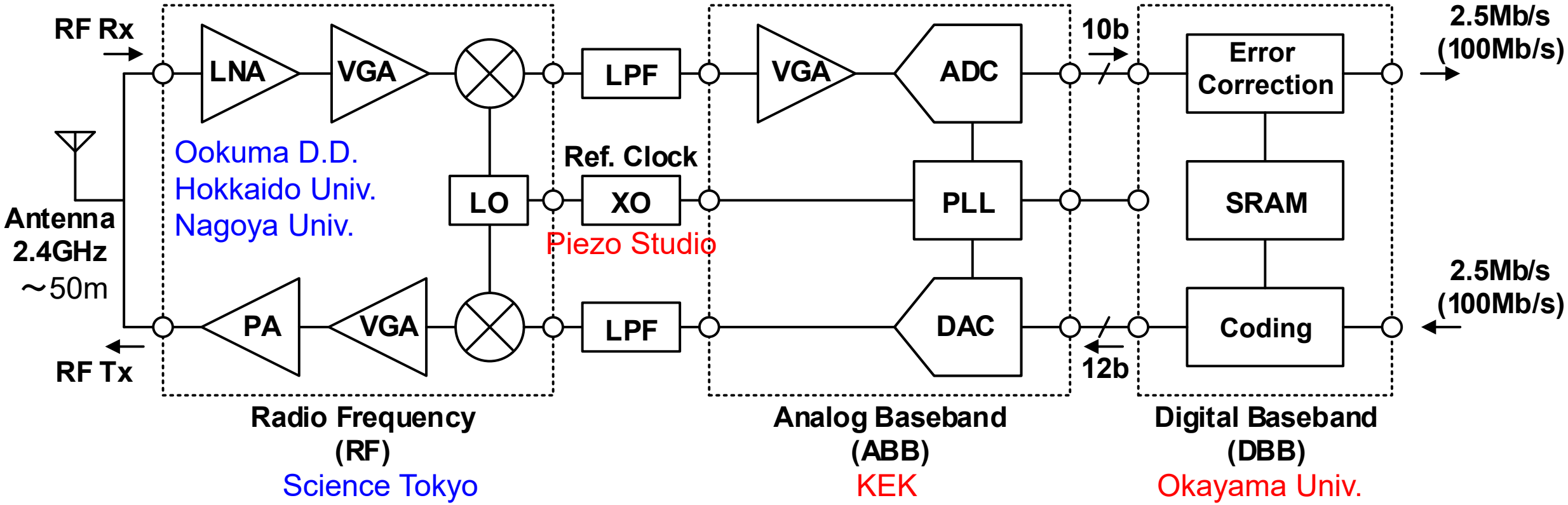
Wireless system ≈ Wi-Fi chip

Item	Specification
Frequency band	2.4 GHz
Data rate	2.5 Mbps (up to 100 Mbps)
Communication range	50 m
Radiation dose rate	10 Gy/h (up to 1 kGy/h)
TID tolerance	≥ 1 MGy
Operational lifetime	≥ 1 year

[1] https://www.seeedstudio.com/Grove-UART-WiFi-V2-ESP8285.html

Chipset architecture and development framework

- Using a 65 nm CMOS process with demonstrated operation at 1 kGy/h and TID > 3 MGy.
- The electrical specifications will be defined in accordance with the IEEE 802.11n standard.
- The development will be carried out with future single-chip integration in mind.

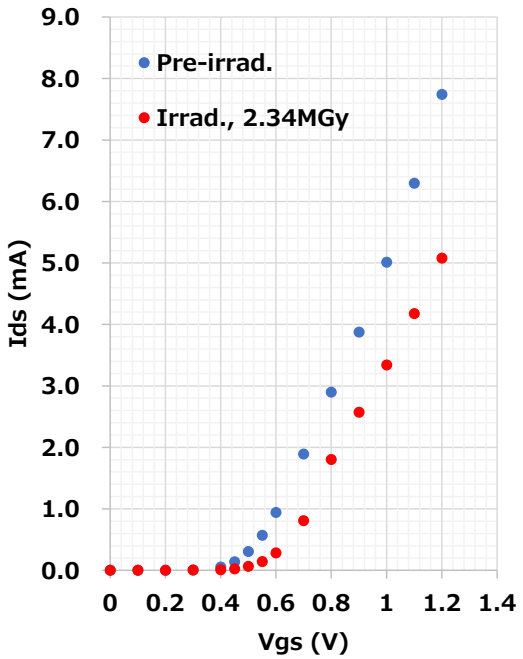


Challenges in radiation-tolerant wireless chipsets

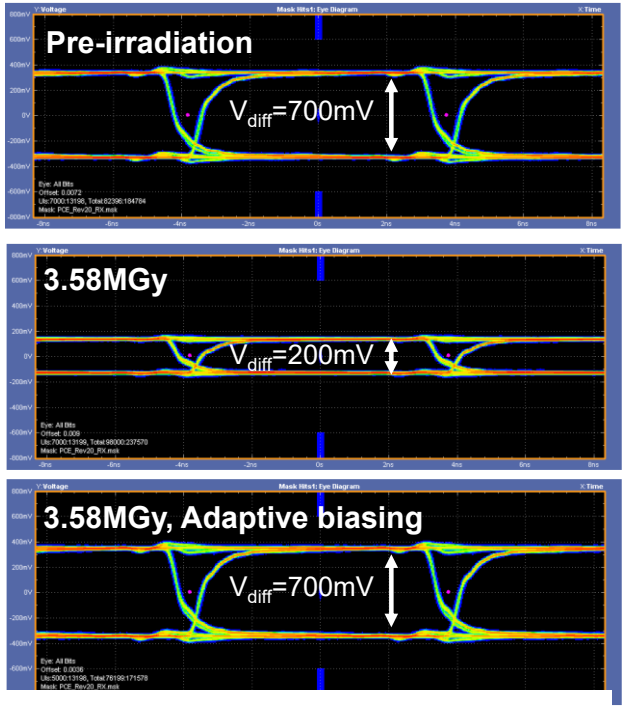
- Performance degradation by TID
  - Analog Circuits
    - Gain / bandwidth degradation
    - SNR reduction
    - Lower ADC/DAC resolution & speed
  - Digital Circuits
    - Reduced operating speed
    - Increased leakage current
    - Functional failures (esp. SRAM)
  - Clock Generation
    - Frequency drift
    - Increased jitter
- Development Costs
  - Man power
  - Verification
  - Expenses

High-level synthesis

1. Quantitative evaluation of communication performance
2. Extraction of bottleneck blocks
3. Improvement by circuit techniques

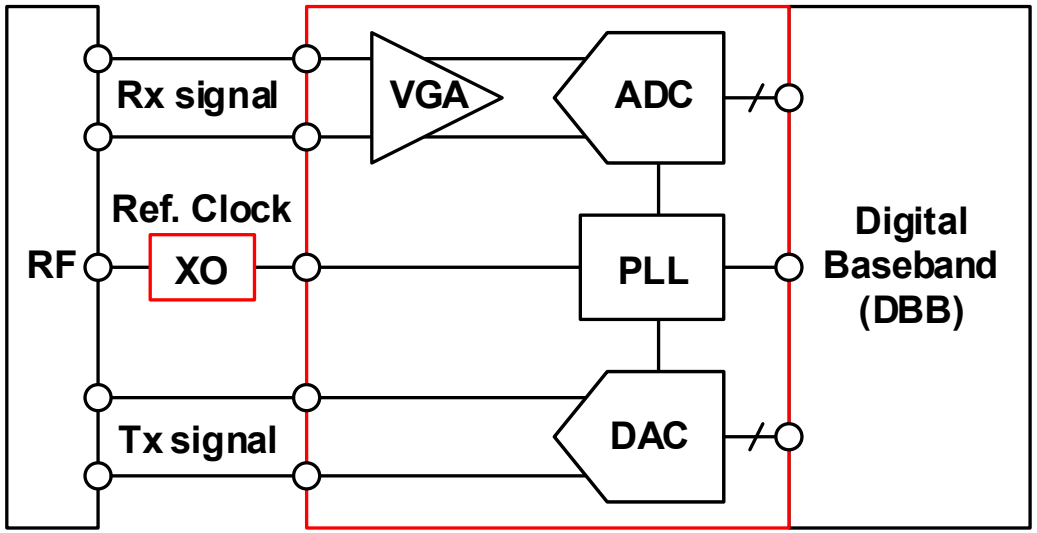


NMOS I-V after γ-irradiation

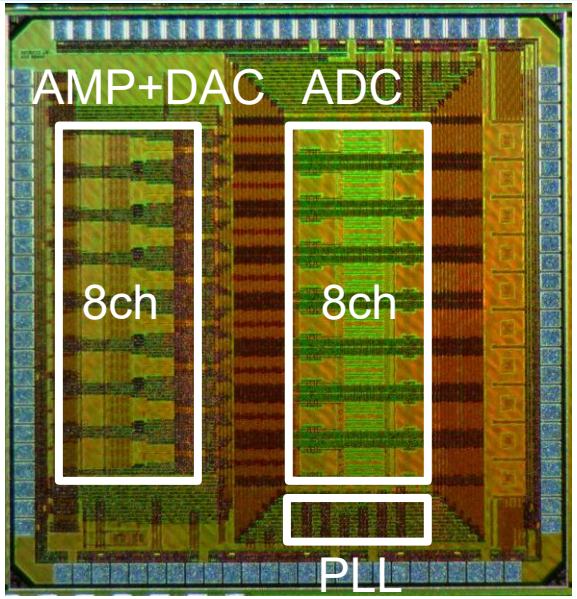


Driver output amplitude degradation

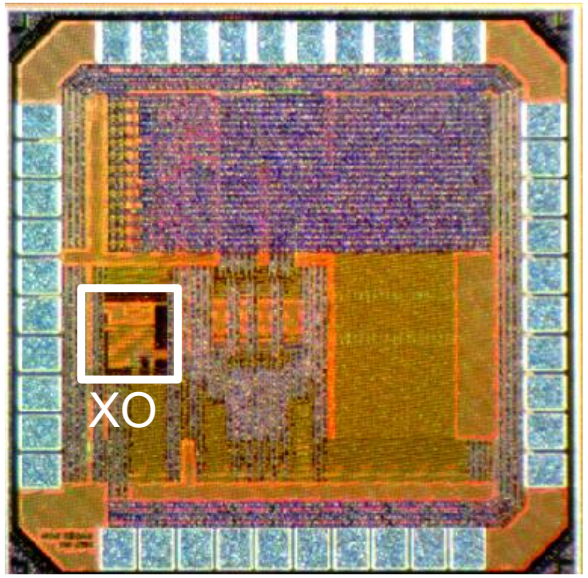
Development of the Analog Baseband chip



Analog Baseband component



RAPID



Data transfer ASIC

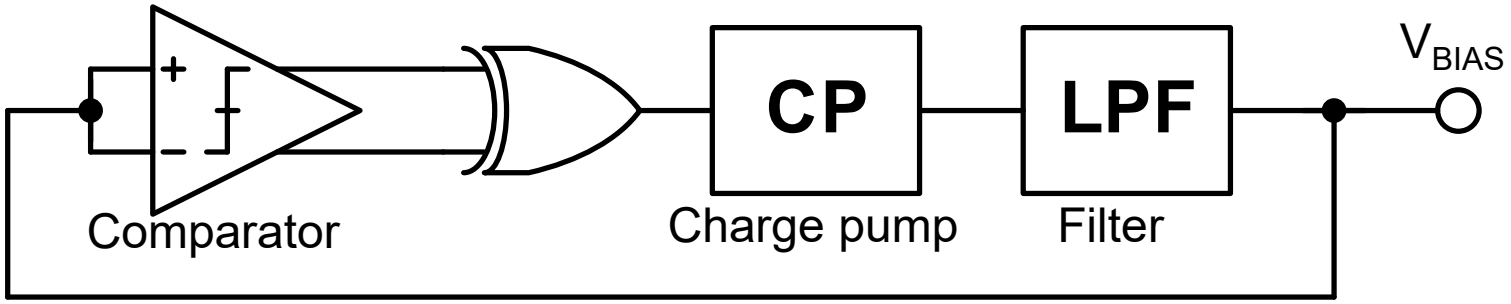
- **Component requirement（802.11n）**
  - VGA : 0～40dB, 40MHz Bandwidth
  - ADC : 10bit, ～80MS/s
  - DAC : 12bit, ～160MS/s
  - PLL : ～ 320MHz
  - XO : 40MHz, ～0.1ps Jitter

Customize!

- **Analog IP available at KEK**
  - High-speed Opamp for VGA
  - 10bit 100MS/s ADC
  - 12bit 2GS/s DAC
  - 1GHz PLL
  - 10MHz～156MHz XO

Radiation hardening of the ADC

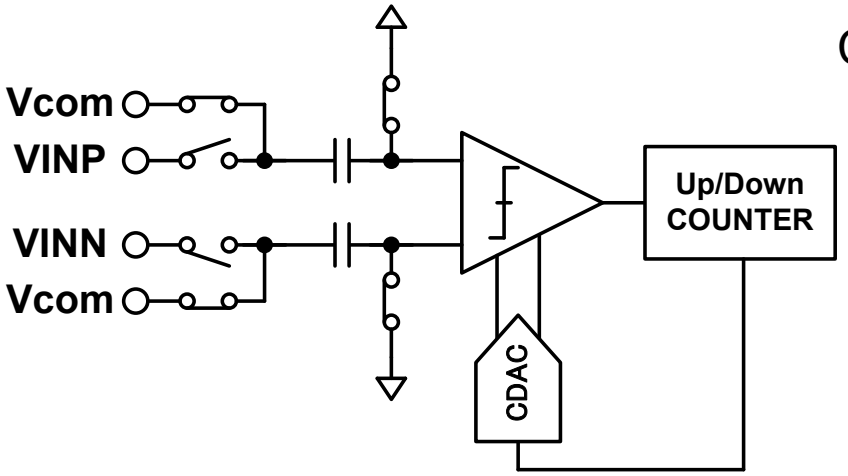
Mitigation for ADC speed degradation

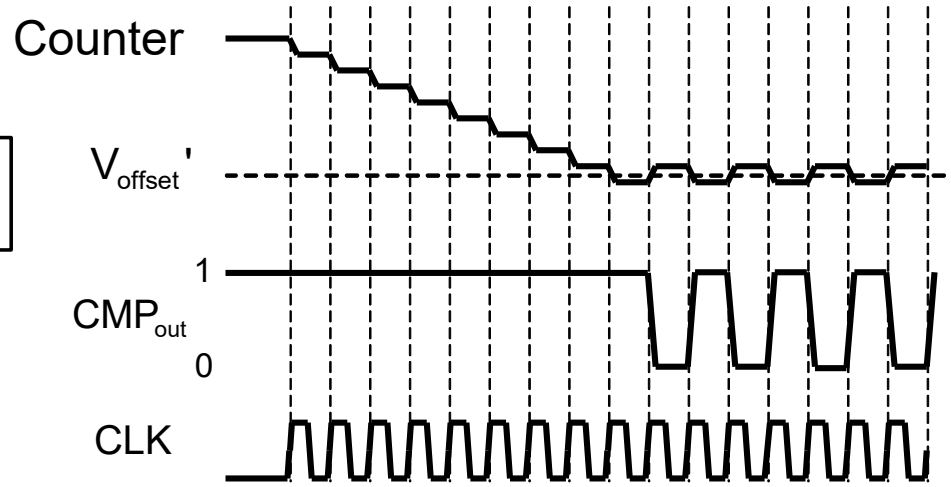


Feedback to compensate TID-induced threshold-voltage shift

- TID effects reduce circuit speed
- Detect speed degradation and compensate it to mitigate TID-induced impact

Mitigation for ADC accuracy degradation



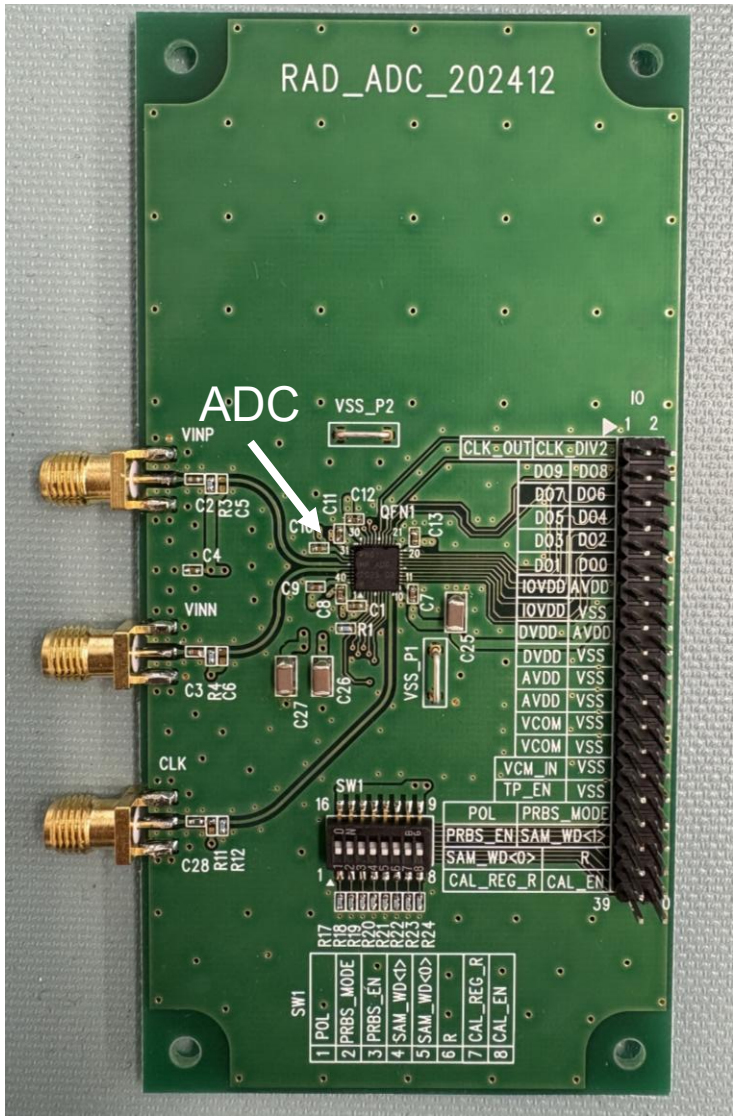


- TID increases device mismatch (e.g., Vth variation), reducing ADC resolution
- Automatically detect and compensate errors to maintain resolution

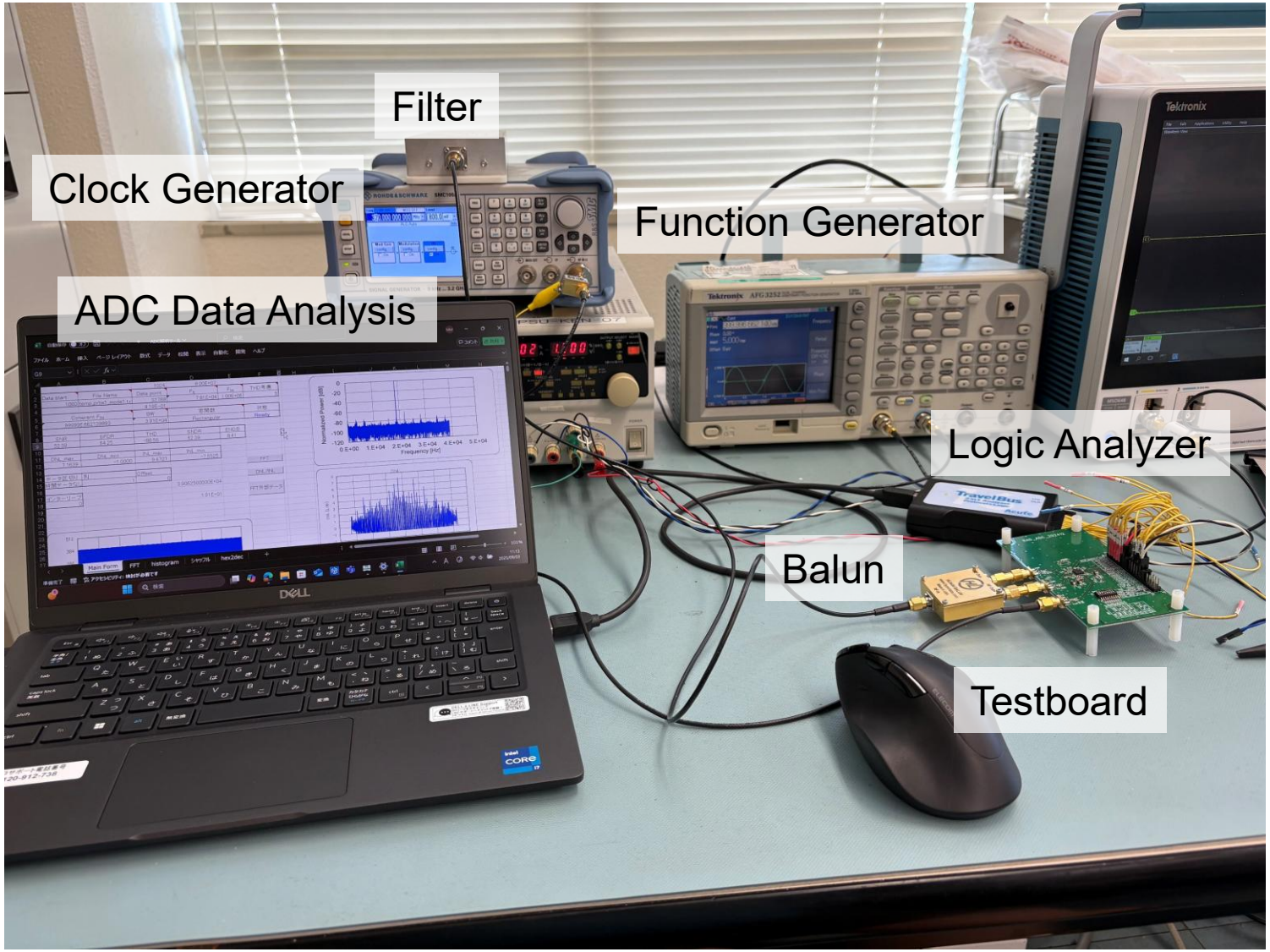
Rad-hard ADC Measurement setup

Analog Input

Clock



Rad-hard ADC test board



Rad-hard ADC Measurement setup

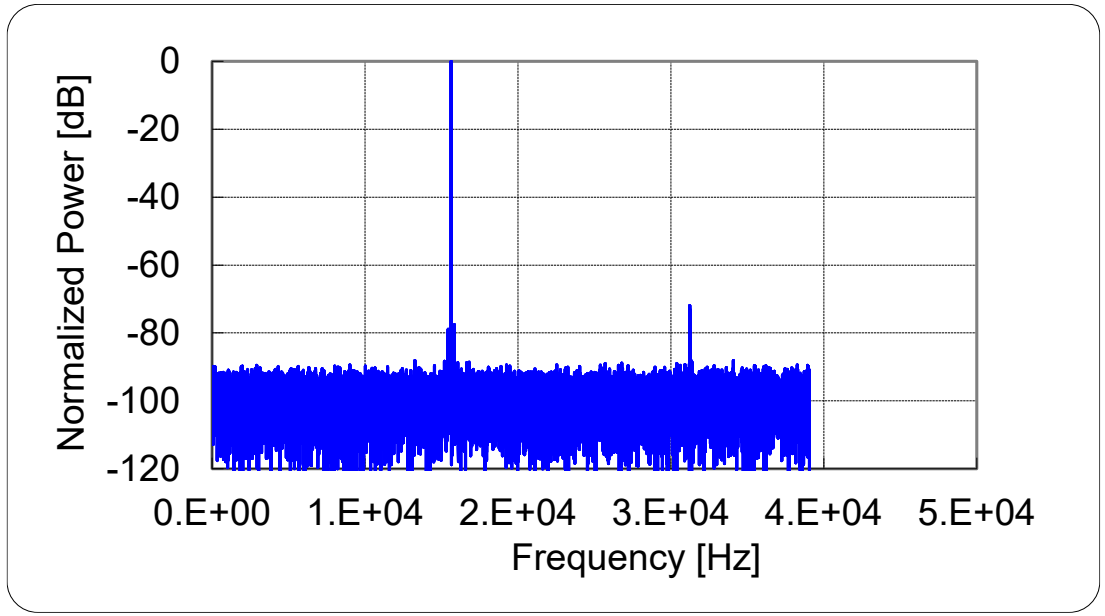
Performance comparison before and after γ-ray irradiation

The performance degradation is within an acceptable range.

Sampling rate: 80MS/s, Input Frequency: 1 MHz, Decimation: 1/1024
Power Consumption: ～3 mW with 1.2 V power supply

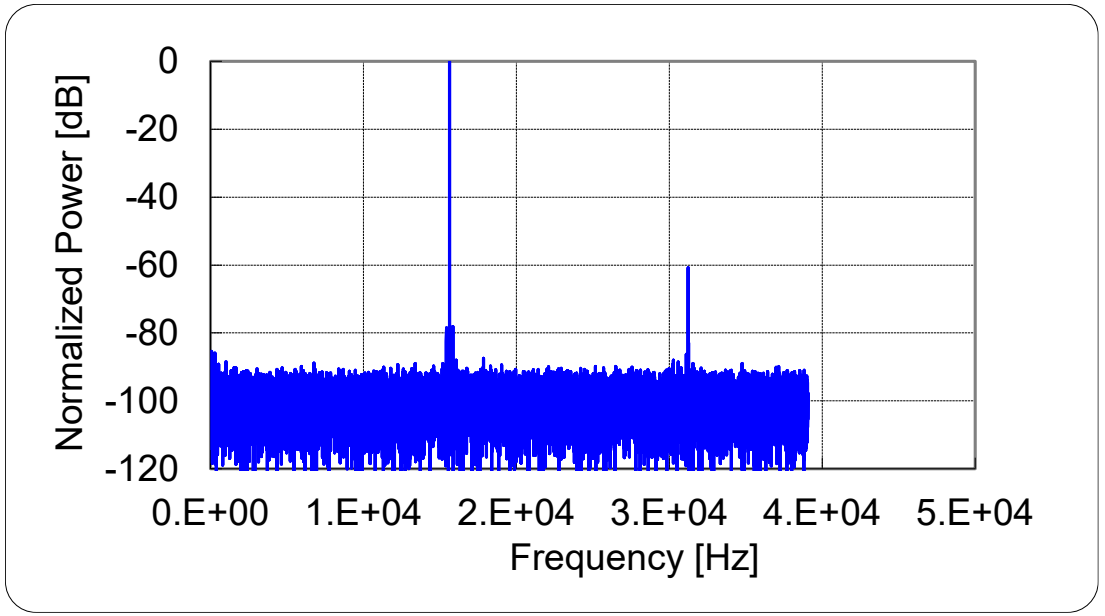
ENOB: Effective Number Of Bit

SNR	SFDR	SNDR	ENOB
55.7 dB	71.9 dB	55.5 dB	8.9 bit



Before

SNR	SFDR	SNDR	ENOB
56.0 dB	60.8 dB	54.8 dB	8.8 bit



After, 2.4 MGy (Co60, QST)

Chipset architecture and development framework

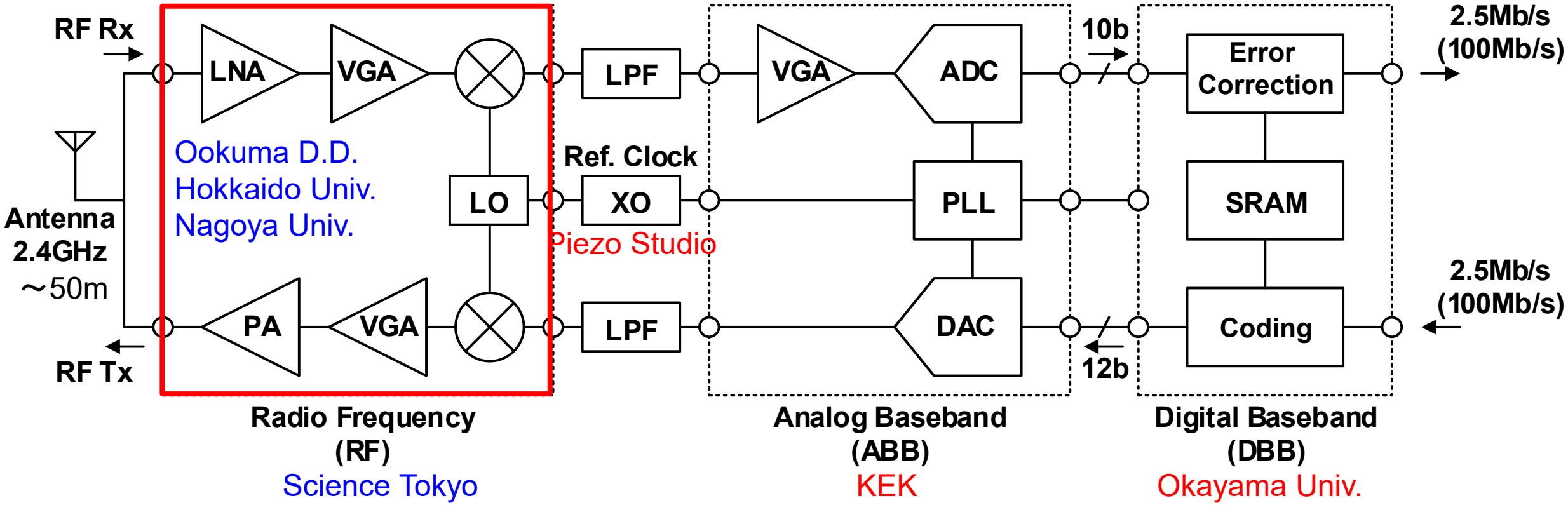
22.5 A 500kGy Radiation-Hardened 2.4GHz Wi-Fi Receiver for Innovative Nuclear Power Plant Decommissioning

Y. Narukiyo[1], S. Kato[1], K. Yanaka[1], Y. Takahashi[1], M. Miyahara[2], J. Mayeda[1], A. Shirane[1]

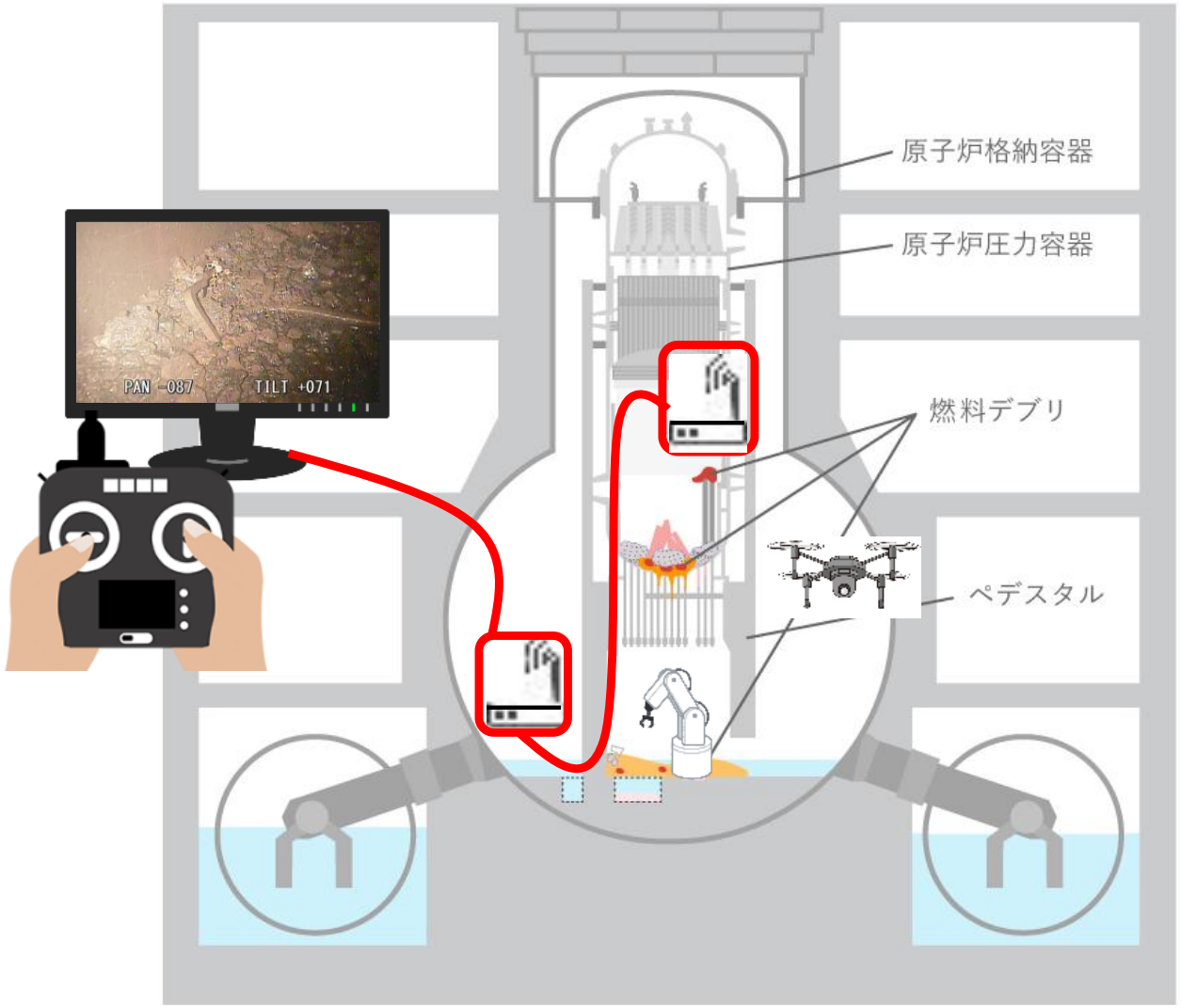
[1]Institute of Science Tokyo, Tokyo, Japan
[2]High Energy Accelerator Research Organization, Ibaraki, Japan

We will present the results of the RF block at ISSCC 2026!

https://www.isscc.org/

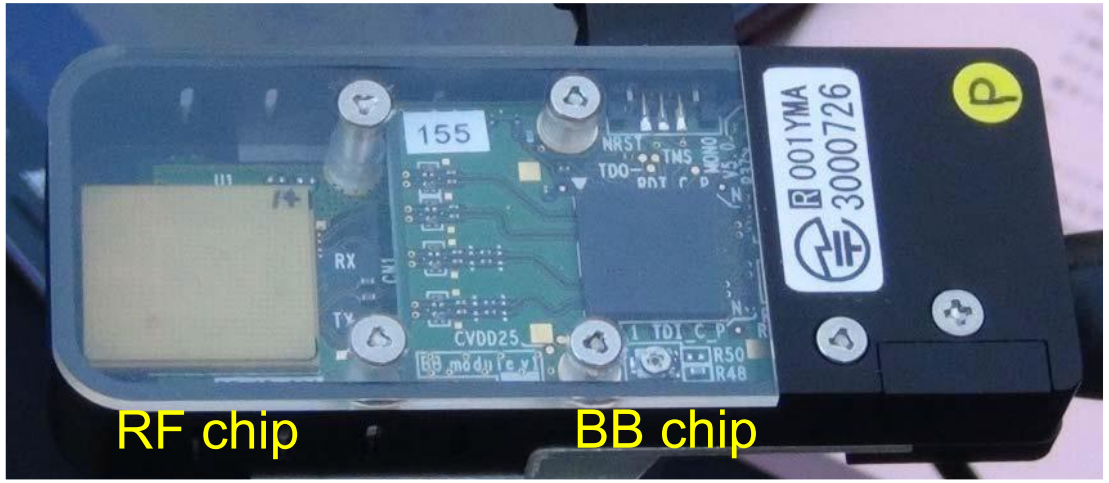


Practical implementation of the development



Conceptual View of Practical Implementation

- Master unit of the wireless system
- Supports video transmission data rates
- Targets: 2.5 Mbps (min) / 100 Mbps (stretch)
  - ✓ 480px → 2.5Mbps
  - ✓ 2160px (4K) → 35～45Mbps
- Two-chip architecture (RF + BB)
  - ✓ Both chips developed in the same CMOS process for future integration



Conceptual module image of RF and BB chips

Summary

- Development of ASICs for particle & nuclear physics
  - Including RAPID and other front-end chips for detector readout.
- Progress in Cryo-CMOS technologies
  - Circuits operating at cryogenic temperatures for quantum applications.
  - 10bit, 2 GS/s ADC operated at 4.2 K environment.
- Radiation-tolerant wireless chipset project
  - Leveraging KEK's existing ASIC IP to build analog baseband circuits for high-radiation environments.
  - 10bit, 80MS/s ADC normally operated after irradiation of 2.4 MGy.