Co-Designing Deep Learning Pipelines for the Belle II ARICH Detector on Virtex UltraScale FPGAs

Real-Time Cherenkov Ring Identification from Keras to Vitis HLS via *hls4ml*

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Who Am I? (Engineering, Heritage, and Hobbies)

My Roots & Academic Base

- **Ethiopia to Japan:** Representing the land of rich history, elite runners, and world-class coffee!
- **ECE @ AAU:** Senior specializing in tailoring AI algorithms directly onto hardware microchips.

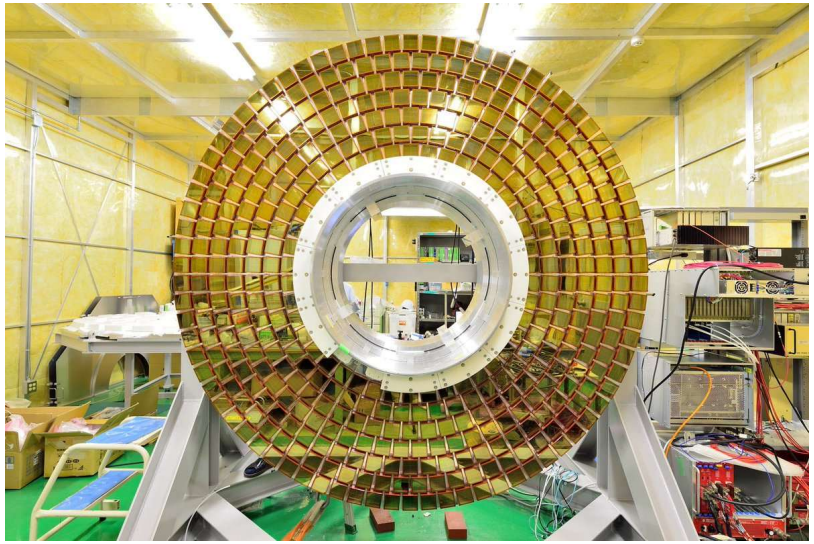
Hobbies & The Creative Spark

- **Music & Mountains:** Passionate about high-altitude hiking and playing complex rhythm patterns on my guitar.
- **The Connection:** Masterful guitar timing + physical trail endurance = building lightning-fast automated loops on hardware silicon!

The Core Mission: Filtering Real-Time Particle Data

The Challenge: High-Speed Particle Filtering

- **The Data Flood:** Particle collisions generate a massive amount of raw sensor data.
- **Microsecond Windows:** Decisions to save or discard data must be made within a few microseconds.
- **FPGA Trigger Purpose:** Software filtering is too slow, requiring a real-time hardware trigger built directly on the readout chips.



[The Real Belle II ARICH Detector Ring]

Core Project Objective

Train a compact AI model to identify Cherenkov rings and deploy it for real-time FPGA trigger purposes.

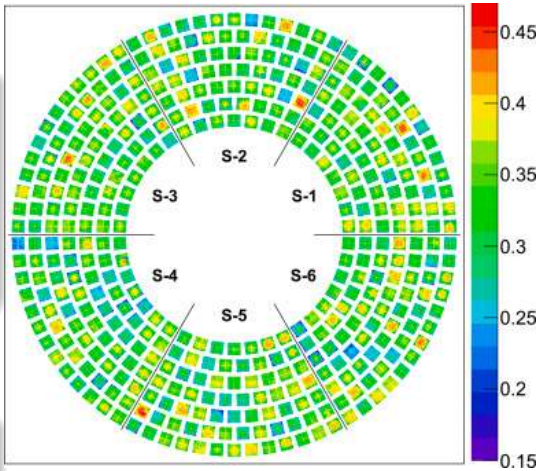
Data Visualization: From Raw Strikes to Reconstructed Rings

Managing the Volume

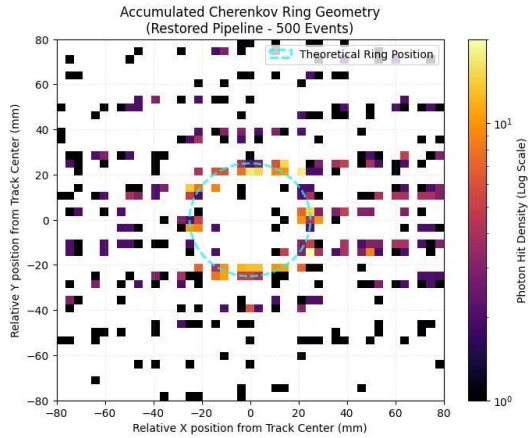
Cleaned and processed a massive dataset of **1.3 Million raw events** containing scattered particle coordinate matrices.

Pattern Isolation

Successfully filtered out noisy background signals to isolate and visually reconstruct clear, definitive geometric ring structures.



[Raw Sensor Grid Activity]



[Isolated Cherenkov Ring]

Figure: Left: Scattered hits recorded by the detector. Right: The clean ring isolated by our pipeline.

The AI Brain Architecture for Ring Recognition

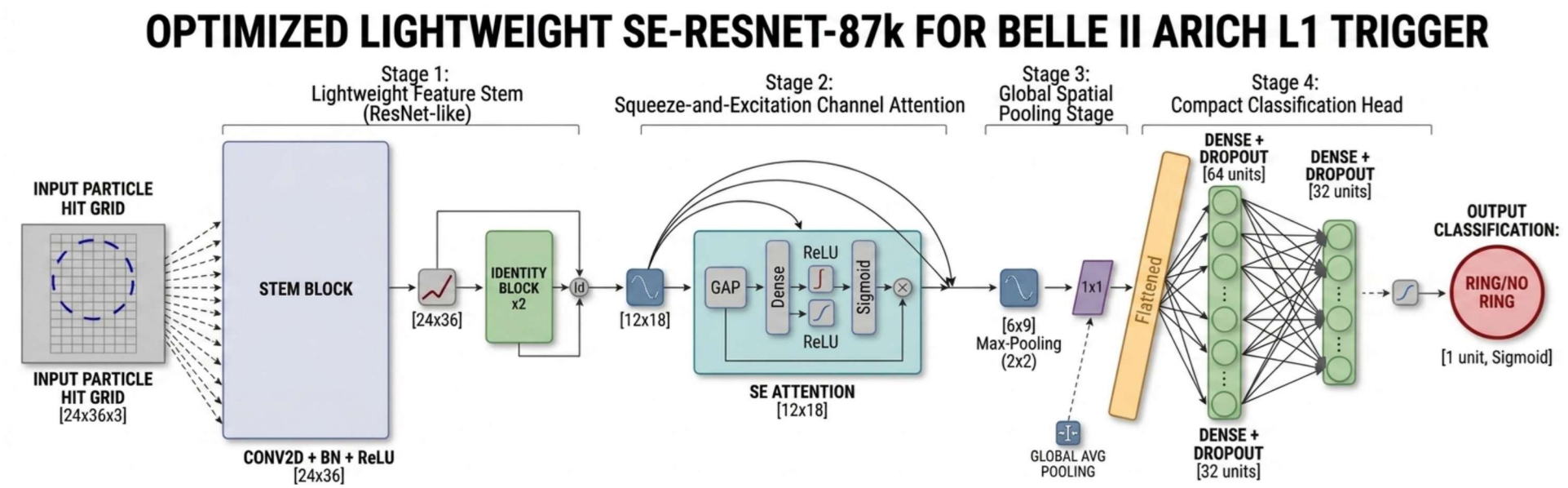


Figure: Our tailored, lightweight Neural Network topology optimized to analyze spatial hit grids and predict ring presence instantly.

Hardware Co-Design: Shrunk AI Performance

Optimizing AI for Silicon Microchips

- **Hardware Compression:** We drastically reduced the AI model's size and memory footprint to fit the strict physical limits of the microchip.
- **High Efficiency:** Despite this extreme shrinking, our best performance so far can reach an excellent **96.85% accuracy**.

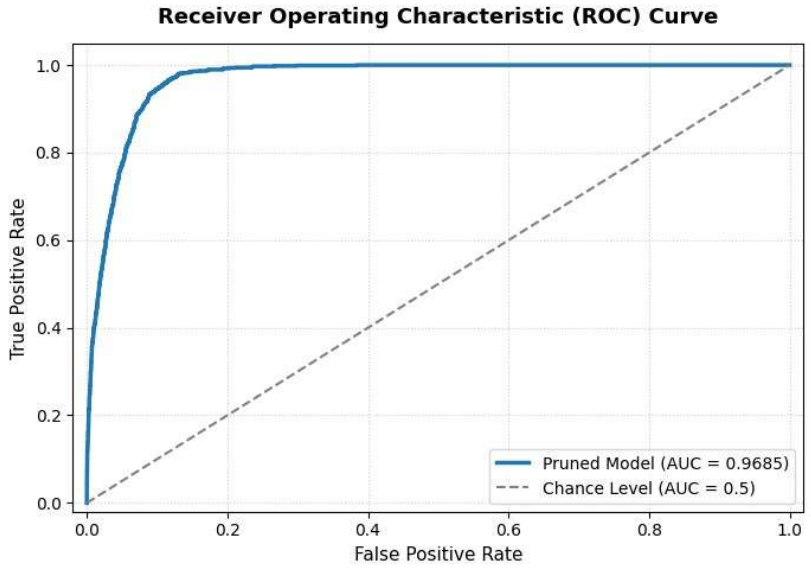


Figure: Accuracy stability relative to model size reduction.

Target Hardware Platform

Targeted Hardware Specifications

- **Target Board:** Belle II Universal Trigger Board 4 (UT4)
- **Core FPGA:** AMD/Xilinx Virtex UltraScale+
- **Application:** Real-time, sub-microsecond trigger execution

[Target Hardware: Belle II UT4 Board]

The Horizon: Future Plans & Acknowledgements

Ongoing Next Milestones

- Complete core high-level hardware synthesis to extract final speed and latency parameters.
- Integrate the compiled layout architecture directly into the physical trigger board.
- Benchmark real-world execution speeds against traditional software frameworks.

Thank You!

Questions Discussion

Acknowledgements

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