D_RD_27: Study of modern FPGA device and associated new technology, and search for possible application in High Energy experiments

Yun-Tsung Lai

on behalf of the D_RD_27 group

KEK IPNS

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2026 Joint Workshop of FKPPN and TYL/FJPPN

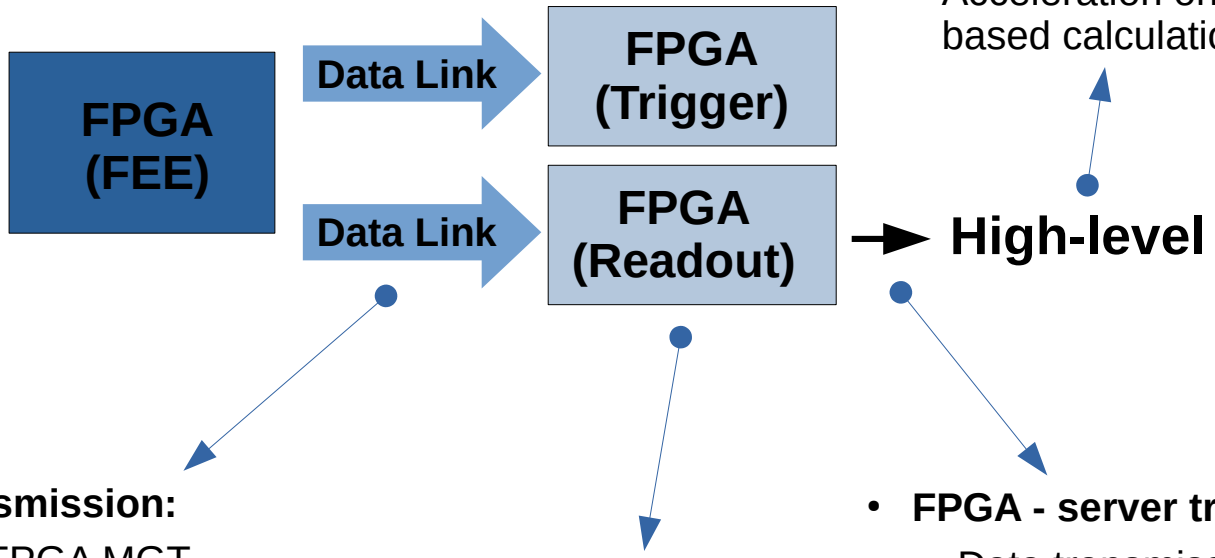
@ ACT CITY HAMAMATSU Congress Center

18th May, 2026

Application of FPGA in HEP experiments

- **Our target:** Study the latest COTS FPGA devices and their associated new technologies for possible application and upgrade in different aspects of HEP experiments.

- **Hardware acceleration:**
  - Not only CPU, but also GPU and FPGA.
  - Acceleration on software-based calculation.



- **FPGA - FPGA transmission:**
  - Optical link with FPGA MGT and optical modules.
  - Non-Return-to-Zero (NRZ).
  - Different encoding based on protocol design purposes. e.g. 8B/10B and 64B/66B.
    - <10 Gbps for DAQ.
    - <25 Gbps for TRG.

- Strong **FPGA devices** with:
  - Larger number of cells.
  - Larger data bandwidth.

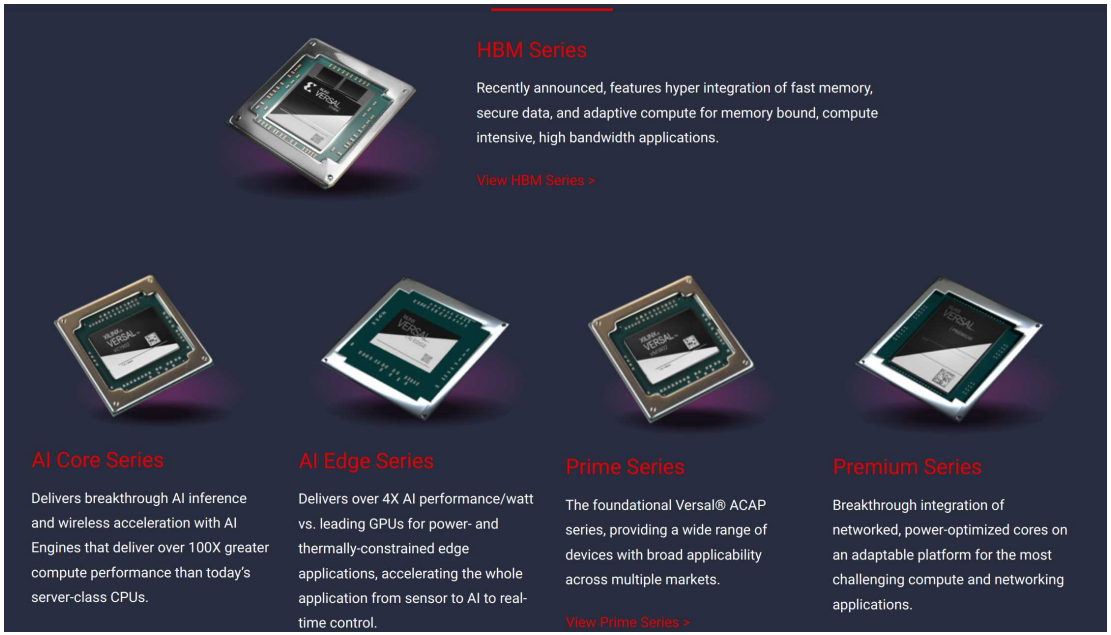
  are critical for the usage in:
  - **TRG**: complicated algorithm implementation.
  - **DAQ**: collect and process large data.

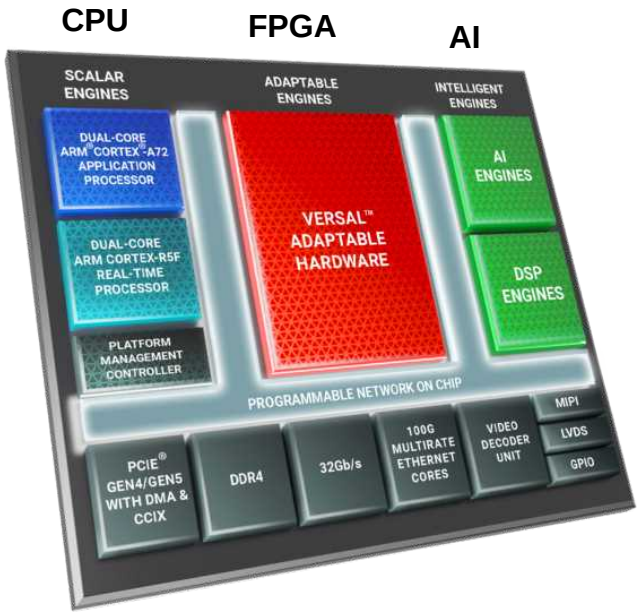
- **FPGA - server transmission:**
  - Data transmission and system slow control.
  - GbE, PCI-express, VME, etc.
  - PCI-Express is the most popular one nowadays: PCIe40 in ALICE, LHCb, and Belle II.

D_RD_27: Modern FPGA devices for HEP

- D_RD_27: Study on modern FPGA devices for application in HEP.
  - Mainly based on the **Xilinx Versal series of ACAP**.
- KEK together with Japanese HEP community purchased a few evaluation kits.
  - Plan: Common and general studies on the new technologies for future electronics device's R&D. Now we plan to use Versal for L1 TRG, DAQ or HLT purpose.

- The features of different Versal series ACAP:
  - AI engine: convenient interface to implement ML core into firmware.
  - High Bandwidth Memory (HBM).
  - Larger number of cells + High transmission bandwidth.





source: Xilinx website

D_RD_27 members

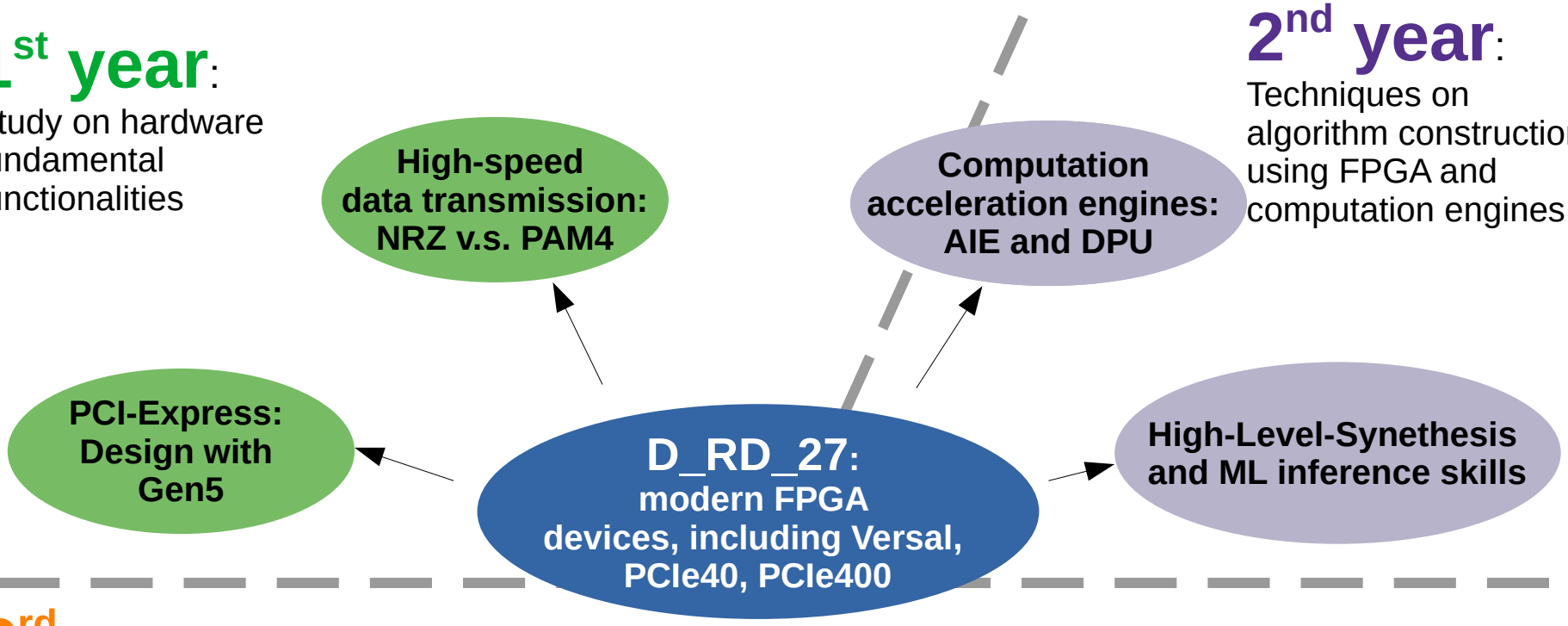
- Activities in 2025:
  - Japan→France: Visited IJCLab for resource sharing of IDROGEN project and discussion on Belle II readout upgrade after LS2.
  - France→Japan: Viisited KEK for the deployment of IDROGEN/WhiteRabbit in SuperKEKB system.

France			**Japan**		
Name	Institute		Name	Institute	
Daniel Charlet	IJCLab Orsay	PCIe readout device for Belle II / LHCb, IDROGEN project	Yun-Tsung Lai	KEK IPNS	E-sys, Belle II
Patrick Robbe			Manobu Tanaka		E-sys
Tak-Shun Lau			Makoto Tomoto		ATLAS
Emi Kou			Satoru Yamada		Belle II
			Yutaka Ushiroda		Belle II
			Kunihiro Nagano		ATLAS
			Taichiro Koga		Belle II
			Yu Nakazawa		Belle II
Julien Langouet	CPPM Marseille	PCIe400 readout upgrade	Ryotaro Honda		E-sys
Renaud Le Gac			Mikhail Remnev		Belle II
			Hiroshi Kaji	KEK ACCL	SuperKEKB
			HIdetaba Baba	RIKEN	Nuclear experiment

Project overview and working plan

1st year:
Study on hardware fundamental functionalities

2nd year:
Techniques on algorithm construction using FPGA and computation engines



3rd year: R&D works for utilizating Verasl in real experimental systems

- New Level-1 Trigger device for Belle II: UT5
- Upgrade for Belle II HLT with FPGA
- SuperKEKB Bunch Oscillation readout system
- Belle II Readout Upgrade
- High-Speed Ethernet

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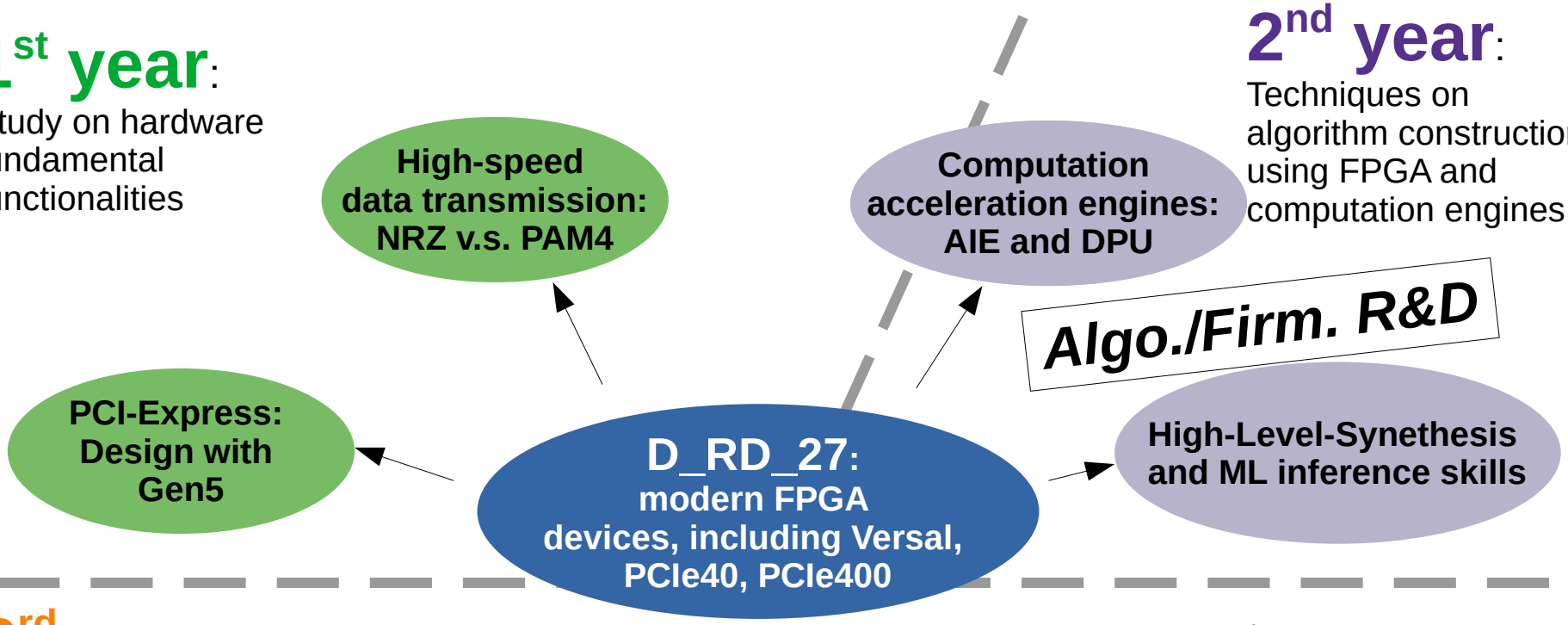


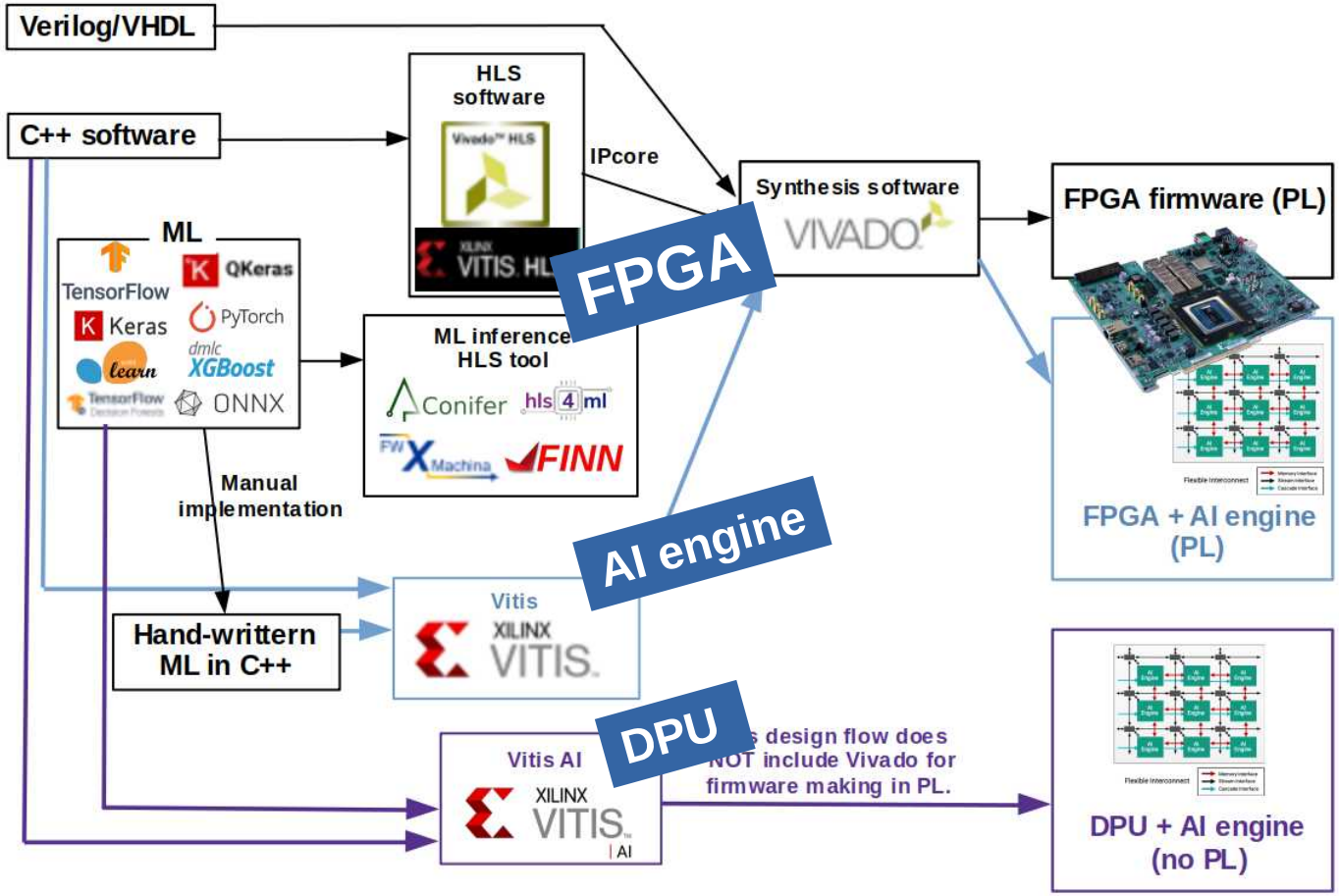
3rd year: R&D works for utilizating Verasl in real experimental systems

Hardware R&D

- New Level-1 Trigger device for Belle II: UT5
- Upgrade for Belle II HLT with FPGA
- SuperKEKB Bunch Oscillation readout system
- Belle II Readout Upgrade
- High-Speed Ethernet

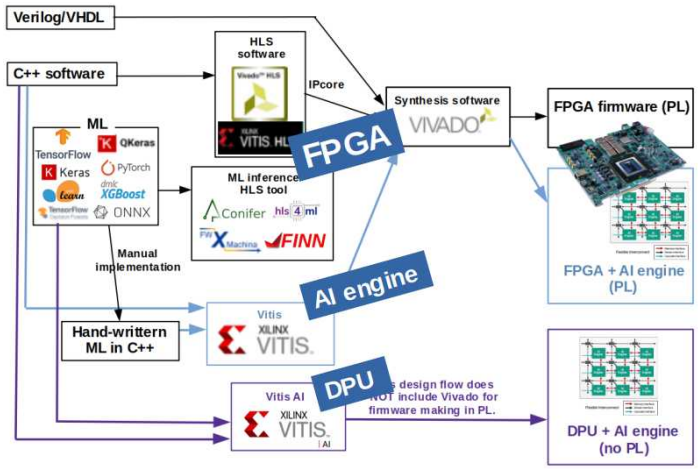
HLS, ML, AI engine: roadmap of FPGA methodology

- Not only "what kind of logic to make", but also "how to make it".
- We hope to perform basic study on each of the items, collect experience, build a database of techinical knowledge, and prepare material to support our experimental colleagues.
  - We believe this kind of effort on fundamental technique is essential.
  - Completed in 2025 with a summer school!



Summer school on HLS, ML in FPGA, AIE

- Based on the technical database we collected, we held a summer school in 2025.
- In total 25 people from Japan and other countries.
  - Also people from different time zone!
- Content: HLS, hls4ml, Conifer, FINN, Versal AI engine
- Device: Nexys4 boards from Digilent
- We plan to have it once per year.



Algo./Firm.: Efforts so far

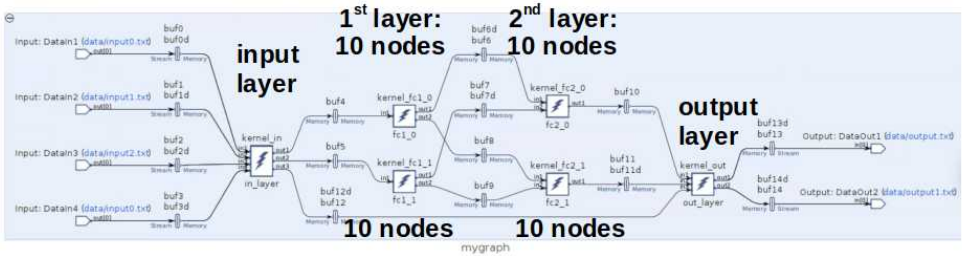
- The original designs are based on HLS inference tools for FPGA implementation. Then, plain C++ is written in Vitis for Versal AI engine.

NN for tau trigger in L1

R. Nomaru (Univ. of Tokyo)

- Neurons: 19,20,20,1

Keras hls4ml

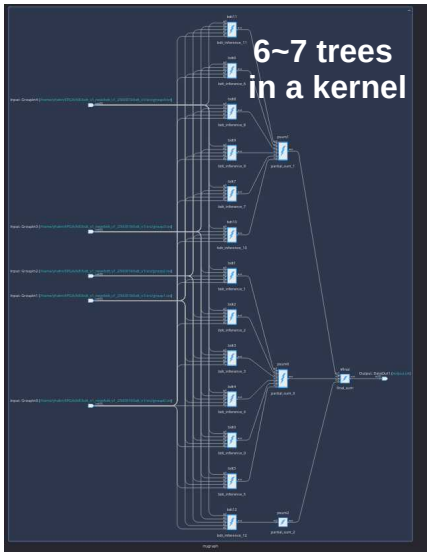


BDT for tau trigger in L1

- N of estimator = 90
- Depth = 3

Y. Ahn (Korea Univ.)

scikit learn Conifer



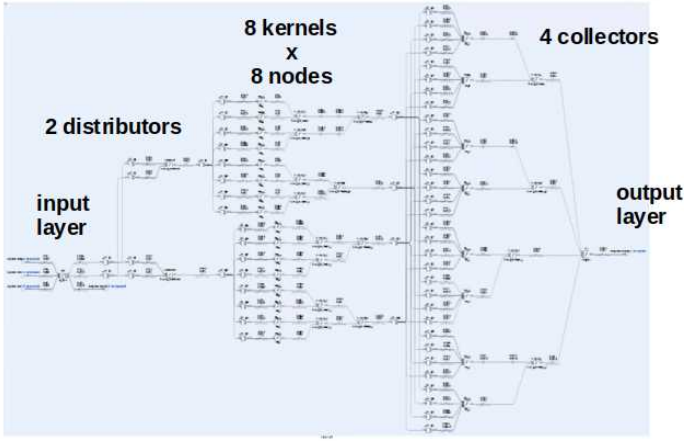
NN for KLong-Muon chamber trigger

- Neurons: 8,64,16,3

A. Little (Univ. of Sydney)

Keras hls4ml

8 kernels
x
2 nodes

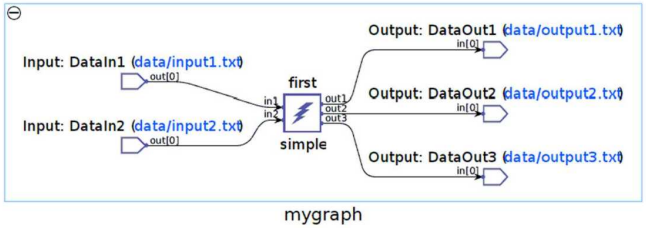


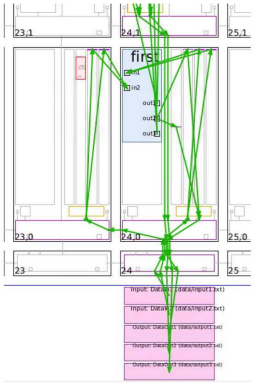
Linear fitter

J. Song (Korea Univ.)

XILINX VITIS HLS

- Based on linear algebra
- C++ in Vitis HLS

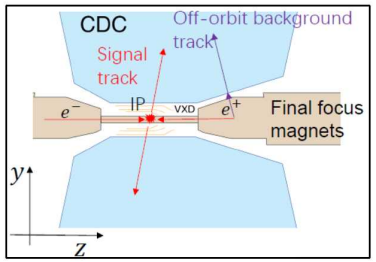


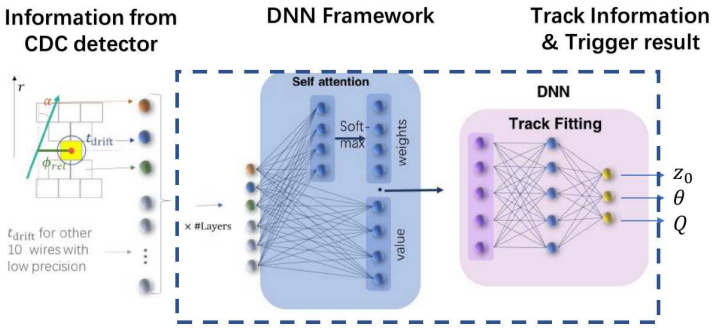


Algo./Firm.: Exploration on more ML methods

- Belle II L1 trigger: Deep-Learning NN for 3D tracking (z-trigger).
  - Original design based on Pytorch and hls4ml.

PyTorch hls4ml

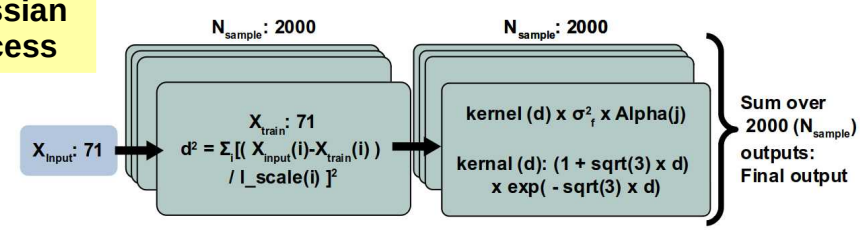




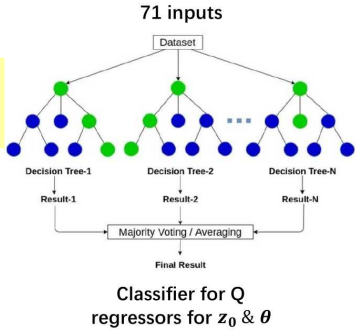
Original design: Y. Liu (SOKENDAI)

- Our works: Exploration on more new ML methods with deployment on Versal FPGA and AI engine:

Gaussian Process

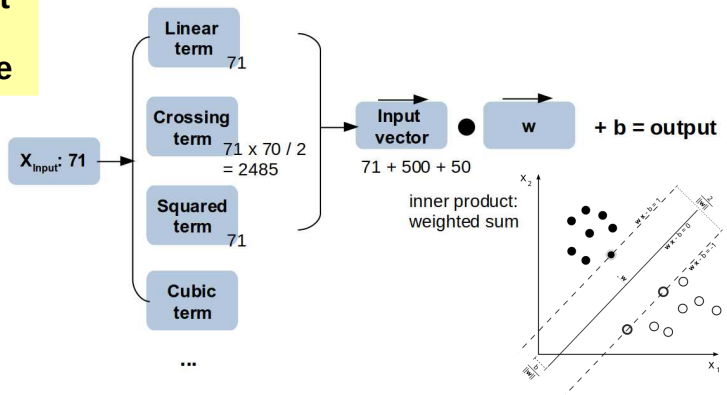


Decision Tree

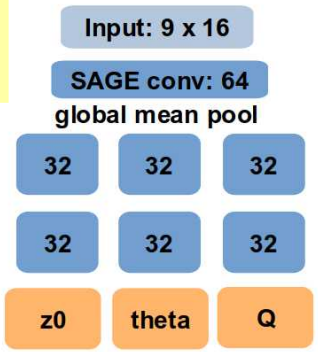


Yang Yi (Fudan/KEK)

Support Vector Machine



Graphic Neural Network



HW: Belle II Level-1 Trigger board UT5

Belle II UT3

Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

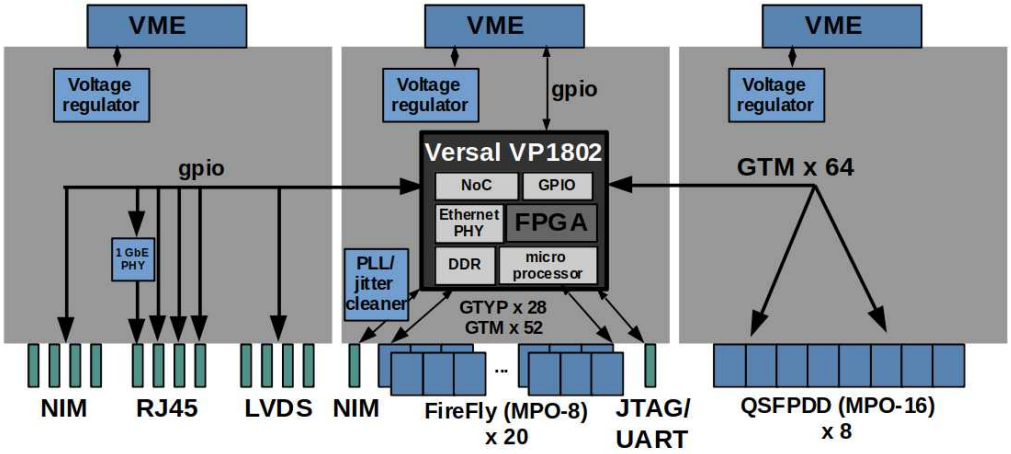
Belle II UT4

Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

- QSFP28
- No Processing System (PS)
- VME 6U

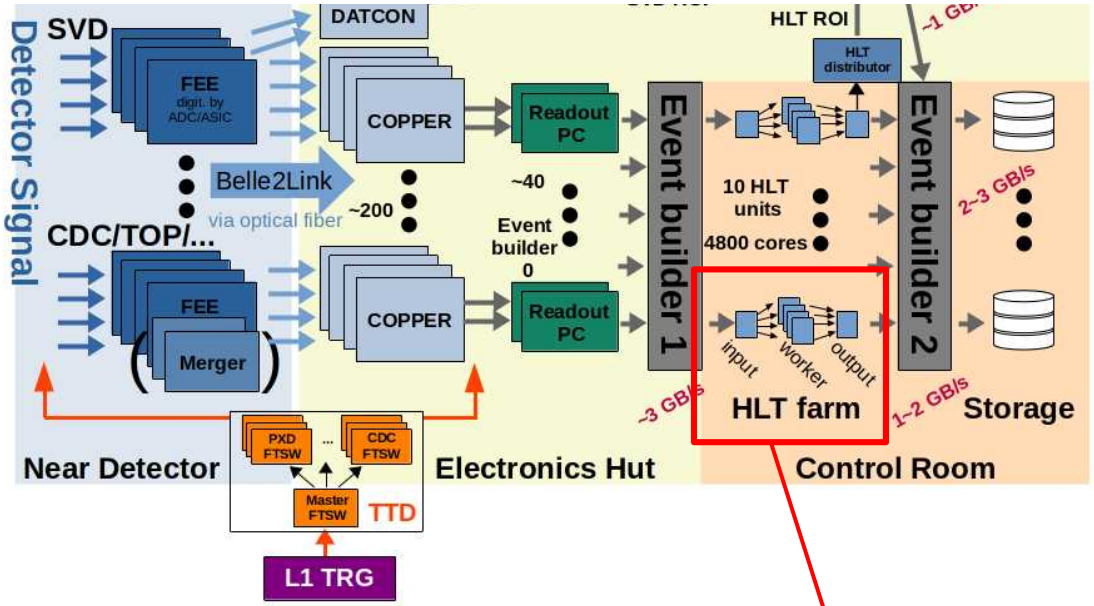
New design: UT5

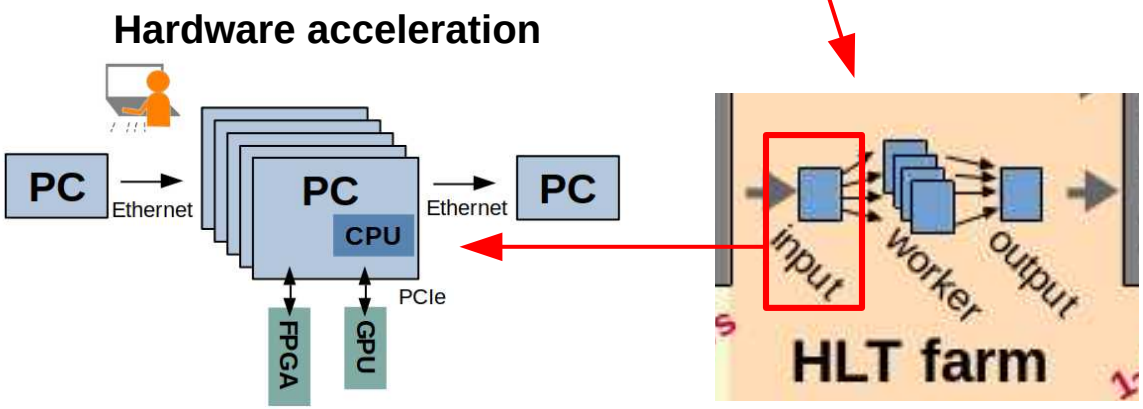
Preliminary block diagram



- **Already discussed with private company about the general design.**
  - **Spec. has been defined.**
  - **Now design is ongoing.**
  - **VP1802**
  - **Prototyping in 2026**
- QSFP28 → FireFly. QSFP-DD for PAM4.
- VME 6U, FMC
- LVDS, Ethernet PHY, NIM IO, etc
- No AI engine in UT5. Still open for UT6

HW: Belle II HLT upgrade

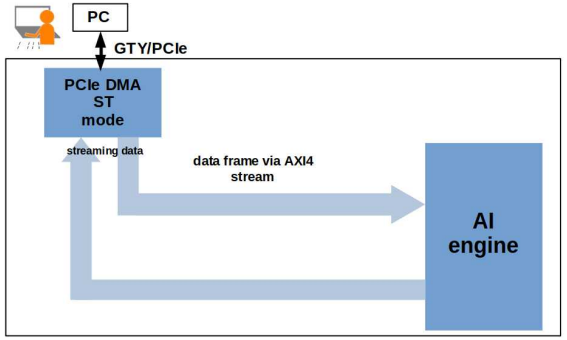




- HLT in Belle II DAQ system:
  - HLT input: From readout
  - HLT worker nodes: The major processing part
  - HLT output: Toward storage
- Potential scenario of Belle II HLT upgrade:
  - Hardware acceleration with GPU or FPGA as exetnsion in HLT input, not worker nodes.
  - Implementing L3 filter algorithm as event filter.

HW: Belle II HLT, L3 in Versal

- Our development plan: Using Versal with AI engine for L3 filter at HLT input.
  - Hardware framework:
    - Server - FGPA data exchange via PCI-Express.
    - Main logic processing deployment in AI engine.

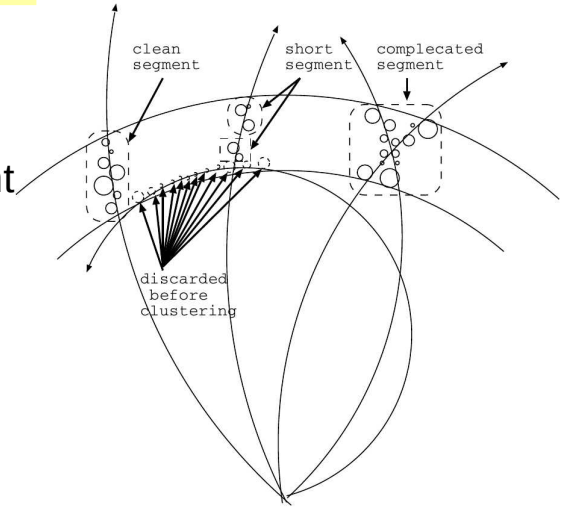


- L3 filter logics:
  - Fast tracking with drift chamber and clustering with calorimeter.

M. Remnev (KEK/BINP)

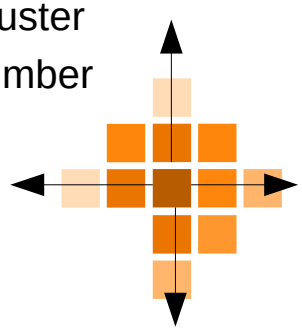
L3 tracking

- Simplifed segmen-based tracking
- Ignore low-pt segment
- 2D track with r-ϕ
- 3D track with s-z



L3 clustering

- To reduce loops and accesses to panther tables for faster unpacker.
- Connecting hits into cluster
- No limitation on the number of hits in a cluster
- 4 directions for neighbor hits

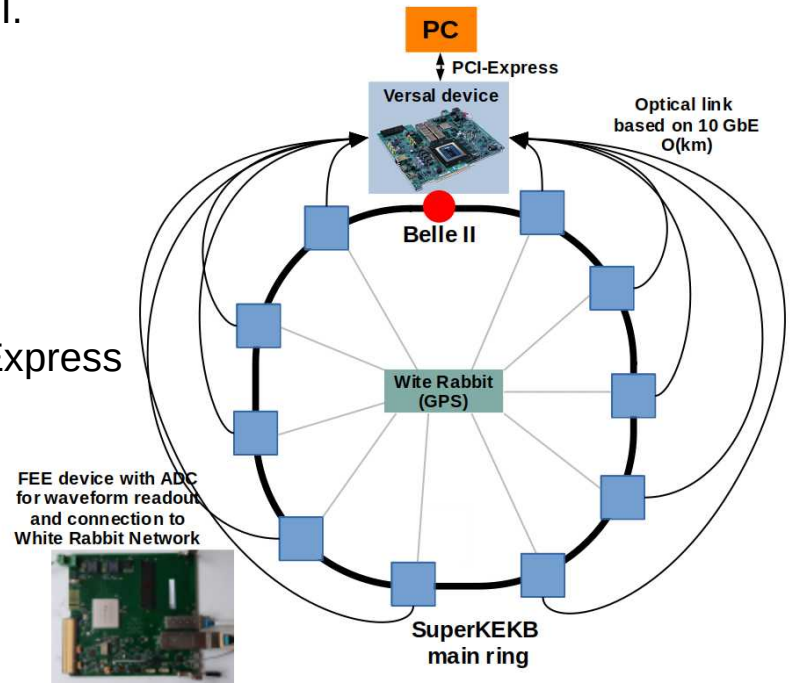


HW: SuperKEKB Bunch Oscialltion Readout system

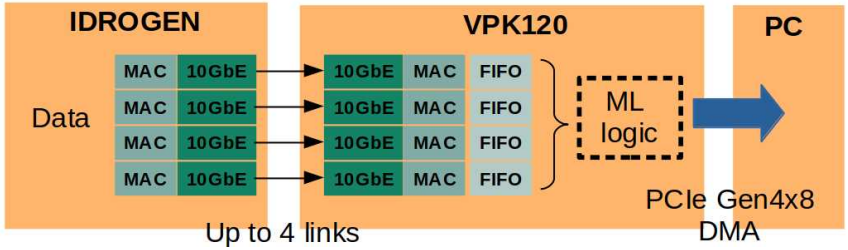
- Motivation: To handle the sudden beam loss problem in SuperKEKB, we plan to prepare a system to readout the bunch waveform of oscillation
  - Final target: real-time prediction on the sudden beam loss using FPGA readout system.
    - Protection on the inner detectors of Belle II.
  - Feature study for sudden beam loss issue.

- System:
  - FEE: IDROGEN + ADC + WhiteRabbit
  - Long-distance optical link
  - Readout: Versal (ML-based logic) with PCI-Express

- Collaborators:
  - Univ. of Hawaii: K. Yoshihara
  - KEK ACCL
  - KEK E-sys/CEF
  - IJCLab.



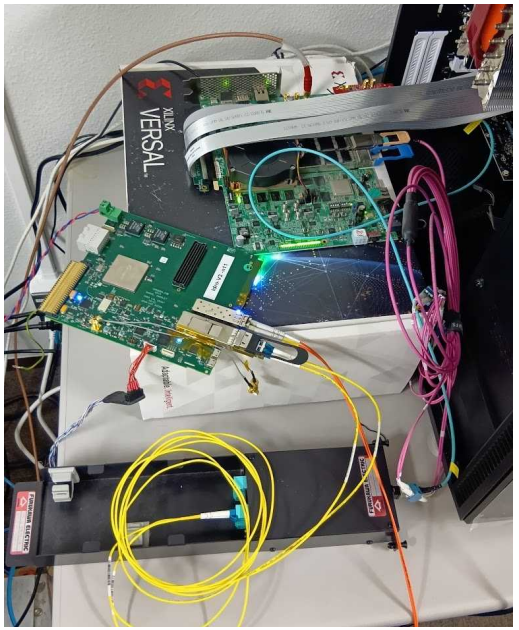
- Progress up to 2025:
  - Data readout chain with simplifed IDROGEN firmware was established:

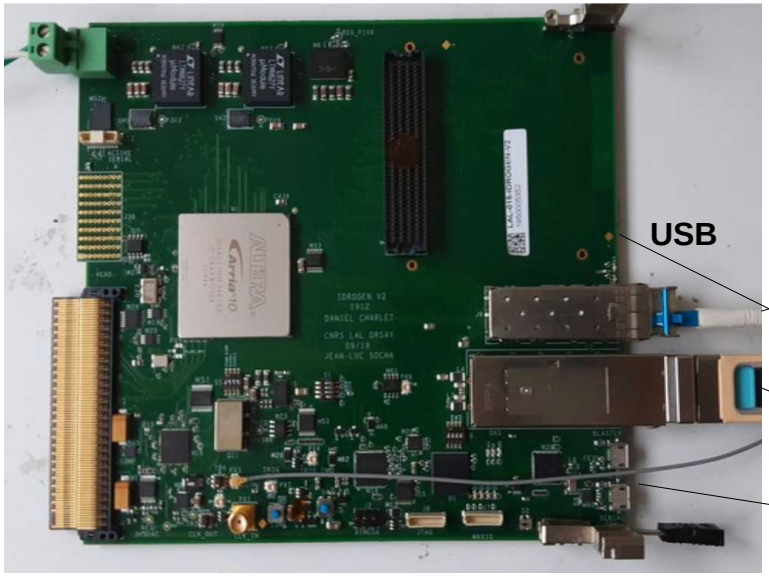


HW: SuperKEKB Bunch Oscialltion Readout system

- Our progress so far:
  - Visited IJCLab in Jan. 2026 to discuss about the full resource sharing for IDROGEN:
    - Firmware, software, etc.
  - We received the full firmware and compiled it.
  - Doing test with SuperKEKB test bench.
  - Duplicating the working test bench to KEK E-sys.

Devices at KEK E-sys





USB

SFP

QSFP 1x

USB

WhiteRabbit

Host PC:
- idrogentool: SLC via IPbus
- idrogenconfig: SLC via USB
- PAON software: ADC config
- picocom: WB config

HW: New PCIe device for readout upgrade

source: CPPM Marseille group

- CPPM Marseille group has received the first prototype of PCIe400 in Jan. 2025.
  Progress up to 2026:
  - Error-less high bandwidth serial interfaces (PCIe Gen4, 48 lpGBT up/downlink, QSFP112 4x100G)
  - lpGBT transmission
  - White rabbit node

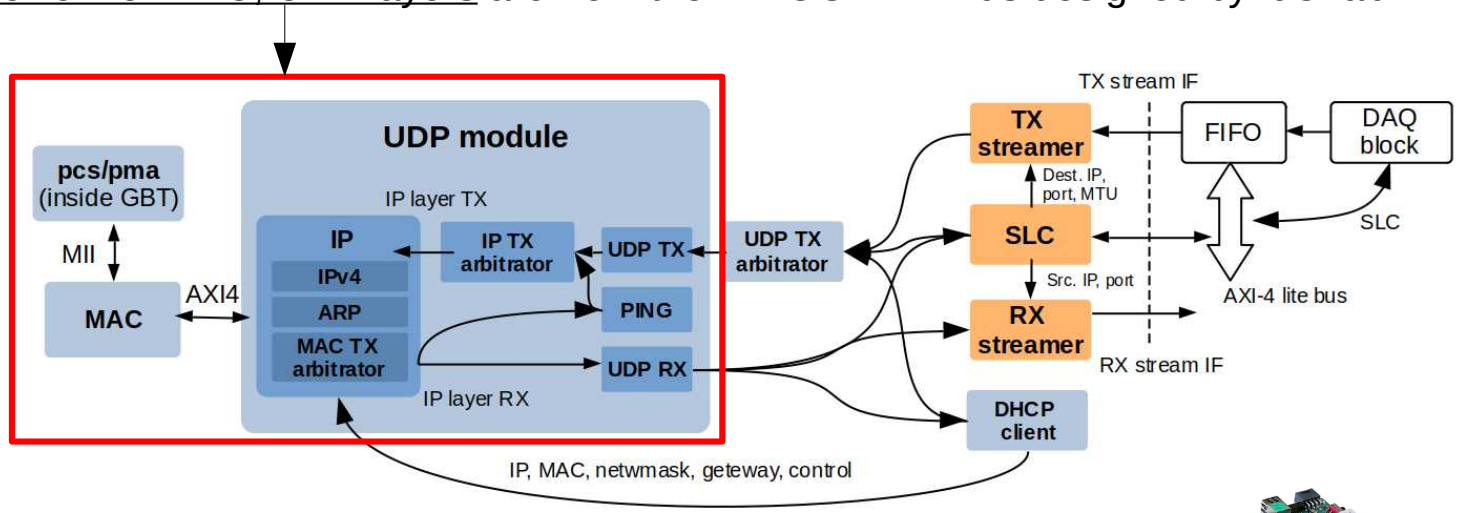
- LHCb has no plan to use PCIe400 for LHC Run 4 nor 5: No production of PCIe400 foreseen
  - PCIe400 studies might continue in background for DRD7 projects

- At KEK/Belle II:
  - Discussion is ongoing regarding acquiring a new board of PCIe400 or FELIX at KEK for feasibility study in 2026 FY.
  - Keep communication with CPPM Marseille and netFELIX community.

HW: High-speed Ethernet

- New sub-project: Development a general-purposed UDP-based ethernet protocol.
  - Collaboration with nuclear physics experts from RIKEN (H. baba) and KEK E-sys (R. Honda), and technical consulation from IJCLab.

- Framework of MAC, UDP layers are from the IDROGEN IPBus designed by IJCLab:



- Our development plan @ KEK:
  - **1 GbE, 10 GbE**: Design mostly complete
  - Moving forward to **40 GbE and 100 GbE**
  - Higher speed: **Embedded Ethernet of Versal**
    - **MRMAC (Multi-Rate Ethernet MAC): 100G**
    - **DCMAC (Data Center Ethernet MAC): 600G**
  - We will expand the design into a general one for all the Ethernet standard.
  -

Xilinx Versal VPK120: MRMAC and DCMAC

Summary

- In our project of D_RD_27, we study the modern FPGA devices for their potential application in experimental HEP for future upgrade.
  - Mainly based on Versal, and also other new PCIe devices.

- We have been cultivating the technical methodologies of ML inference in FPGA devices with a knowledge database, and provided educational activity as contribution to our community.

- As we have performed fundamental studies in various aspects, we are moving toward R&D projects for algorithm, firmware, and hardware for different applications.
  - Algorithm/Firmware (Trigger): Level-1 Trigger logic
  - Hardware (Trigger): Belle II new Level-1 trigger board with Versal
  - Hardware (HLT): Belle II HLT upgrade with L3 filter
  - Hardware (Trigger/Readout): SuperKEKB Bunch Oscillation Readout system
  - Hardware (Readout): High-Speed Ethernet with Versal's embedded Ethernet cores
  - Hardware (Readout): New PCIe-Express readout board