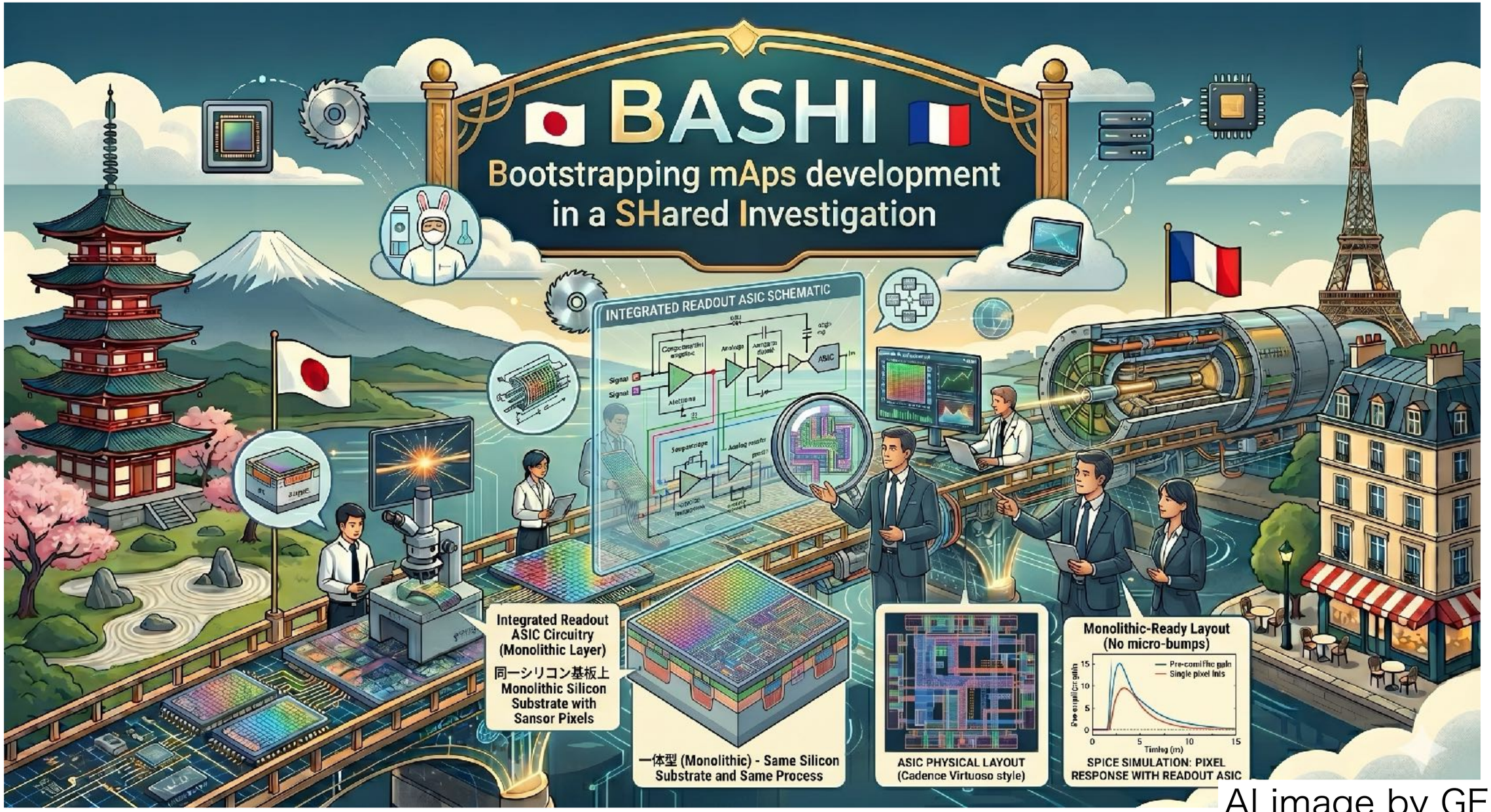


AI image by GEMINI

Manabu Togawa (KEK)
for the BASHI project (D_RD_29)

May 19, 2026
Joint Workshop of TYL/FJPPN and FKPPN 2026

BASHI project

- A collaboration for development CMOS monolithic active pixel sensors (MAPS) btw French and Japanese teams.

- Goals : Co-developments for
  - “OBELIX” for Belle II experiment
  - “MAPS with amplification” for high speed response sensor
  - “TPSCo65” for ALICE experiment
- The inaugural MAPS academy

Project institutes and members

ITDC

KEK

- **Tomoto Makoto (PI)**
- Kazunori Hanagaki
- Yuji Enari
- Yuta Okazaki

ATLAS

- Manabu Togawa
- Koji Nakamura

Belle II

- Katsuro Nakamura

IPHC

- **BAUDOT Jerome (PI)**
- BESSON Auguste
- SHAMAS Hasan
- HU-GUO Christine
- EL BITAR Ziad
- MOREL Frédéric
- SENYUKOV Sergey
- MAIRE Antonin

U. Tsukuba

- Tatsuya Chujo
- Motoi Inaba

ALICE

U. Hiroshima

- Yorito Yamaguchi

U. Tokyo (CNS)

- Taku Gunji

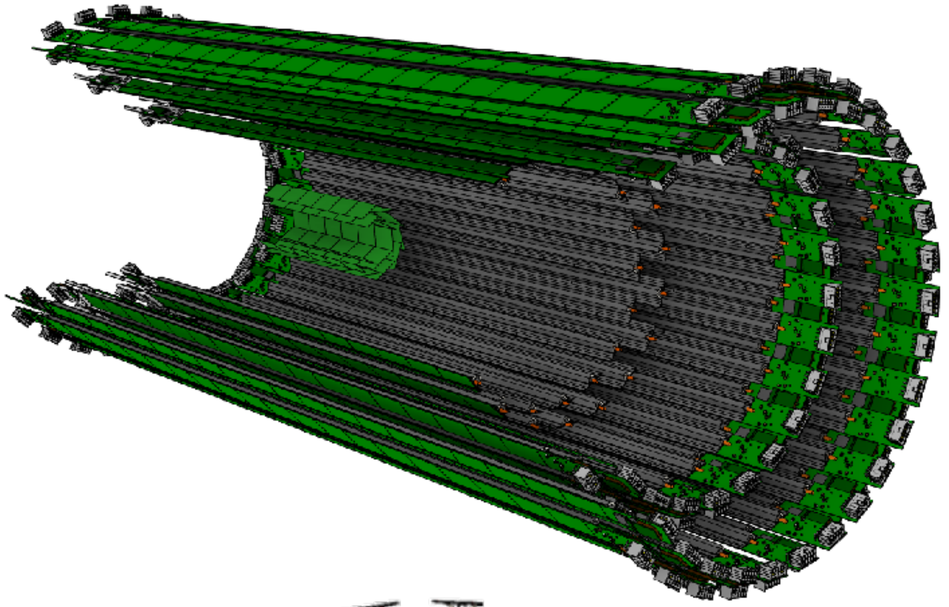
LPSC

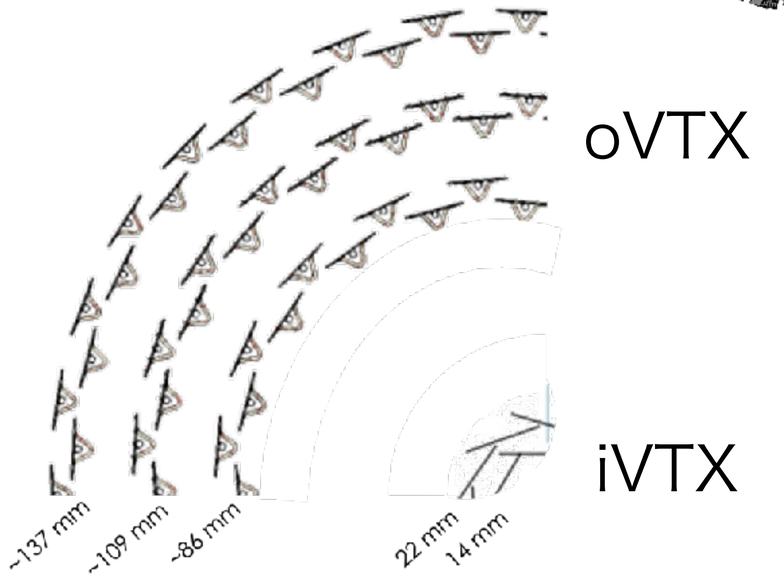
- GUERNANE Rachid

OBELIX for Belle II upgrade

- VTX upgrade
  - Six layers, with full pixel detector.
  - Higher space and timing granularities.
  - Total material budget : 3.5 % X_0
- Radiation level
  - Total Ionization dose (TID) : 100 Mrad.
  - Non-ionizing energy loss (NIEL) : 5 x 10^{14} n_{eq} cm^{-2}

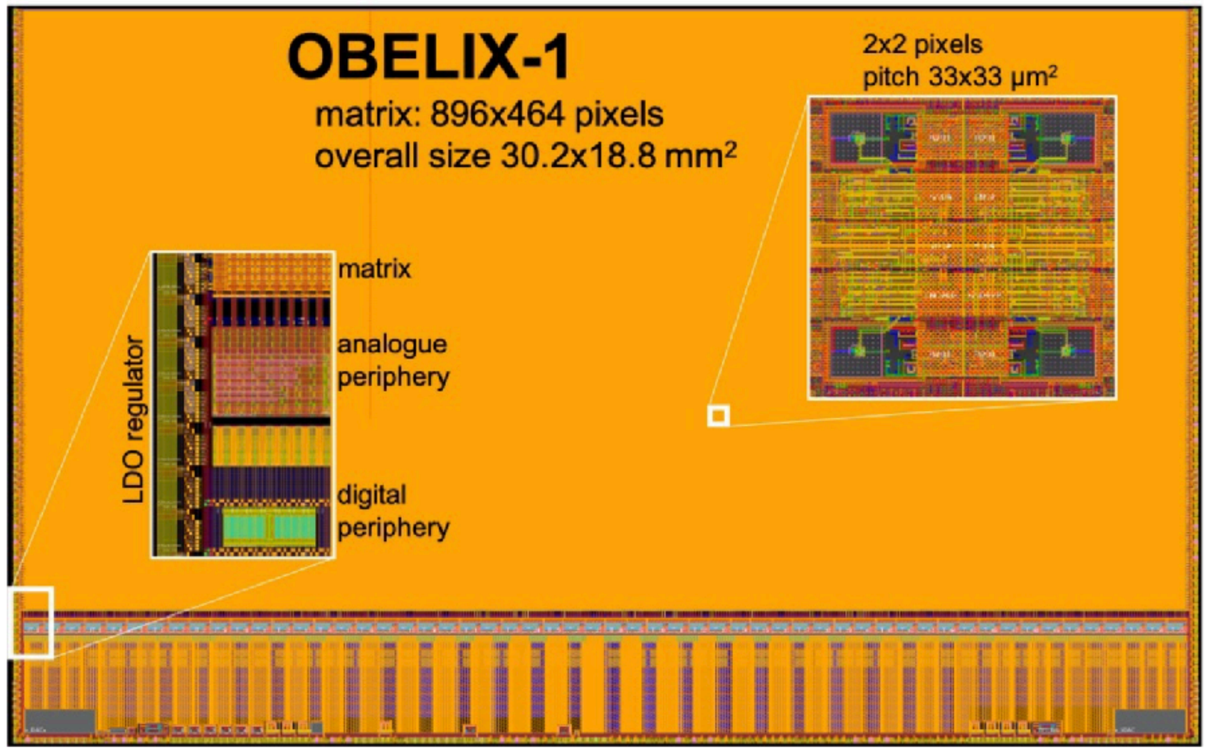
- Thin MAPS sensor : Optimized BELle II pIXel chip (OBELIX)
  - OBELIX is based on TJ-Monopix2 for HL-LHC ATLAS





Optimized BELle II pIXel chip : OBELIX

	TJ-Monopix2	OBELIX (target)
Year	2020	2026 (1st prototype)
Pixel pitch	33 µm	33 µm
Sens. area	17x17 mm^2	30.2x18.8 mm^2
Signal digits	7-bit ToT	7-bit ToT
Integration	25 ns	50 to 100 ns
Bandwidth	320 MHz	320 MHz
Power	200 mW/cm^2	< 200 mW/cm^2
Hit rate capability		120 MHz/cm^2
TID fluence	0.1 MGy 10^{15} n_{eq}/cm^2	< 1 MGy < $5x10^{14}$ n_{eq}/cm^2



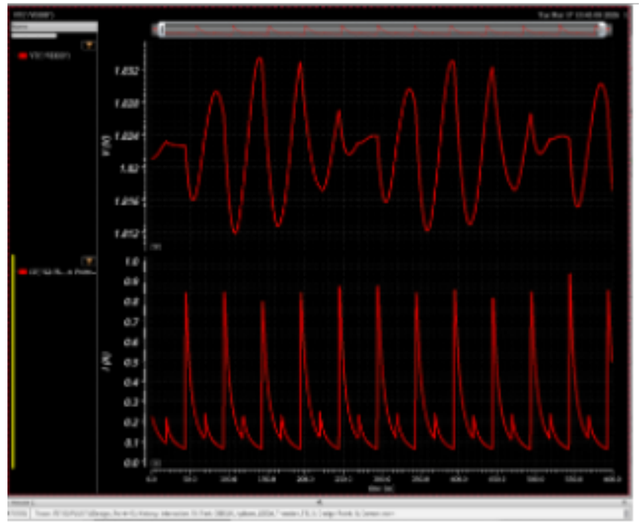
- Implementing new digital periphery and trigger logic
- New powering scheme based on on-chip regulation
  - Low Drop Out (LDO) regulators for all power inputs.
  - Essential element of powering for easy sensor integration.

Design of OBELIX-1 sensor

- OBELIX-1 submission delay due to additional efforts
  - Review of OBELIX-1 in October 2025 with strong KEK participation
  - Recommendations implemented in the next 5 months

- Mitigation of cross-talk observed in TJ-Monopix2.
- Large effort for verification of digital functionalities
  - Initially underestimated wrt various functions, operation w/ and w/o trigger, precision timing.
- LDO regulator is difficult to “stabilize”
  - **Strong work by KEK Ph.D student Xiangyu Xu, co-supervised by IPHC**

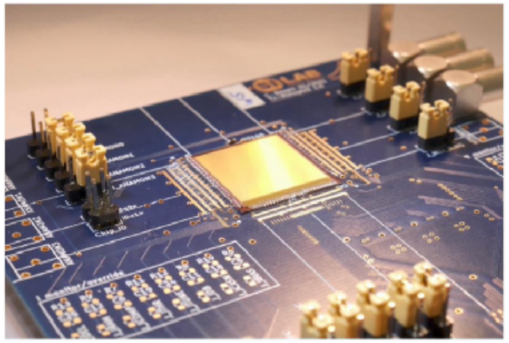
Simulation of LDO regulations to oscillating input charge



- **Finally OBELIX-1 was submitted at May 1st.**
  - **The delivery date is on discussion, expected at Oct.**

TJ-Monopix2 beam test at DESY and KEK PF-AR test beam line

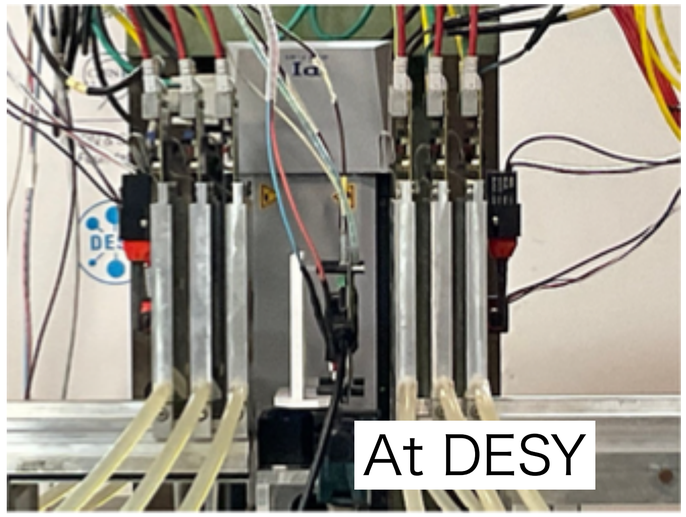
TJ-Monopix2

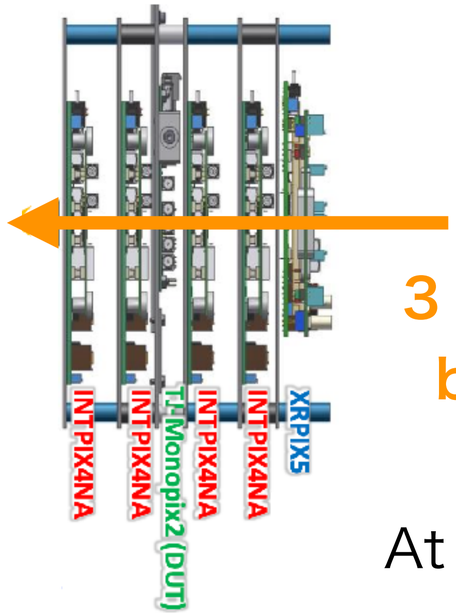


- Chip size : 2 cm × 2 cm
- Pixel pitch : 33 μm × 33 μm
- 512 × 512 ch
- ~ 1 μW/pixel (90 mW/cm2)
- 25 ns time stamping

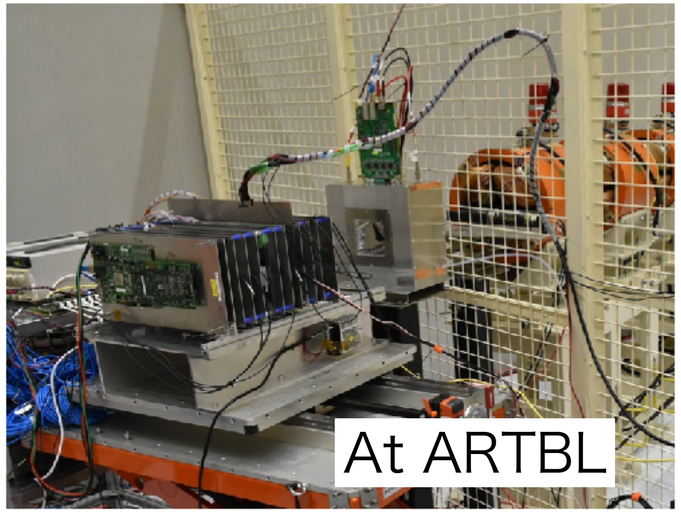
Different irradiated samples studied

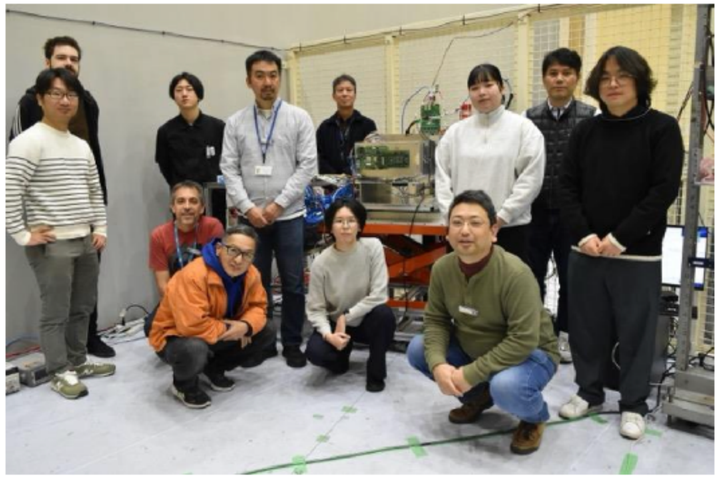
TJ-Monopix2 samples	Irradiation type	NIEL flux n_{eq}/cm^2
Chip-1	24 MeV proton	$1x10^{14}$
Chip-2	24 MeV proton	$2x10^{14}$
Chip-3	24 MeV proton	$5x10^{14}$
Chip-4	90 MeV electron	$5x10^{14}$





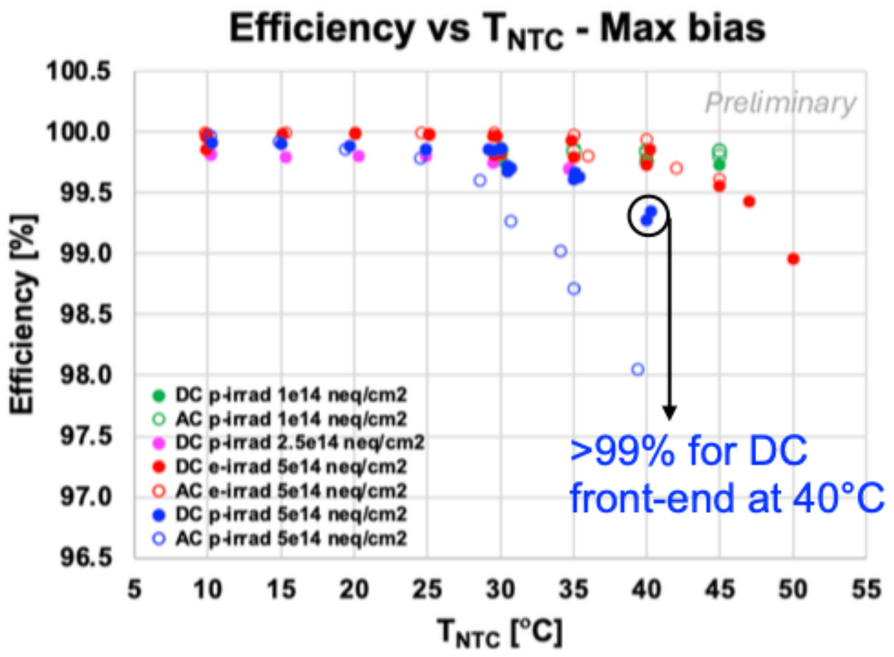
At ARTBL

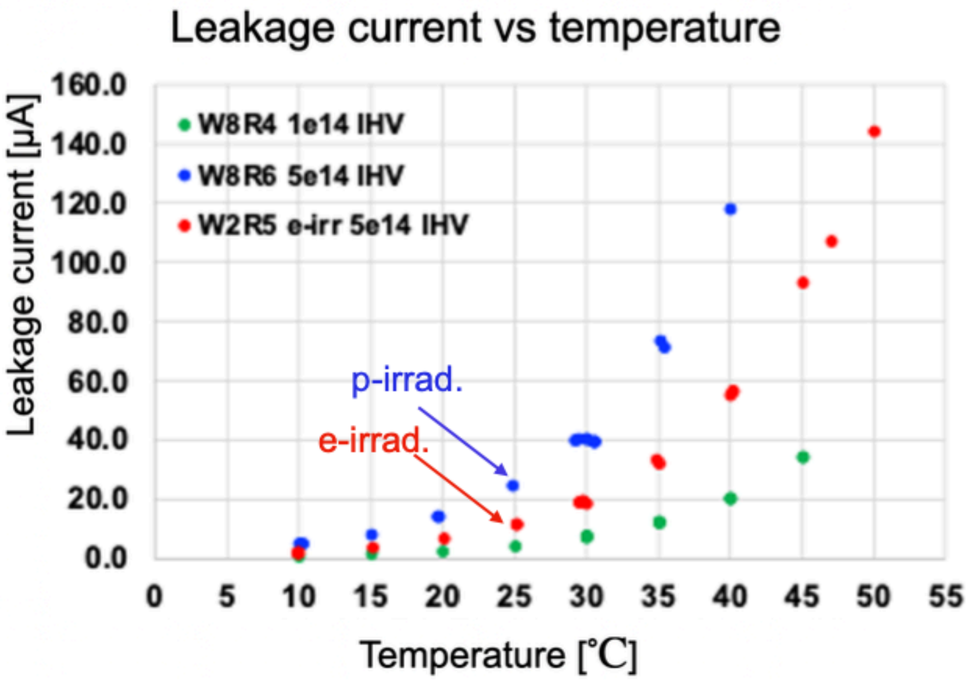




More details of telescope will be shown by Jerome Baudot (D_RD_39)

TJ-Monopix2 beam test at KEK PF-AR test beam line



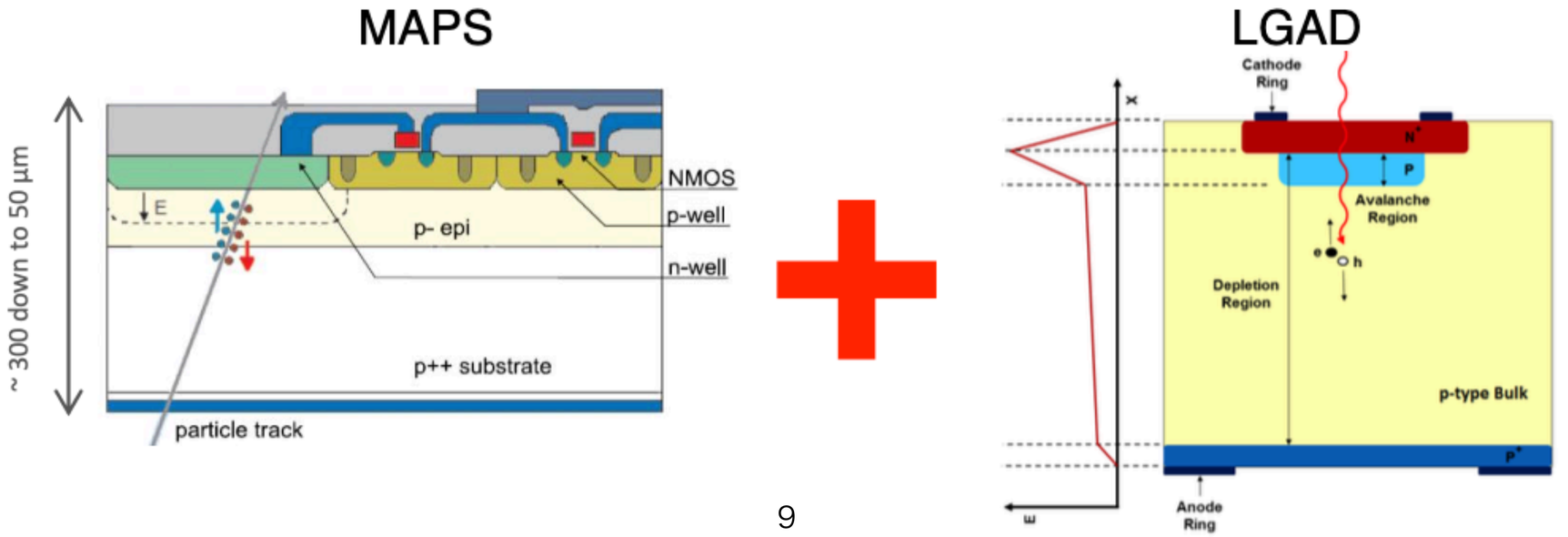


- Detection efficiency degradation is observed with larger irradiation. However, the efficiency can still reach >99% in DC front-end up to NTC temperature of 40 °C.
- Comparison between e-irrad. and p-irrad. sample shows more bulk damage in proton-irradiation, crosschecked by leakage current measurement.

Presented at HSTD14
by Shijie WANG
(PhD. Student of Tokyo University.)

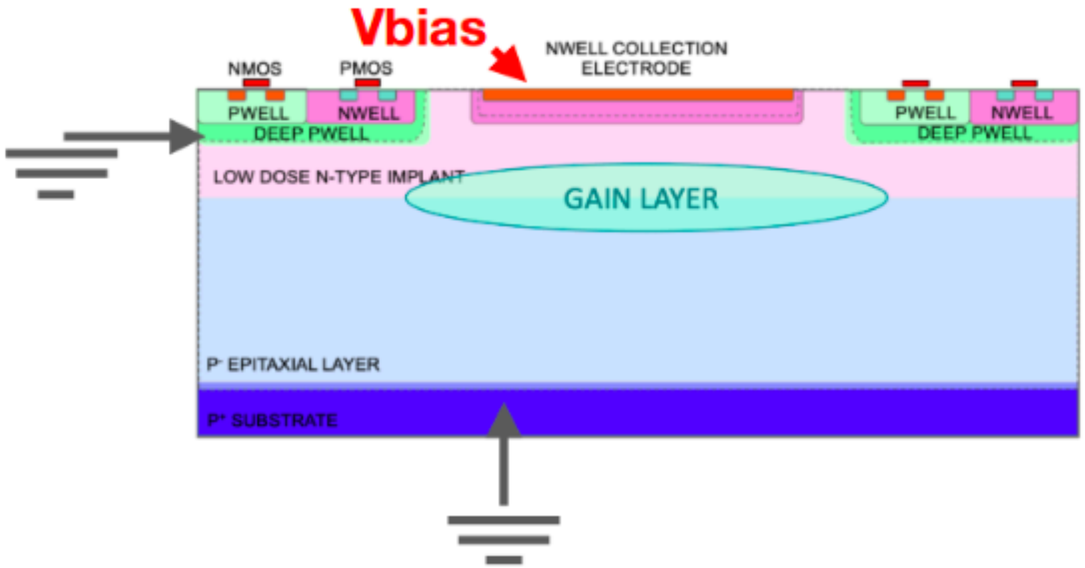
MAPS with an amplification layer

- Internal gain in sensor is very beneficial
  - Fast timing : achieve < 30 ps with low gain (~x10) : developed as APD, LGAD.
  - Low power consumption : lower (or can be no ?) amplification in ASIC side.
- Combining MAPS with LGAD
  - CMOS Active SenSor with Internal Amplification (CASSIA) project
    - Recognized as one of ECFA DRD3 projects.

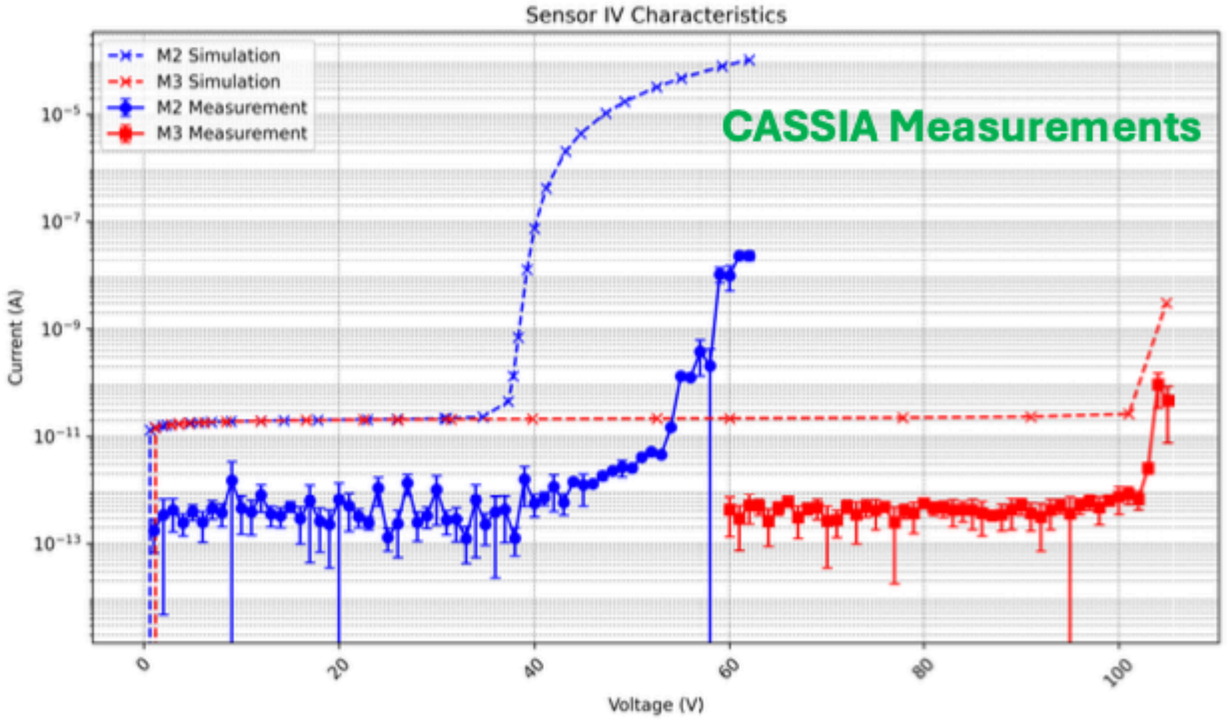


TCAD simulation

- **Prototypes from CERN – 2024 (DRD3 CASSIA Project)**
  - Large pitch ~ 80 µm



Generic doping profiles



- Comparison between TCAD simulations and CERN laser data
- **Testing and discussion were conducted in Strasbourg by Hasan Shamas and Yuta Okazaki**

Presented at HSTD14
by Hasan Shams
((PhD. Student of IPHC)

Impact Amplification with CMOS pixel Sensor (APICS) prototype

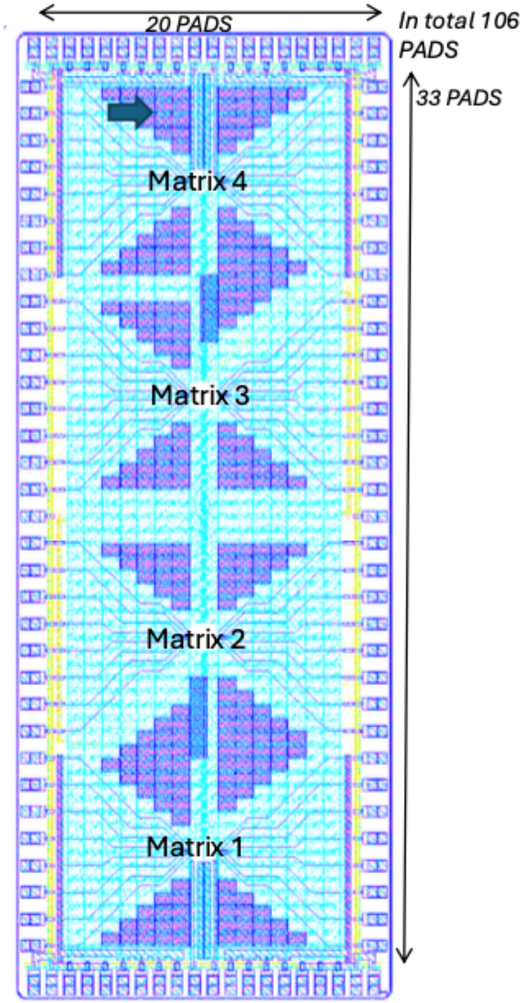
1st chip

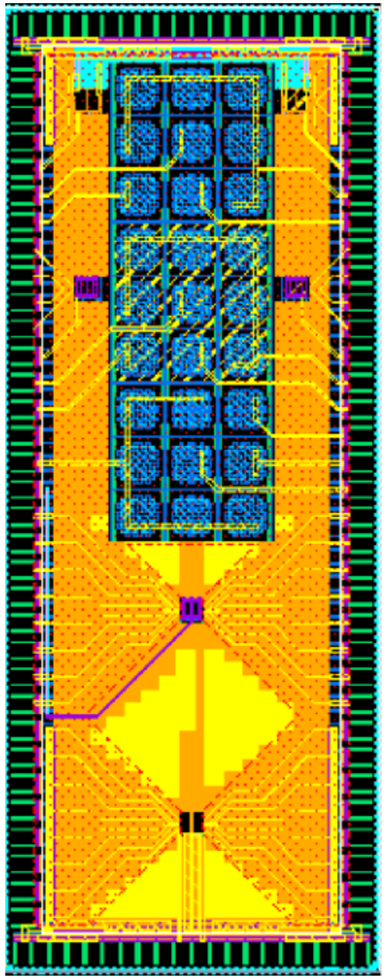
Chip size : 5.5 mm × 2 mm (TowerJazz 180 nm)

- 4 matrixes of 8x8 pixels of 15 um x 15 um
- Only internal part of matrix (4x4) read-put

1st chip - Matrixes:

Matrix	Collection electrode	Gain layer	Circuit
1	Nwell, r=4um	GL1	AC+BUF
2	Nwell, r=4um	GL1	DC
3	Nwell, r=2.2um	GL3	DC
4	Nwell, r=2.2um	GL3	AC+BUF





2nd chip

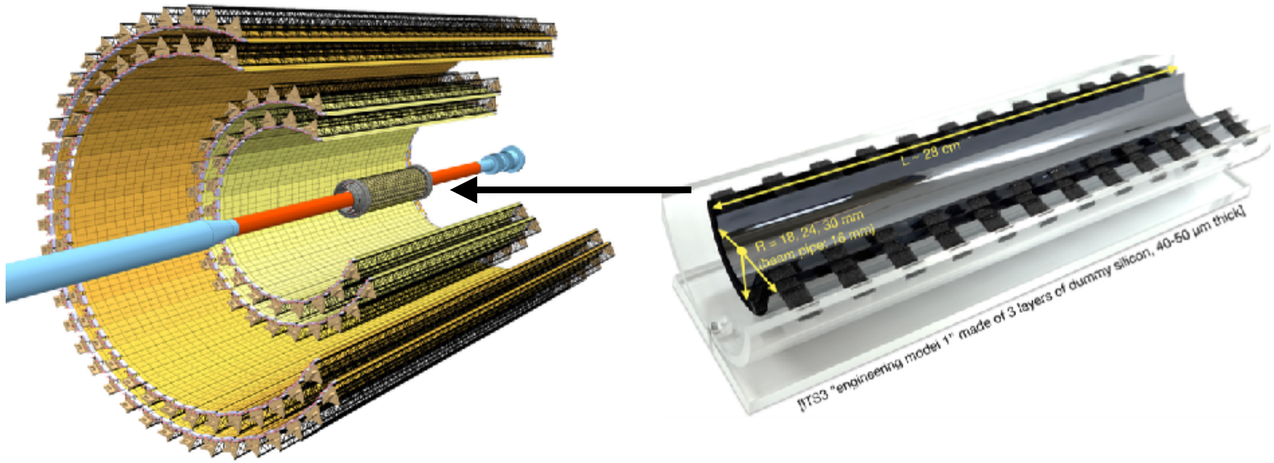
Simple diode (for measurements of characteristics)
- 300 μm × 300 μm pixel size
- 3 × 3 matrix
- Different p-layer pattern
- Different structure (STD, BLK)

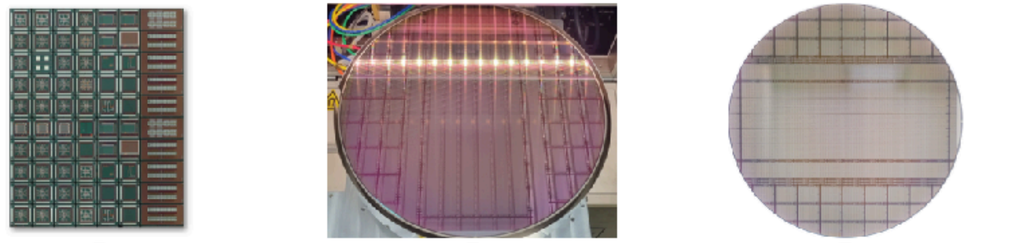
MAPS with an amplification layer
- 15 μm × 15 μm pixel size
- 8 × 8 matrix
- Different p-layer pattern
- Different structure (STD, BLK)

Presented at HSTD14 by Hasan Shams ((PhD. Student of IPHC)

Submitted at January 23rd. Expected delivery date is the end of June.

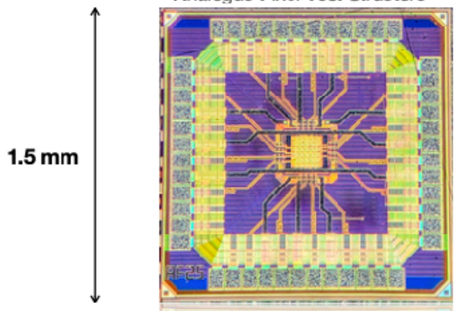
MAPS for ALICE





First submission of TPSCo 65nm (ITS3 with CERN EP R&D)

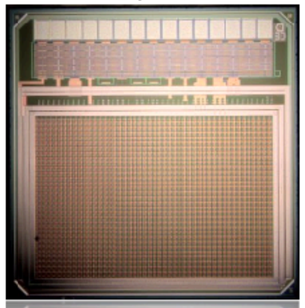
APTS
Analogue Pixel Test Structure



- 6x6 (4x4 readout) matrix, pitch: 10-25 µm
- 3 process variants
  - Standard/modified/modified with gap
- 2 types output buffer
  - Source follower (SF)
  - OpAmp: very fast, driving 50 Ohm

NIM.A 1069 (2024) 169896
NIM.A 1070 (2025) 170034

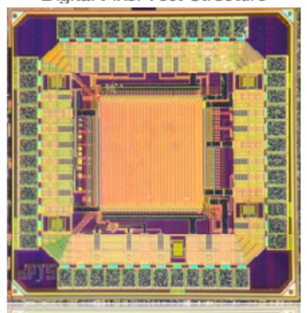
CE65
Circuit Exploratoire 65nm



- 64x32/48x32 matrix, pitch: 15-25 µm
- Rolling shutter readout
  (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower

JINST 20 (2025) 03, C03033

DPTS
Digital Pixel Test Structure



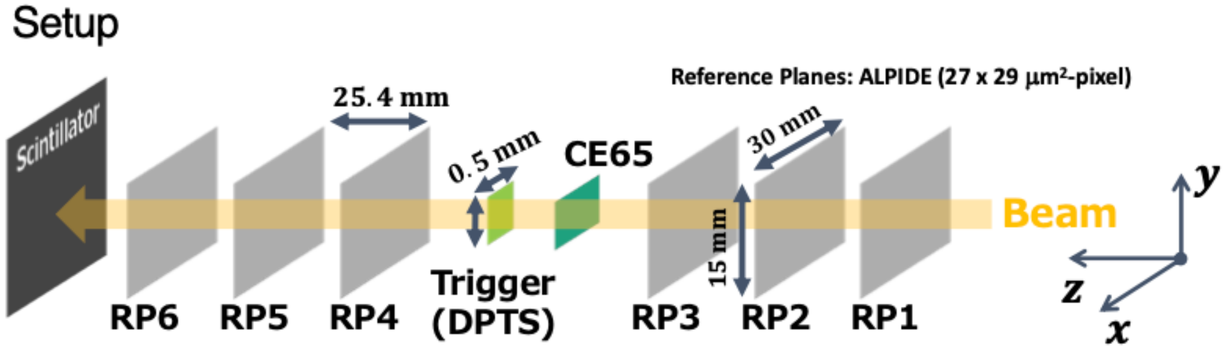
- 32x32 matrix, pitch: 15 µm
- Asynchronous digital readout
- Time-over-Threshold (ToT) information

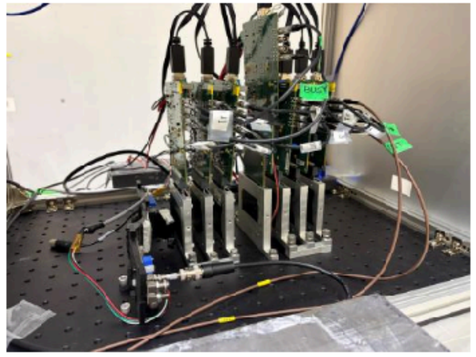
NIM.A 1056 (2023) 168589

- MAPS sensor development for ALICE Inner Tracking System Upgrade (ITS3)
  - First MAPS of TPSCo 65 nm process. (CERN EP R&D)
- The CE65 was designed under the leadership of IPHC.
- Asynchronous readout (SPARC) in ER2 is also lead by IPHC
- ER3 submission is planned at Q4-2026.

Evaluation for ALICE chips

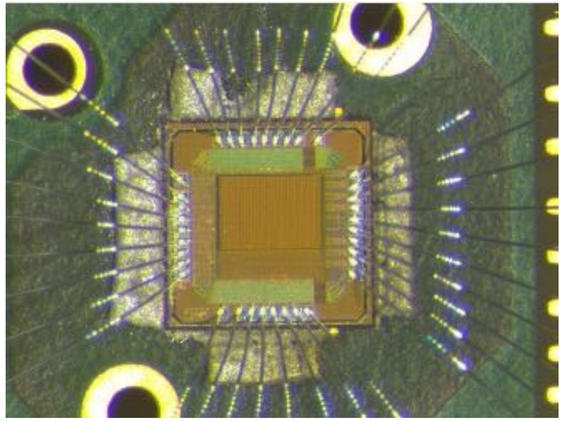
4th Beam Test in Dec. 2025





- SPARC test have started since 3 weeks
  - Produced in ER2
  - Power, control, test-injection OK
  - **Visit of Kai Teramoto @ IPHC in May for deeper tests**

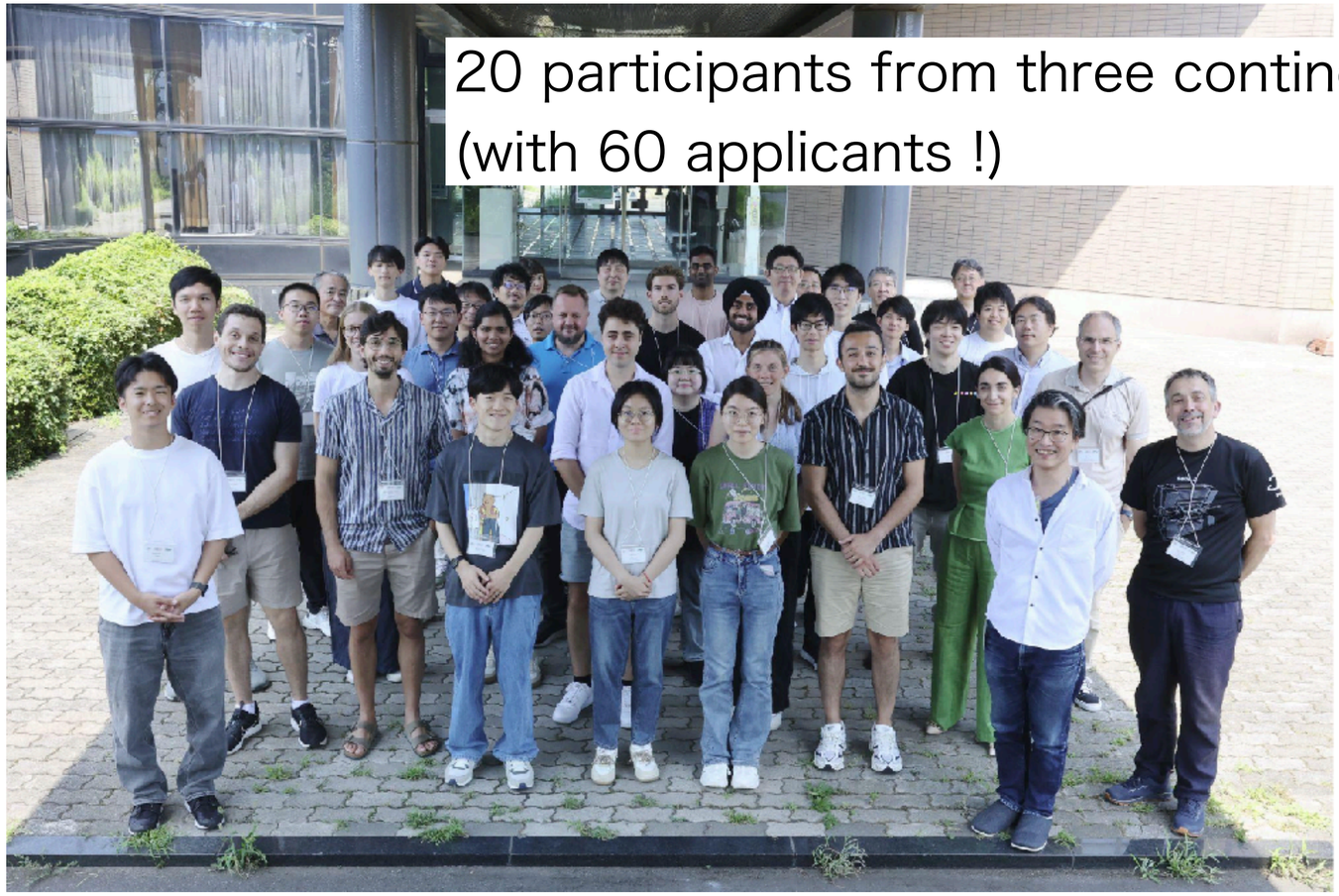
- Test beam is planned at KEK during winter 2026-27



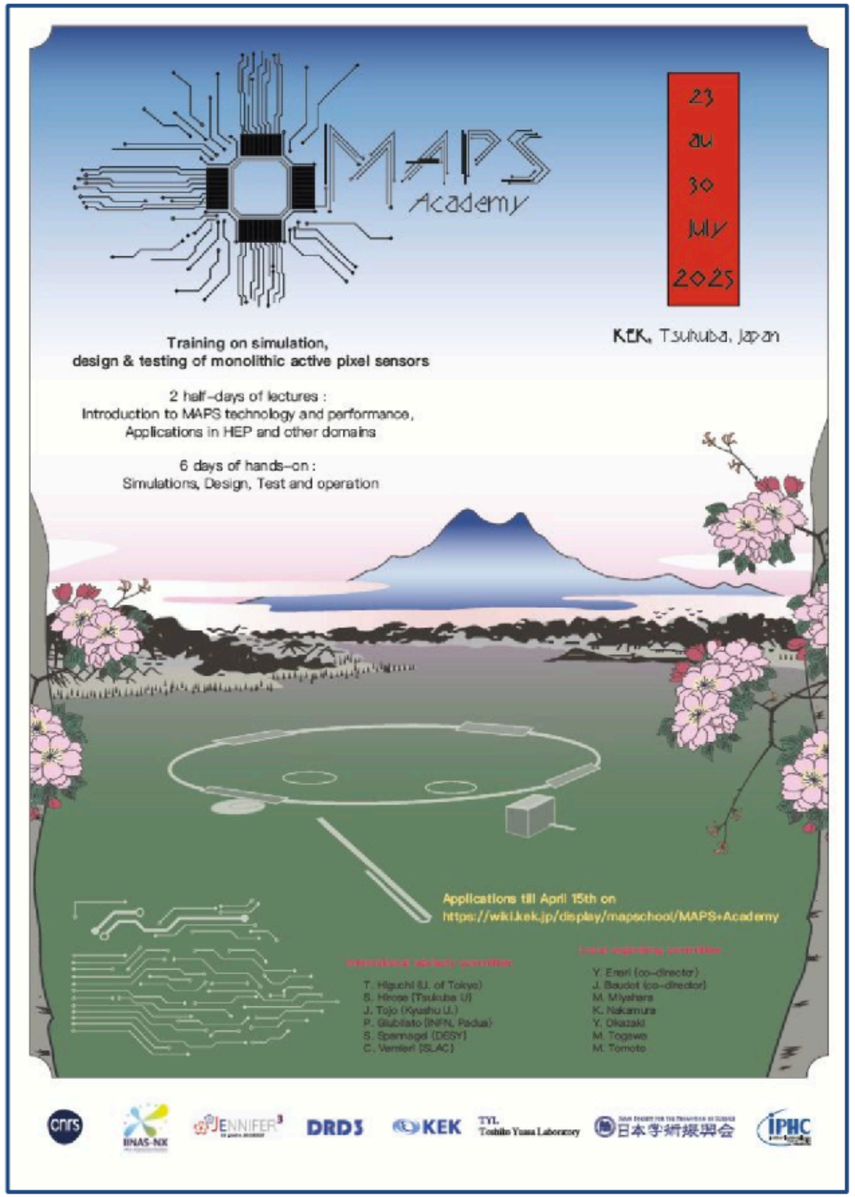
More details of ALICE chips will be shown by Yorito Yamaguchi (D_RD_38)

MAPS academy

- Development and human resource beyond experimental projects
- Acceleration of international joint development
- The inaugural academy was placed at KEK

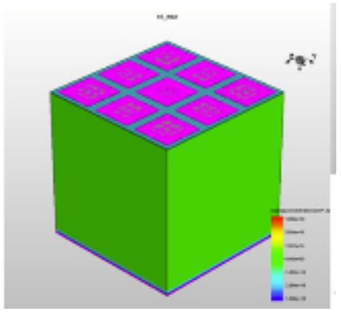


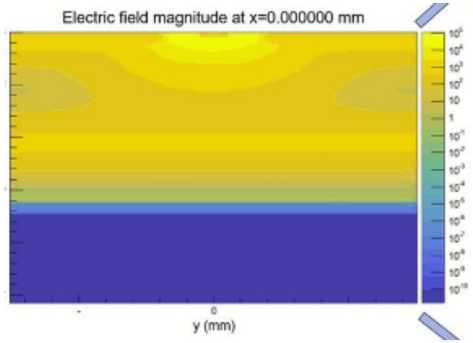
20 participants from three continents.
(with 60 applicants !)

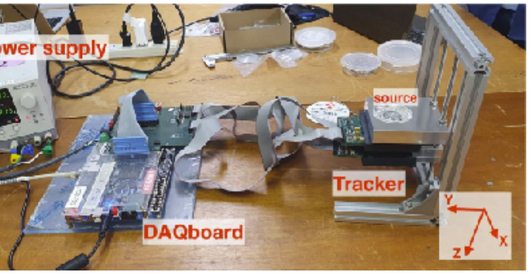


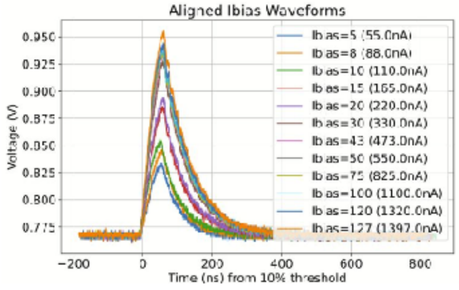
https://wiki.kek.jp/spaces/mapschool/pages/393249796/MAPS+Academy

Contents









Hands on A

SYNOPSYS®

Sensor design

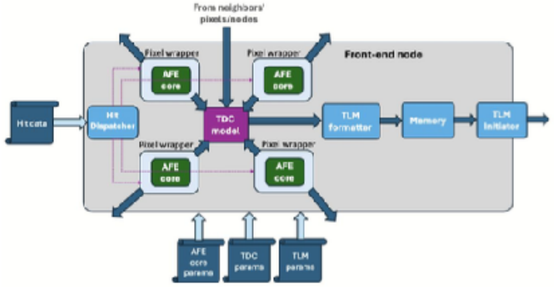
ap²

Charge deposition
+ collection
(+ digitization)

Hands on B

Pix ESL

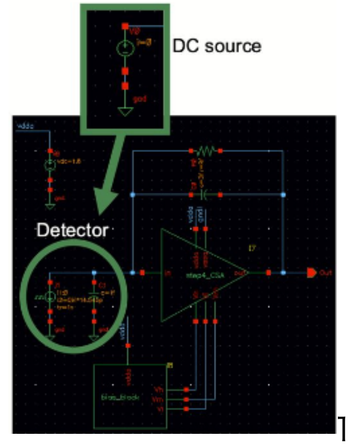
Frontend architecture
+ Readout architecture



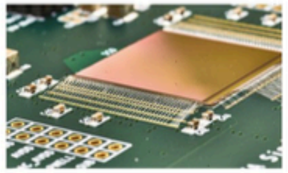
Hands on C

cadence®

Chip design



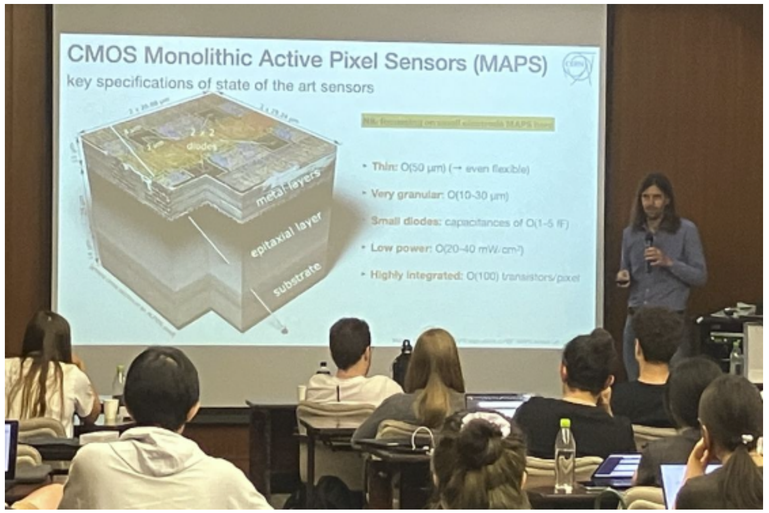
Hands on D

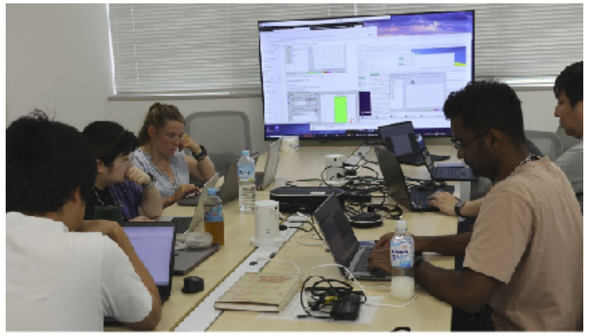


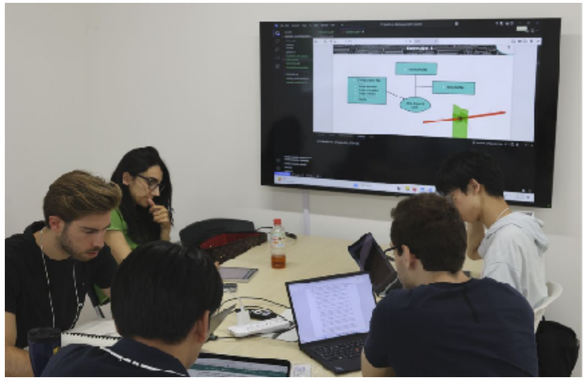
Operation

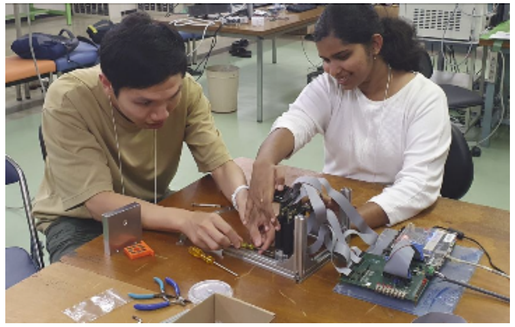
10 pairs from 20 participants
Assignments pairs to each
hands-on and place

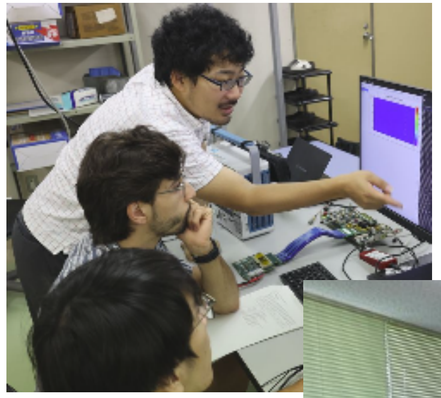
How things went....

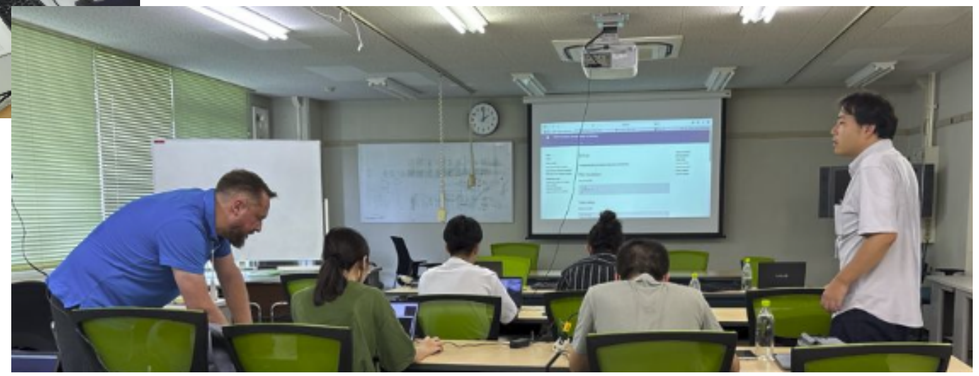












Reported at DRD3 week (Link)

Organizing Staffs

A lot of contributions from BASHI members !!

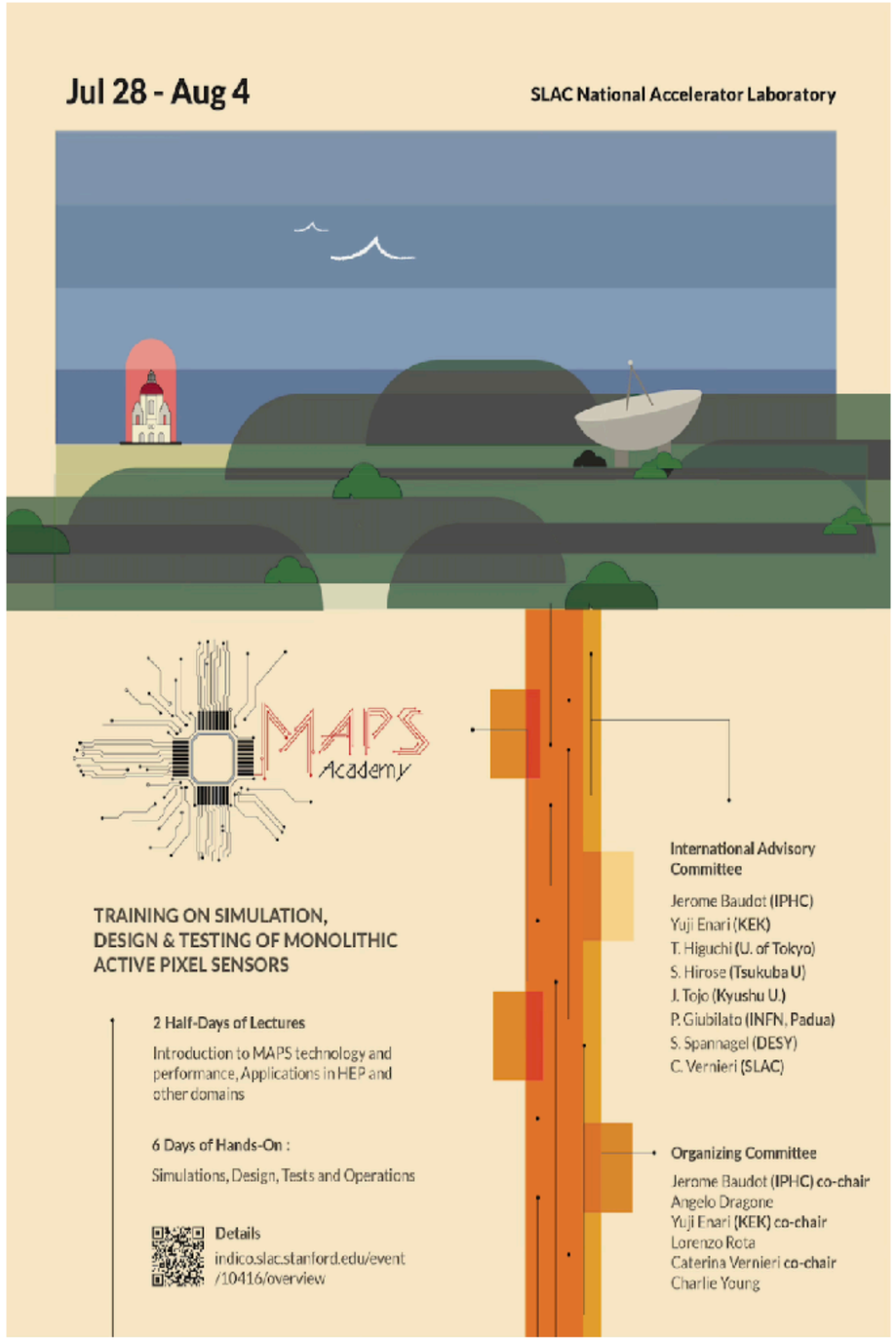
- Directors : **Y. Enari (KEK), J. Baudot (IPHC)**
- LOC (KEK) : **K. Nakamura, Y. Okazaki, M. Togawa, M. Tomoto**, M. Miyahara

- Lectures :
  - **J.Baudoti (IPHC)**, M. Mager (CERN), I. Peric (Karlsruhe)
- Hands-on :
  - **K. Nakamura (KEK)**, E. Sacchetti (IPHC), **F. Morel (IPHC)**, M. Miyahara (KEK), J. Dhaliwal (CERN), **Y. Enari (KEK), M. Togawa (KEK), Y. Okazaki (KEK)**

- International Advisory Committee :
  - Japan: T. Higuchi, S. Hirose, J. Tojo
  - Europe: P. Giubilato, S. Spannagel
  - US: C. Vernieri

Coming MAPS academy

- MAPS academy was such a success that we are making it recurrent.
- Next academy will place at SLAC, July 28 -Aug. 4 2026
  - https://indico.slac.stanford.edu/event/10416/
- We may think next one in Europe (possibly in Strasbourg).



Conclusion

- The BASHI project has successfully served as a bridge between the French and Japanese teams developing MAPS.
  - We have completed the joint design of the OBELIX-1 for Bell II and the APICS implementing gain layer and their submission.
  - We have already completed the initial discovery of the TPSCo 65 nm technology (with the CE65 prototypes), and opened the path for French-Japanese collaboration on ALICE dedicated sensors (D_RD_38).
- We have established “MAPS Academy” a new school for nurturing young talent and leading to joint research that transcends the boundaries between France and Japan.
- The BASHI Project in 2026 is 4th (last) year, we will focus on testings for coming chips.
  - It is time to start thinking about new projects.