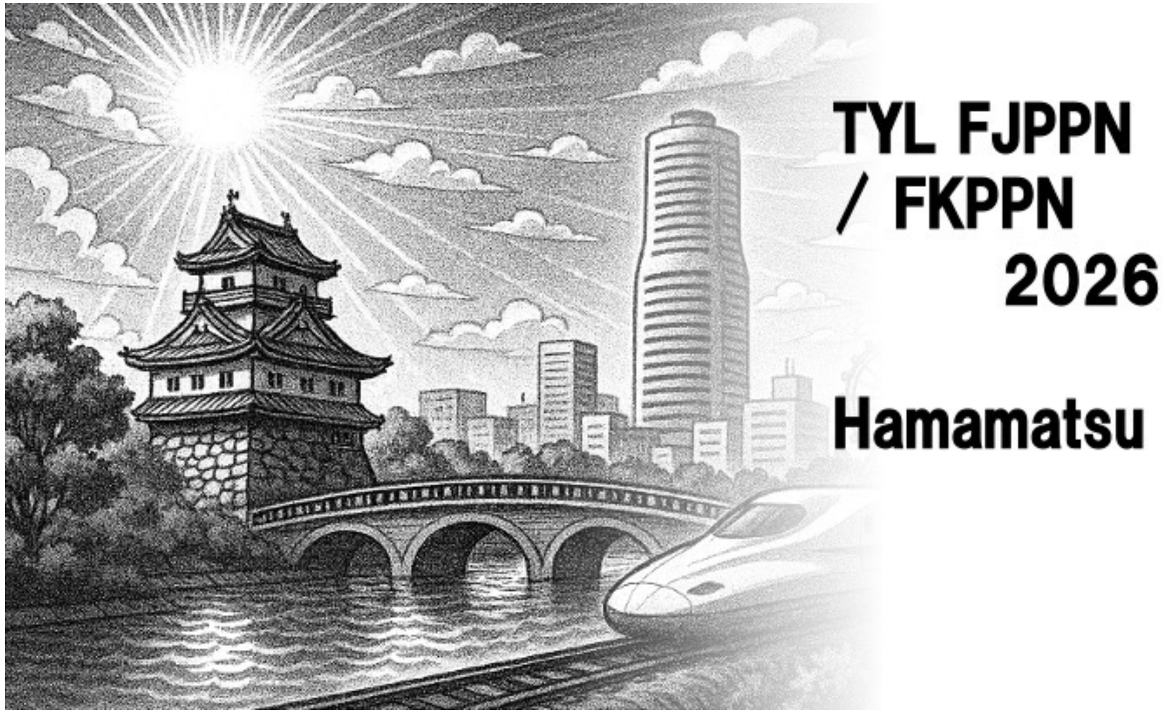
Commissioning and further development of cryogenic readout electronics for LAr-TPC applications

《D_RD_36 》(since 2025)



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国立大学法人
岩手大学
IWATE UNIVERSITY

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LES 2 INFINIS
LYON

Outline

- Detector tests and commisioning for DUNE/ProtoDUNE project
- ASIC developments (LTARS and Cryo-CMOS) for charge readout in cryogenic environment
- Summary

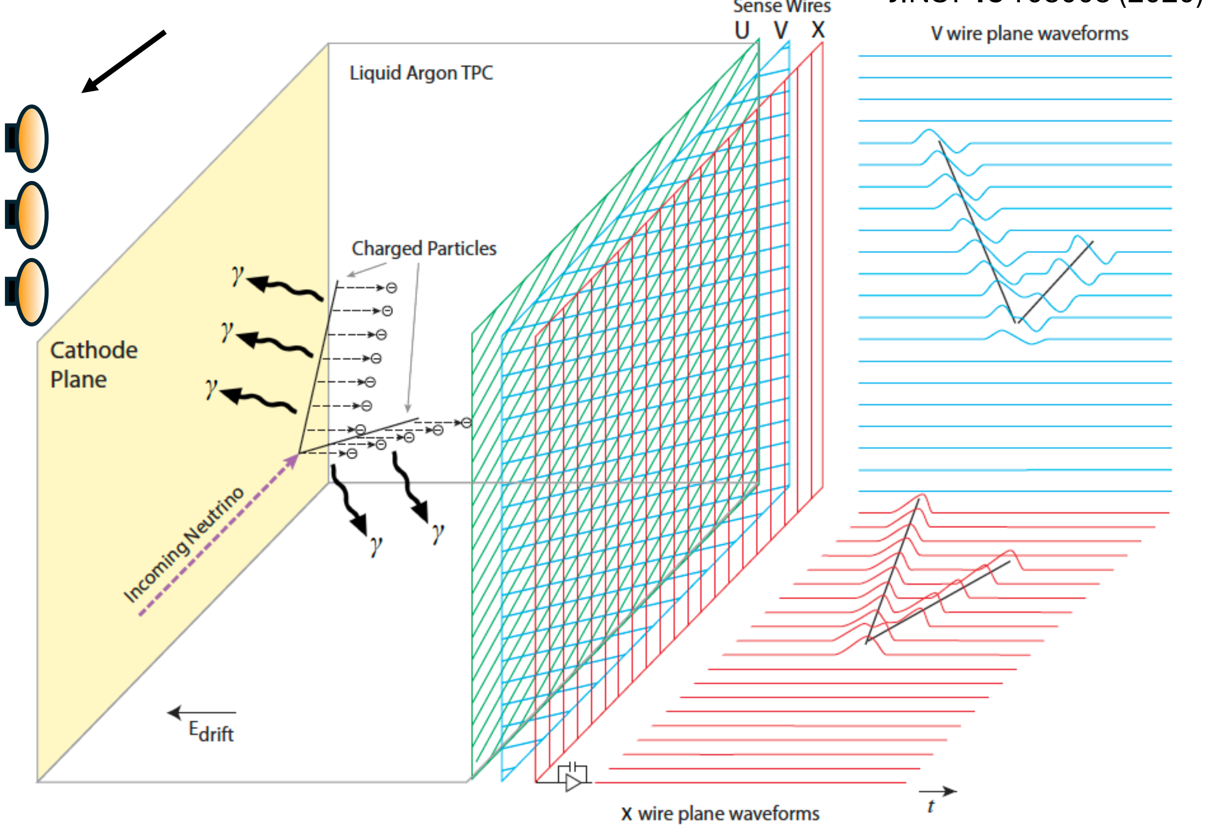
LAr-TPC for neutrino measurements

- High-res (~ a few mm) 3 dimentional imasing of tracks
- Excellent capabilities on energy loss measuement and PID
- Liquid Ar (LAr) is relatively cheap (good for large-scale detector)

- The frontend equipments, such as frontend readout electronics, are exposed to cryogenic environment
  - Boiling point of LAr: ~87.3 K

Light(γ) detectors which will provide the t_0 of the interaction

JINST **15** T08008 (2020)

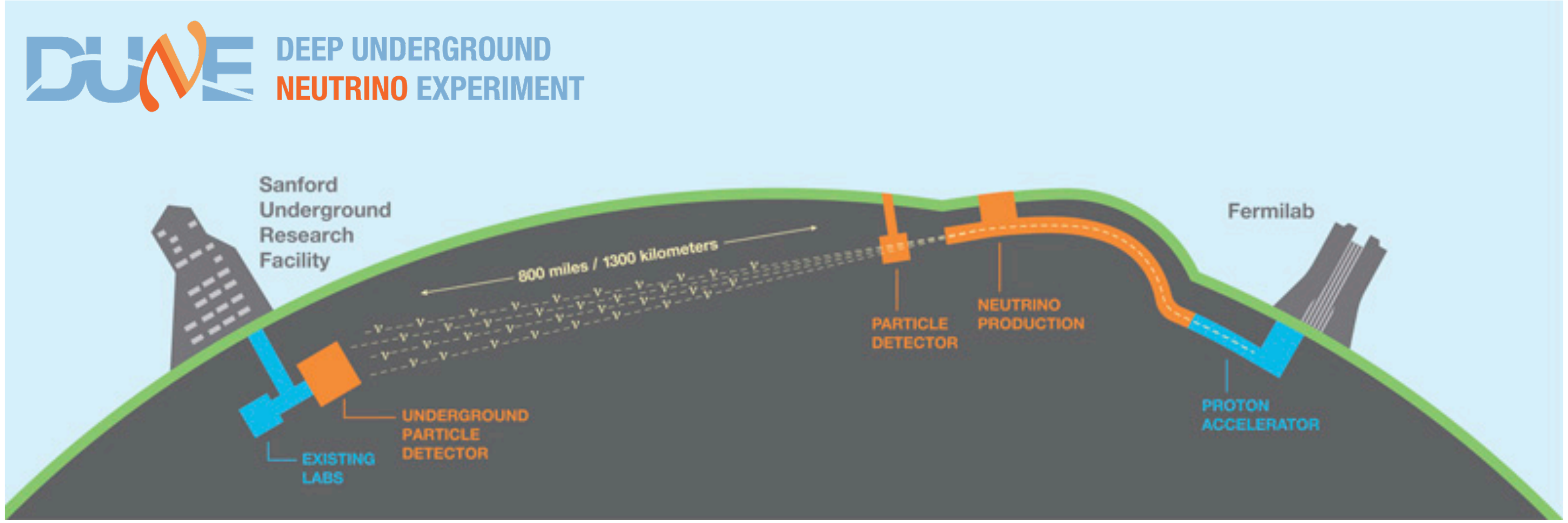


General operating principle of LAr-TPC

➡ <u>Stable operation of readout electronics in cryogenic environments is critical</u>

The Deep Underground Neutrino Experiment (DUNE)

- A next-generation long-baseline neutrino oscillation experiment using the Fermilab accelerator facility and the SURF in USA
- Main physics goals:
  - Measurement of the neutrino mass hierarchy, the amount of CP violation in the leptonic sector
  - Detection of low energy neutrinos such as neutrinos from supernova bursts or the Sun
  - search for nucleon decay and other beyond the standard model phenomena
- Planning to construct ~40 kt scale LAr-TPC for the far detector
- Aiming to start the experiments at around the ~~end of FY2029~~



JINST **15** T08008 (2020)

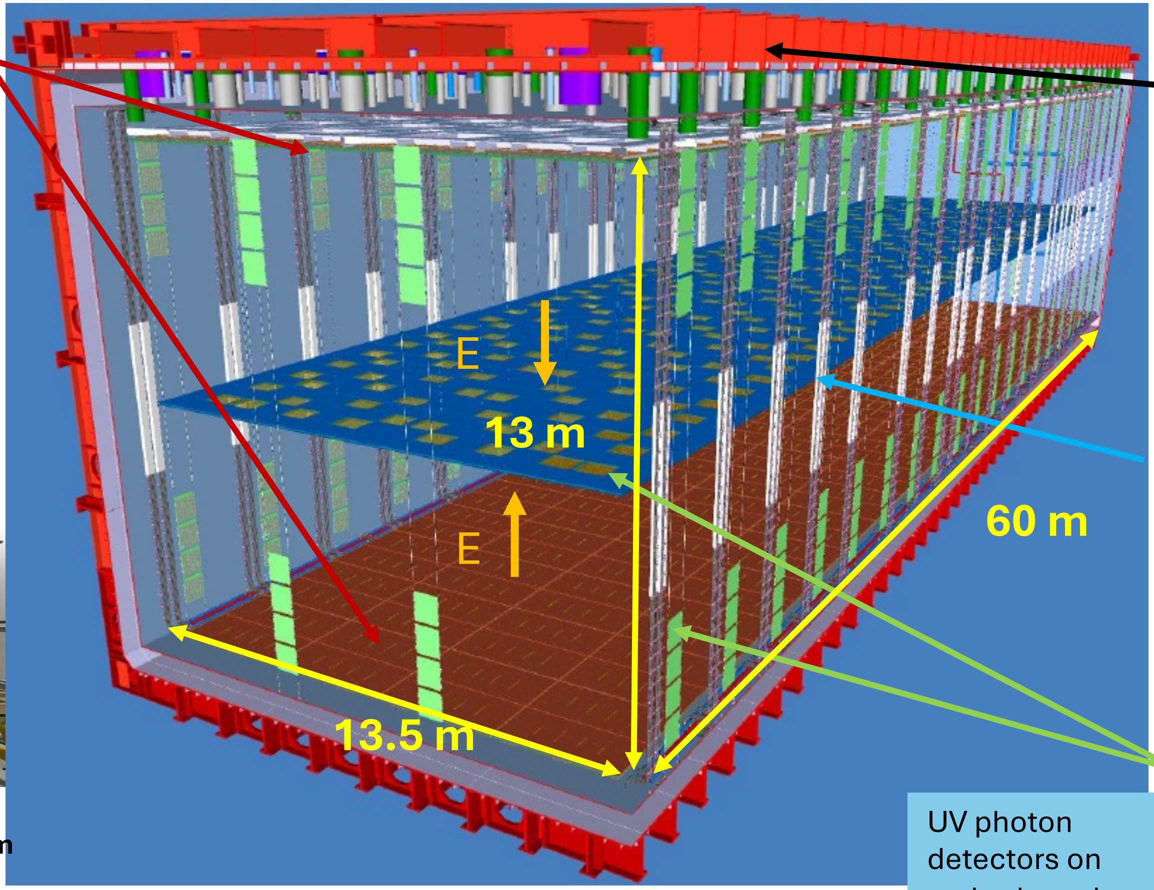
1st DUNE Far Detector Module: Vertical-Drift (**FD-VD**) :

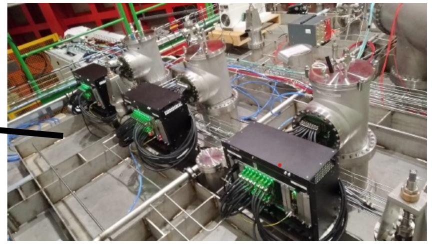
15 kt of active LAr volume

Japanese groups historically involved in the Top-Drift Electronics (TDE) Consortium in collaboration with IN2P3 groups

Top and bottom anode charge readout surfaces:

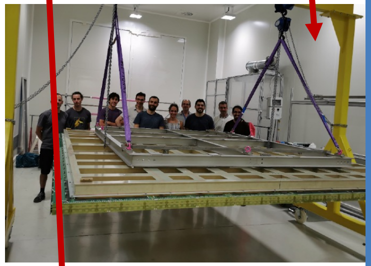
Made of 80+80 Charge Readout Plane (CRP) units 3x3.375 m^2
Each unit: 2 stacked layers of segmented perforated PCBs

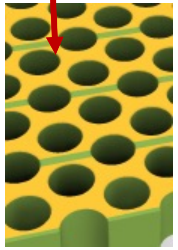




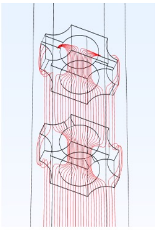
Cryostat roof with TDE Chimneys containing analog cryogenic FEB and µTCA digitization readout

Cathode surface at -300 kV
→ E~500V/cm





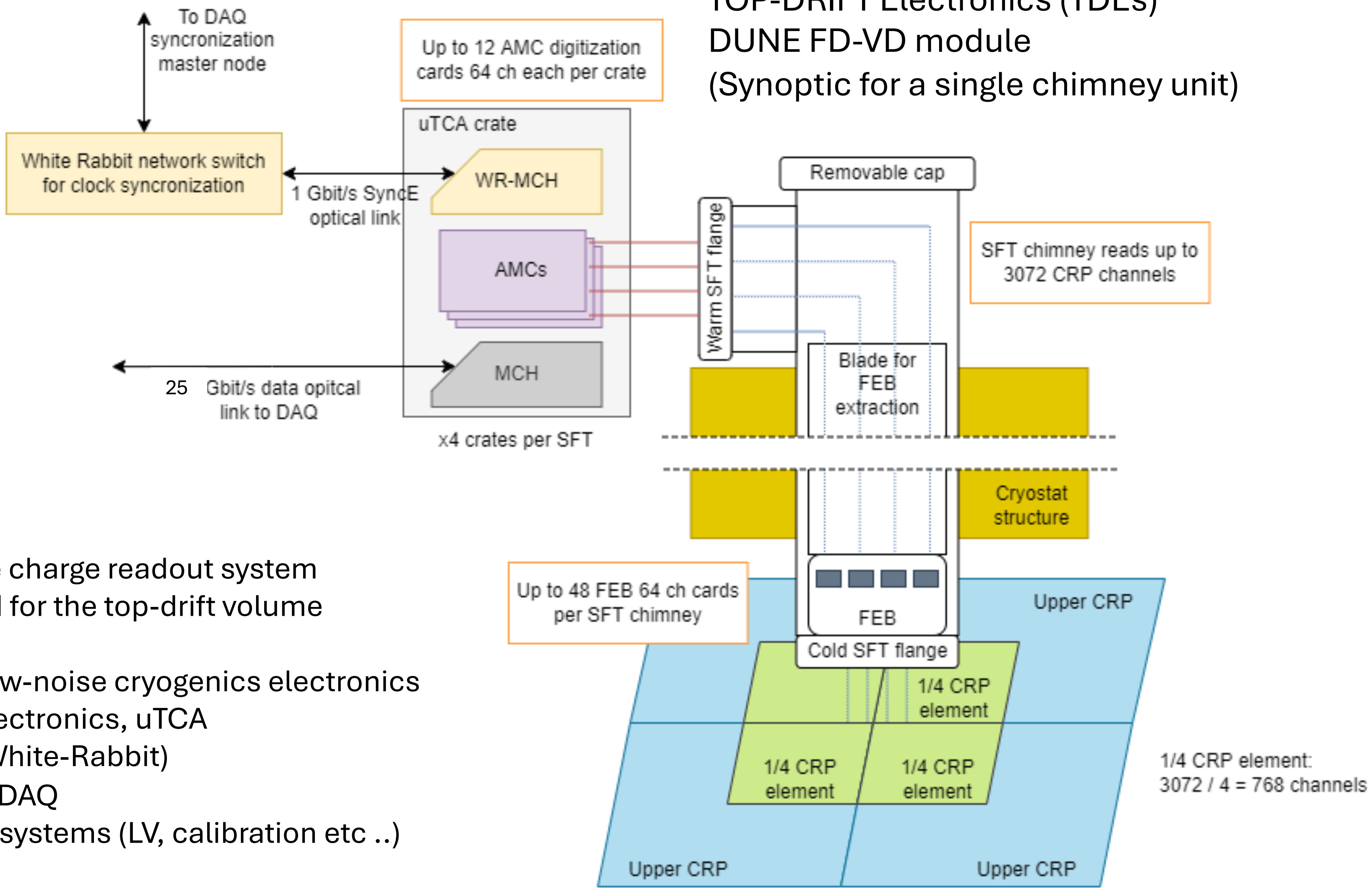
Strips 5 mm
Holes 2.4 mm



1/40 Prototype in CERN cryostat

UV photon detectors on cathode and cryostat walls

TOP-DRIFT Electronics (TDEs)
DUNE FD-VD module
(Synoptic for a single chimney unit)



→ Complete charge readout system optimized for the top-drift volume

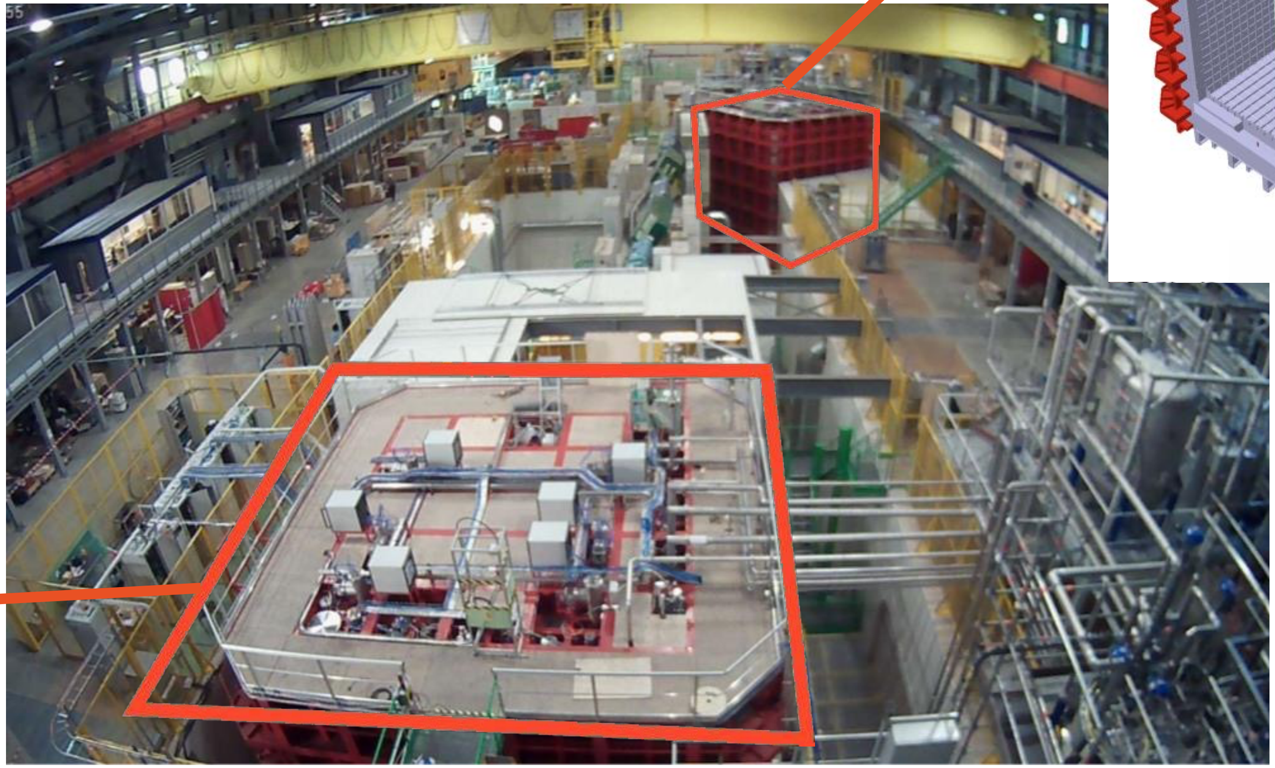
- Analog low-noise cryogenics electronics
- Digital electronics, uTCA
- Timing (White-Rabbit)
- Ethernet DAQ
- Ancillary systems (LV, calibration etc ..)

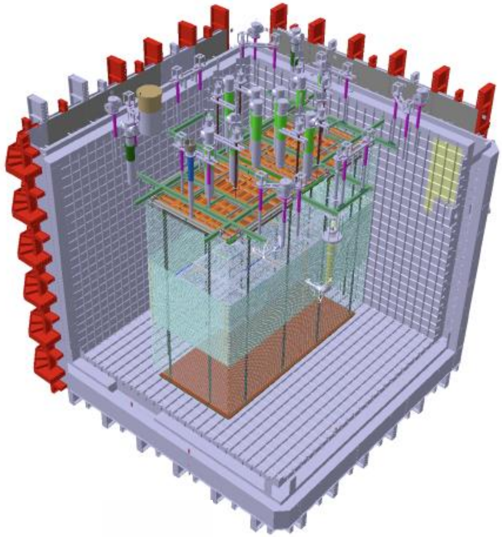
The DUNE prototype experiment (ProtoDUNE)

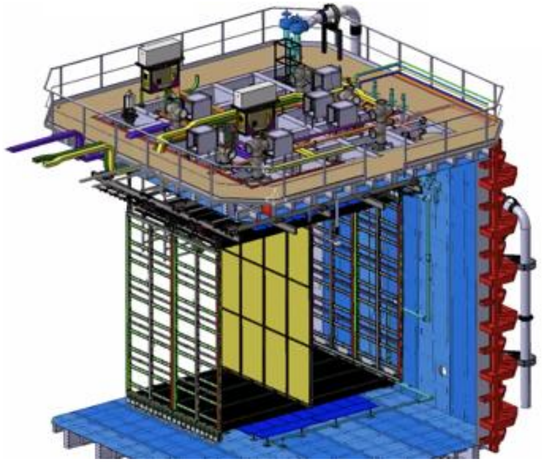
- Prototypes of the DUNE detectors are constracted and tested at the CERN neutrino platform
- Part of full size detectors (1 module)
  - Active volume: ~1 kt

NP02
VD

Figure: CERN Neutrino Platform.







NP04
HD
(Horizontal-Drift)

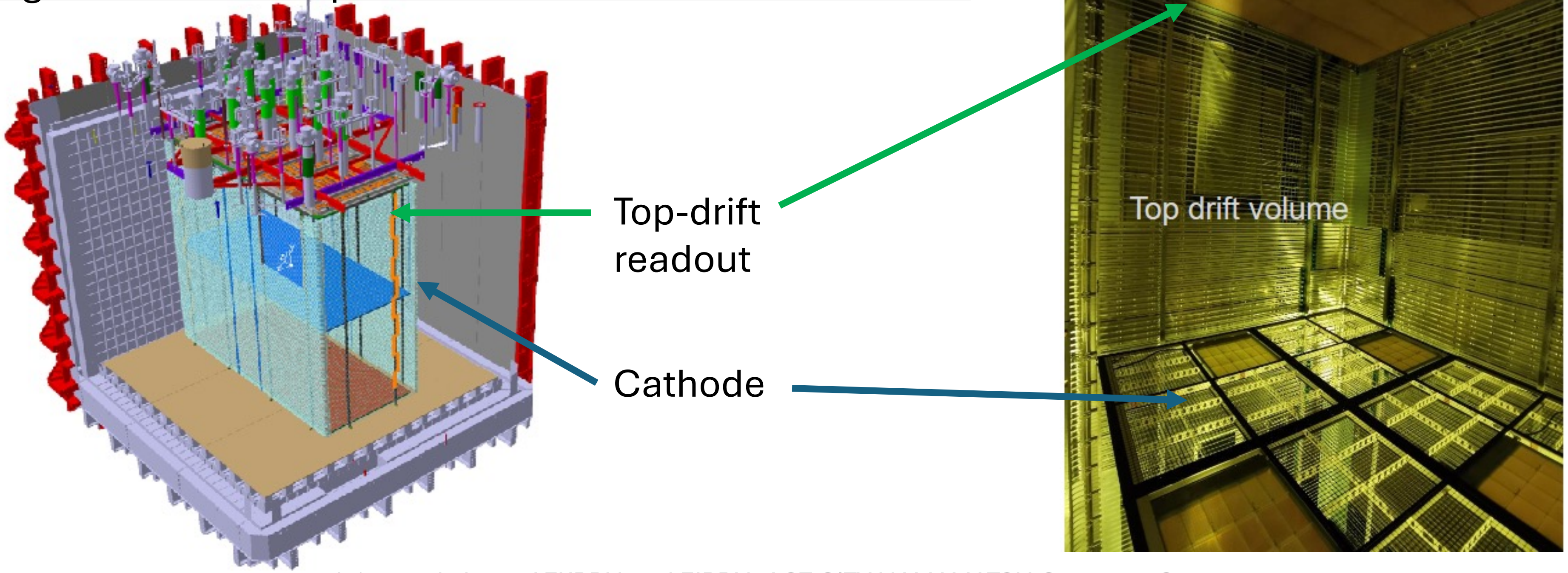
Module-0 VD assembly test in NP02

- Two final top-drift CRPs (CRP2 and CRP3) + TDE readout testing completed by October 2022 in Cold-Box

- 6144 readout channels (96 FEB boards and 96 AMC boards)
- Use of existing NP02 10 FEB chimneys → 10 uTCA crates with 10 AMC each
- Very high bandwidth readout system 400 Gbit/s network infrastructure

- Module-0 integration successfully completed in June 2023

- Detector filled with LAr at the end of 2024 and operational
- Detector exploitation with beam was conducted in summer 2025
- <u>Testing of the signal readout components are continued in the FY2026</u>



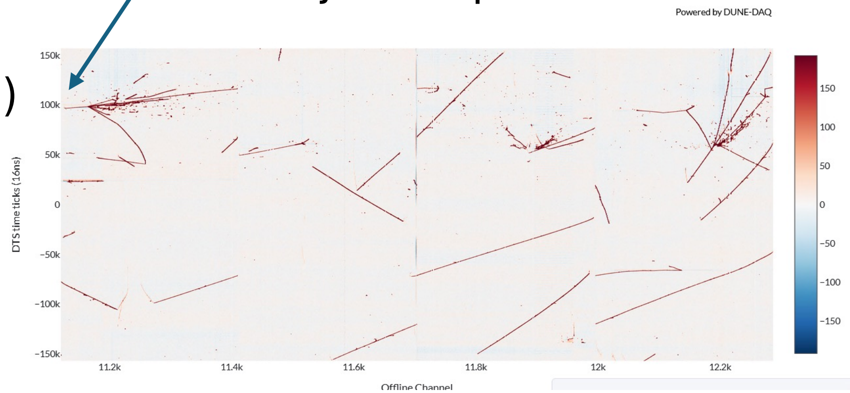
DUNE/ProtoDUNE activities in the FY2025

- ➢ Took part in the beam tests using the ProtoDUNE-VD detector
  - To TDE data taking

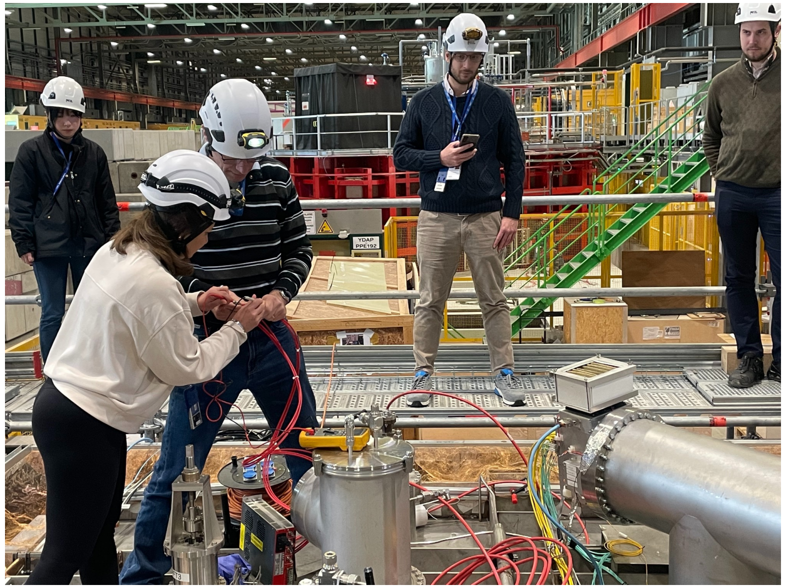
    D. Autiero (Lyon/IP2I), E. Pennacchio (Lyon/IP2I) and R. Hosokawa (Iwate U.)
- ➢ Investigation on noise problem on CRPs at the CERN Neutrino Plattoform
  - A. Morita (Iwate U.), R. Hosokawa (Iwate U.)
  - In collaboration with the DUNE colleagues:

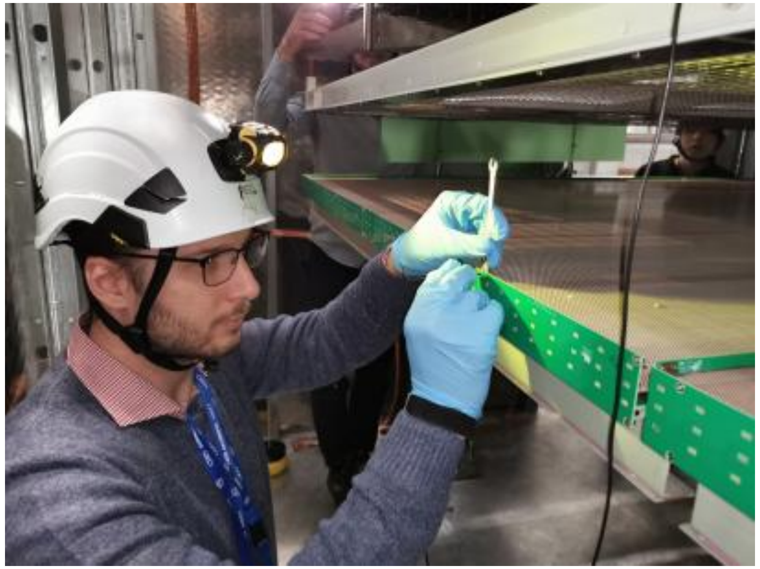
    D. Duchesneau (LAPP/IN2P3), F. Boran (Indiana U.), N. Gallice (BNL), T. D. Stokes (Yale U.)

Beam injection point



<u>Improvements to and installation of PCBs for noise-reduced signal transmission</u>





On-site tests will continue in the FY2026 and we'll perticipate in the activities

DUNE/ProtoDUNE activities in the FY2025

- Visit to Lyon/I2PI
  - A tour of TDE's Quality Control Facility
  - Discussion on the cryogenic electronics development that is led by Japanese group
    - D. Autiero (Lyon/IP2I), S. Galymov (Lyon/IP2I) , A. Morita (Iwate U.), and R. Hosokawa (Iwate U.)

    ✓ Visits (to CERN,Lyon) of A. Morita were supported by the TYL-FJPPN Early Stage Researcher Secondment program

Low Temperature Analog Readout System (LTARS)

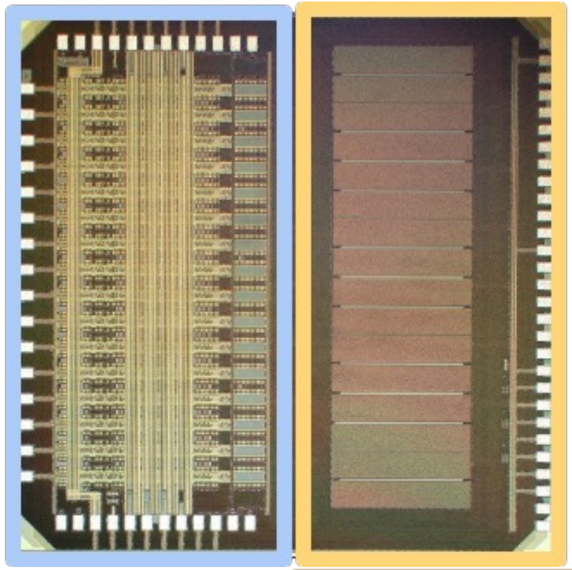
- A project of new signal readout cryo-ASIC is in progress
- The R&D has been led by Iwate-KEK group
  - The latest ASIC has amplifier and ADC on-a-chip

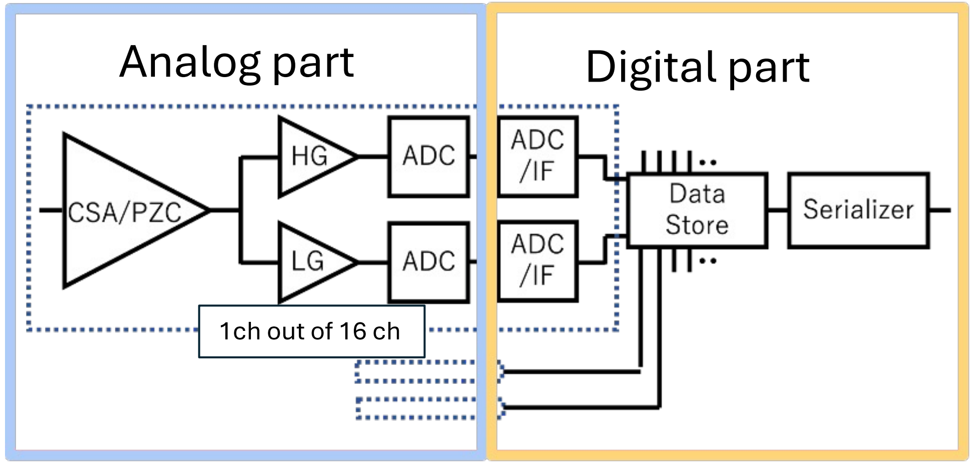
Current targeted design specifications

Parameter	High Gain (HG)	Low Gain (LG)
Peaking Time	1 us, 4us	
Conversion Gain	10 mV/fC	0.5 mV/fC
Dynamic Range	±80 fC	±1600 fC
ENC	<3000 e^-	<62500 e^-

Performance evaluation and debug/improvemnts will be conducted

The latest LTARS ASIC (LTARS16A)

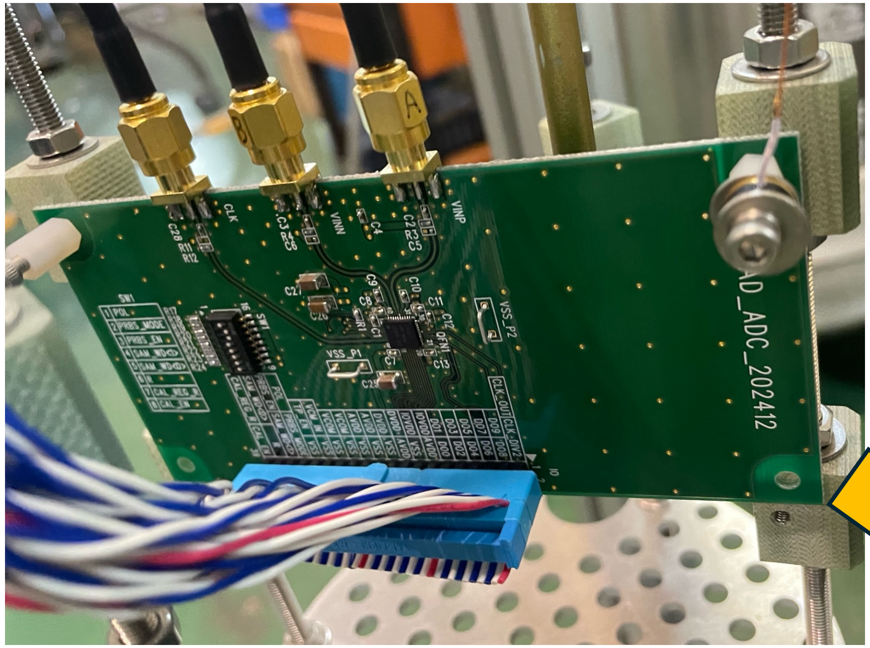


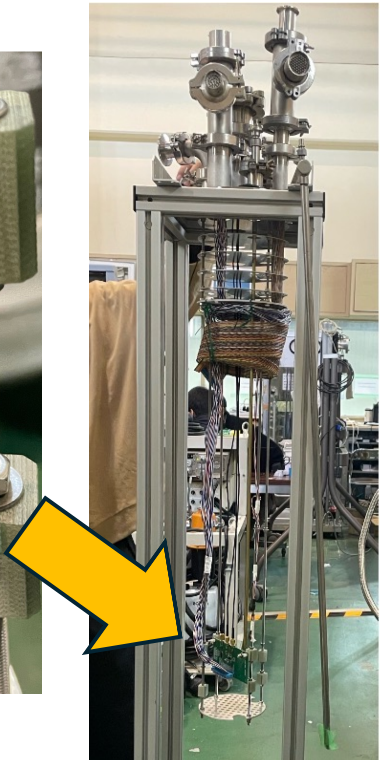


Further challenge to extremely low temperature environment - Cryogenic CMOS ASIC (Cryo-CMOS)

- Challenge of Developing Signal Readout Electronics for Extreme Cryogenic Environments (LHe temperature (~4 K) or even lower)
  - 22nm planer bulk CMOS process
- In the FY2025, Low-temperature operational tests were conducted on a radiation-hardened ADC (RAD-ADC) in order to evaluate the operational characteristics of CMOS in an extremely low temperature environment (~4 K).
  - Conducted by A. Morita (Iwate U.) *et al.*

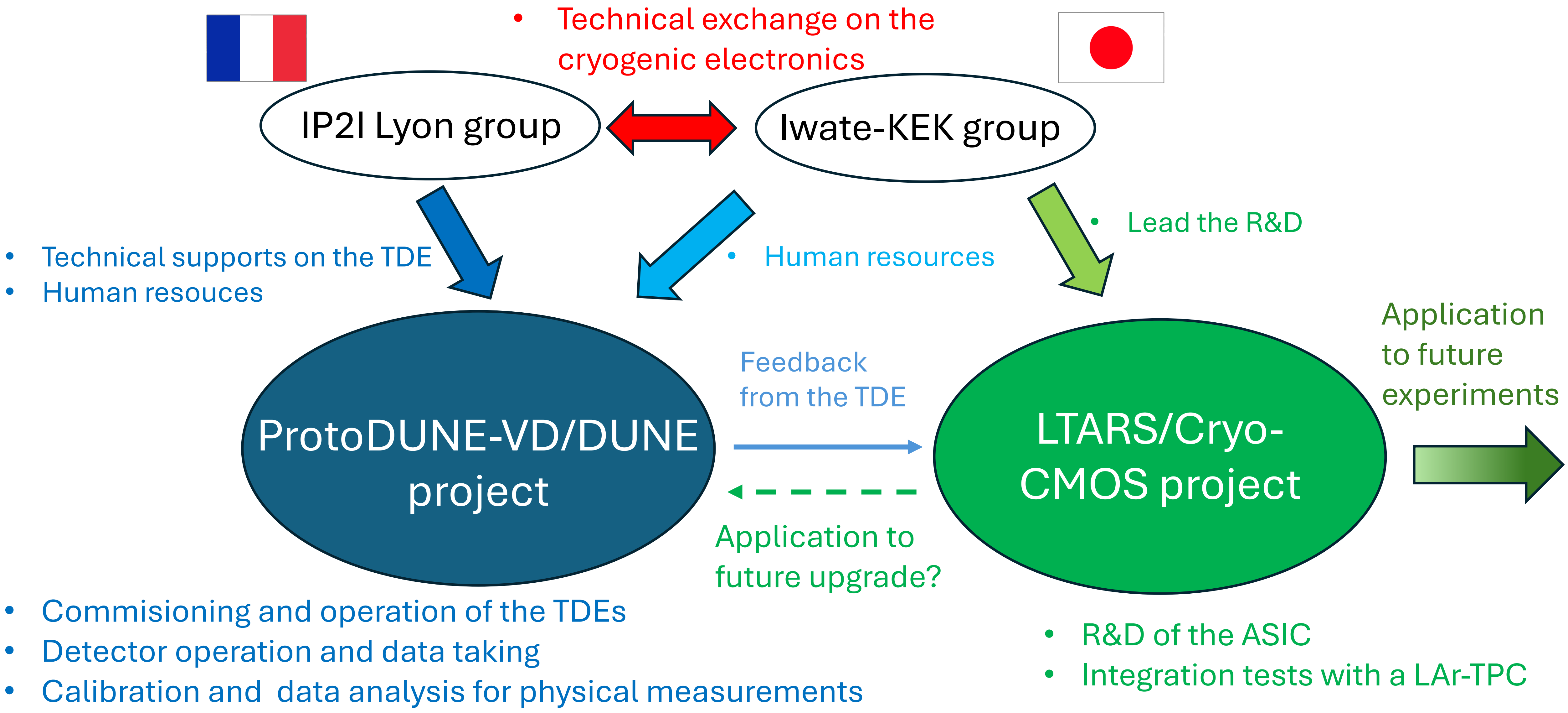
- 65 nm CMOS process
- 10-bit SAR (Successive Approximation Register) ADC
- Implementation of a comparator accuracy compensation circuit
- Integrated a compensation circuit for operating speed degradation due to increased transistor threshold voltage.





<u>We'll designe and fabricate a new readout ASIC using 22 nm CMOS process in the FY2026</u>

Overview of the project



proposal: “Commissioning and further development of cryogenic readout electronics for LAr-TPC applications”

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Affiliation: IP2I Lyon

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Funding Details

DESCRIPTION	UNIT_COST	NUM_UNITS	CURRENCY	REQUESTED_TO
Visit to France	20000.0	30	jpy	KEK
Travel	300000.0	2	jpy	KEK
Visit to Japan (stay)	200.0	7	eur	IN2P3
Visit to Japan (travel)	1500.0	1	eur	IN2P3

Additional Funding Details

REQUESTED_TO	TYPE	TOTAL_AMOUNT	CURRENCY
Iwate Univ.	Consumable	150000.0	jpy

SUMMARY

- Prototype testing of the LAr-TPC detector for the DUNE experiment (ProtoDUNE) and the fabrication of detector components are currently underway.
- Under the support of the TYL-FJPPN framework, we conducted prototype detector testing with beam at CERN, as well as testing of the signal detection components (CRPs) and readout circuits.
    - The detector testing work will continue to be carried out through FY2026.

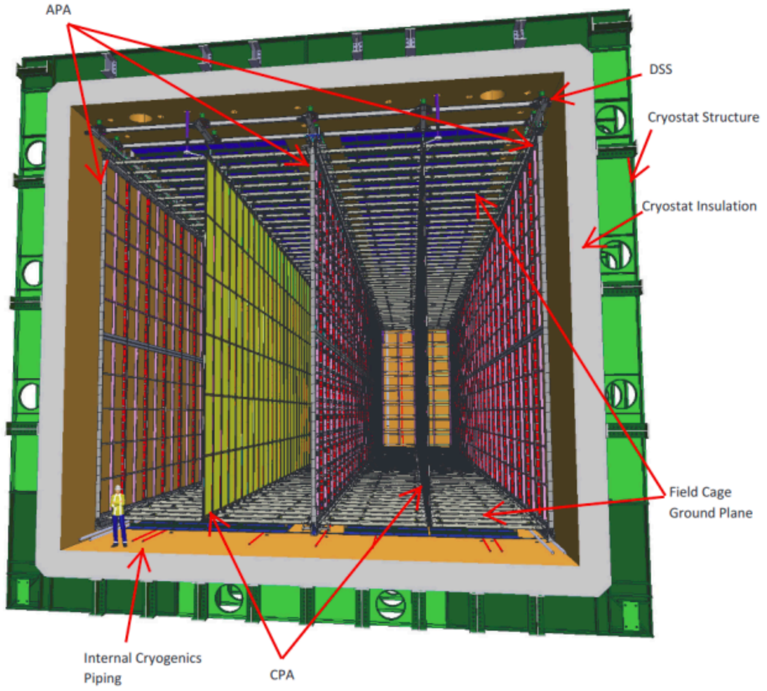
- Under the support of the TYL-FJPPN framework, we engaged in technical exchanges in the FY2025
- Advancement on the development of next-generation signal readout circuits for cryogenic environments will be conducted in collaboration with France and Japanese group

Backup

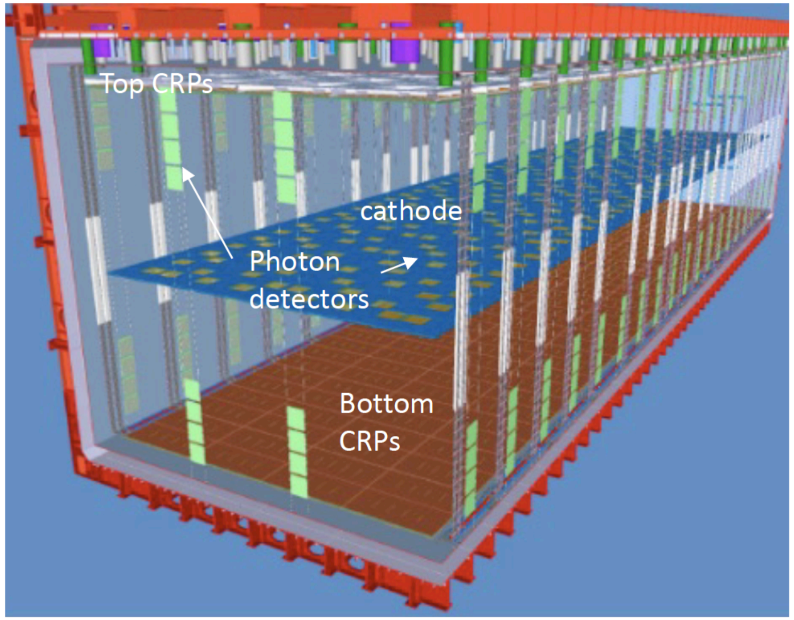
The DUNE Far Detector

- There are two detector concepts; DUNE FD1 and FD2

- FD1
  - Holizontal Drift (HD)
    - ✓ ~3.5 m drift length (drift voltage of 180 kV),
  - Active volume: ~13.66 kt
    - ✓ 4 drift volumes
  - Charge readout: 3 layers wire planes



- FD2
  - Virtical Drift (VD)
    - ✓ ~6.5 m drift length (drift voltage of 300 kV),
  - Active volume: ~14.19 kt
  - Charge readout: Charge Readout Plane (CRP) consists of perforated PCB, reducing overall costs to FD1



Requirements on the TDE

Label	Description	Specification (Goal)	Rationale	Validation
DP-FD-2	System noise	$< 1000\ e^-$	Studies suggest that a minimum of 5:1 S/N on individual strip measurements allows for sufficient reconstruction performance.	ProtoDUNE and simulation
DP-FD-4	Time resolution	$< 1\,\mu s$ ($< 100\,ns$)	Enables 1 mm position resolution for 10 MeV SNB candidate events for instantaneous rate $< 1\,m^{-3}ms^{-1}$.	
DP-FD-13	Front-end peaking time	$1\,\mu s$ ($1\,\mu s$ achieved in current design)	Vertex resolution; 1 us matches 3mm pitch and DP S/N ratio.	ProtoDUNE and simulation
DP-FD-14	Signal saturation level	7,500,000 electrons	Maintain calorimetric performance for multi-proton final state; takes into account an effective CRP gain of 20 in the DP signal dynamics.	Simulation
DP-FD-19	ADC sampling frequency	$\sim 2.5\,MHz$	Match $1\,\mu s$ shaping time.	Nyquist requirement and design choice
DP-FD-20	Number of ADC bits	12 bits	ADC noise contribution negligible (low end); match signal saturation specification (high end).	Engineering calculation and design choice
DP-FD-21	TPC analog cold FE electronics power consumption	$< 50\,mW/channel$	No bubbles in LAr to reduce HV discharge risk.	Bench test

Vertical Drift:

Noise< 1000 e-
Peaking time 1 us
Dynamics 500k e-
12 bit ADC
2 MHz sampling
< 50 mW/ch

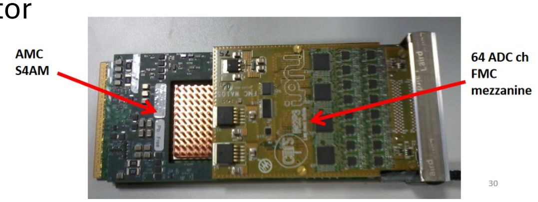
R&D at IP2I since 2006:

- Cryogenic ASIC amplifiers (first cryo-ASIC in the world in 2007)
- uTCA digitization
- ethernet DAQ
- Timing distribution; White Rabbit

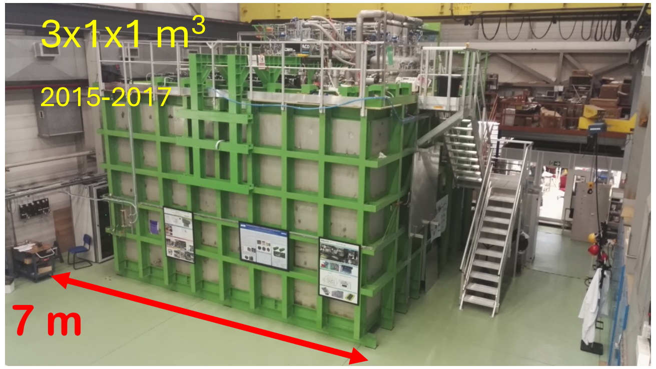
Labex LIO Institut des Origines de Lyon

2009 first μTCA system with prototype digitization AMCs

AMC demonstrator 2014



Validation with large-scale applications and prototyping activities at the CERN Neutrino Platform
(EHN1 Hall and Bd 182) 2015-2023



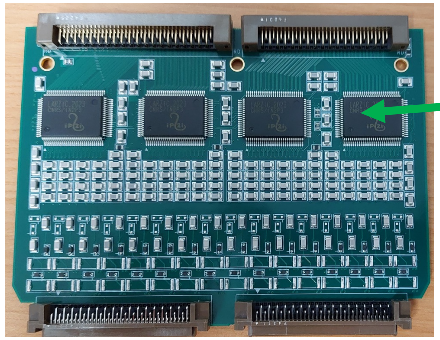
<u>TDE Development activities completed in 2023</u>

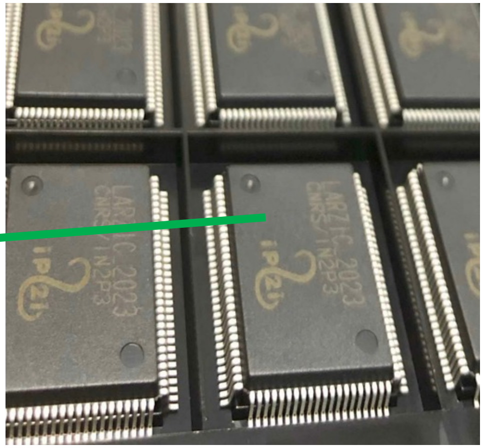
<u>Production for FD-VD in progress since beginning of 2024 (see next slide)</u>

Readout System for the top-drift volume of FD-VD
80 CRP, 3072 channels/CRP, 246k total channels

Nominal number of elements to be installed on FD-VD (production in progress 2024-2026):

- 3840 cryogenic FEB boards (64 channels) with ASIC 16 channels amplifiers



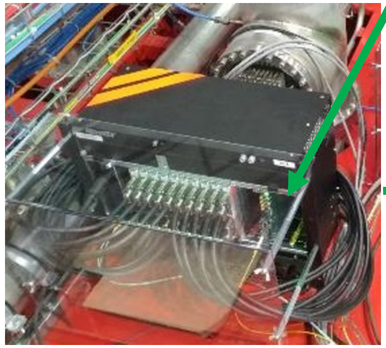


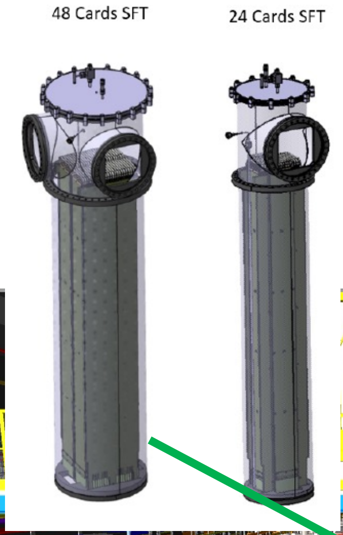
- LARZIC cryogenic ASIC amplifiers 15360 pieces

- 3840 AMC Digitization boards (64 channels)

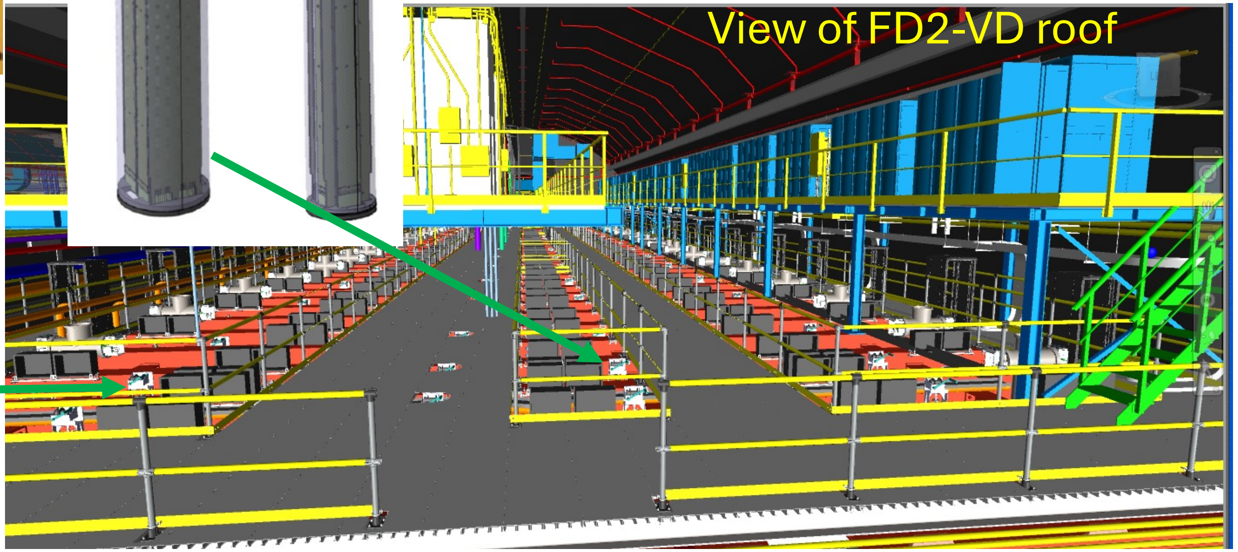
Timing system White-Rabbit
- 320 WR-MCH

- 320 µTCA systems with 25 Gbit/s MCH





- 105 Chimenys hosting 48 or 24 FEB boards (Mechanics)



Top Drift Charge Readout Electronics operating on the roof of NP02 ProtoDUNE Vertical-Drift at CERN after detector integration exercise completion (June 2023)