FKPPL - TYL/FJPPN annual workshop
18-22 May 2026
https://conference-indico.kek.jp/event/364

New generation of MAPS-based telescope with the sensors planned for the Belle II upgrade

J. Baudot for
Miho Yamada (TMCIT)
Christian Finck (IPHC)

- → Context of Beam telescope for Belle II vertex upgrade
- → SOI telescope (2025)
- → MALTA telescope (2026)
- → OBELIX telescope (2027)

Bamboo forest in Hamamatsu park materialising particle tracks

Belle II vertex detector upgrade

SuperKEKB & Belle II project

- $e^+ + e^-$ collision physics at the intensity frontier
  $\sqrt{s} = M_{\Upsilon(4S)}$ => b, c, τ super-factory
- Current world record $\mathcal{L}_{peak} = 0.52 \times 10^{35}$ cm^{-2}.s^{-1}
- Continuous improvement + upgrade in 2032

$\mathcal{L}_{peak} \sim 6 \times 10^{35}$ cm^{-2}.s^{-1}

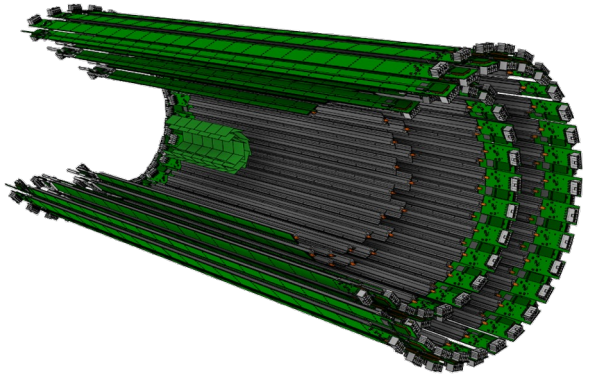
Long Shutdown 2

- New interaction region
- Uncertainties on beam-background rates
- Opportunities to improve performance

New vertex detector

The VTX project

- Mandate:
  - Increased space-time granularity
  - Improved robustness / rate & radiation
  - Simplified system
- Proposal: 5 pixel layers with the same sensor for all



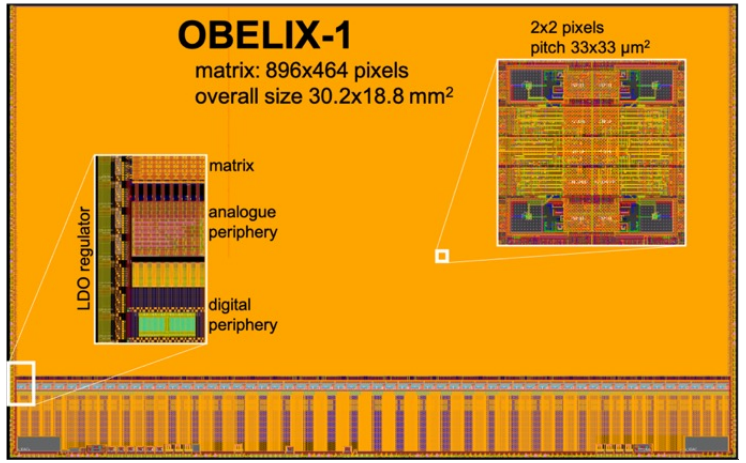
Use of CMOS monolithic pixel technology = OBELIX

Belle II Framework Conceptual Design Report arXiv:2406.19421

OBELIX (Optimized BELle II pIXel) sensor

	OBELIX
Pitch	33 µm
Signal ToT	7 bits
Integration time	50 To 100 ns
Time stamping	~5 ns for hit rate < 10 MHz/cm^2
Hit rate max for 100% eff.	120 MHz/cm^2
Trigger handling	30 KHz with 10 µs delay
Trigger output	low latency ~100 ns with low granularity
Power (with hit rate)	200 – 300 mW/cm^2 (1 to 120 MHz/cm2)
Bandwidth	1 output @ 320 MHz

- **Matrix core**
  - Re-use of **TJ-Monopix2** TOWER 180 nm Imaging
  - Improved threshold tuning
  - Cross-talk mitigation
- **New digital logic**
  - Timing & triggering



=> Precise timing

=> Large hit-rate

=> track-triggering

Tolerance to 5e14 n_{eq}/cm^2 at 30-40 °C

Large test campaign required

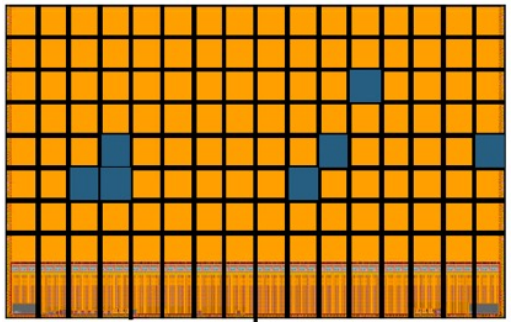
- **Powering**
  - Integrated voltage regulator
- **Planning**
  - OBELIX-1 in fab since 2026, May 1st (~1year delay)
  - **Test to start in October 2026**
  - OBELIX-2 in 2027

Track-triggering with OBELIX / VTX & CDC

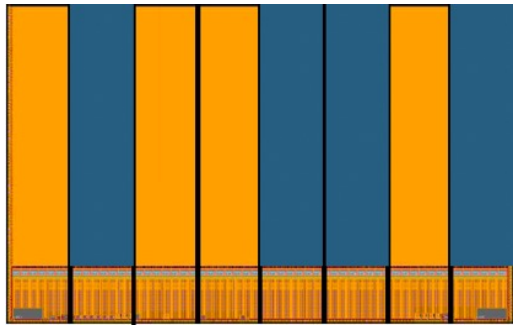
Initial work by Mattéo MAUSHART (TYL student in 2024) followed by Taichiro Koga (KEK) & Yiwei Huang (Nankai U.)

OBELIX capabilities

- Granularity reduced to 8 striplets/sensor
- Output latency ~100 ns



~400k pixels, >>µs latency

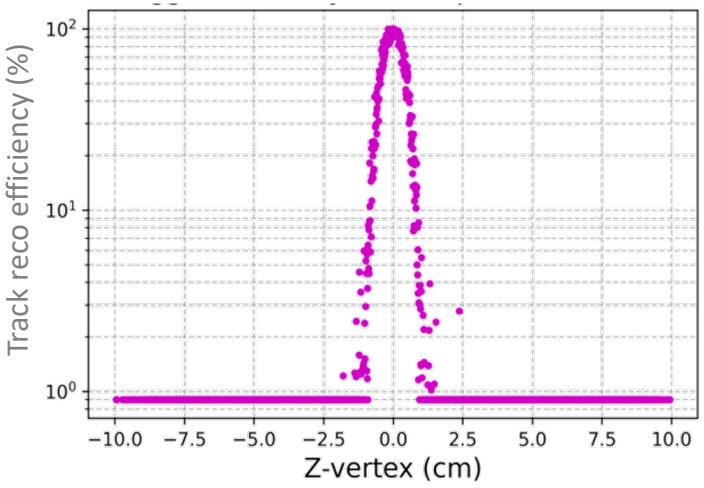


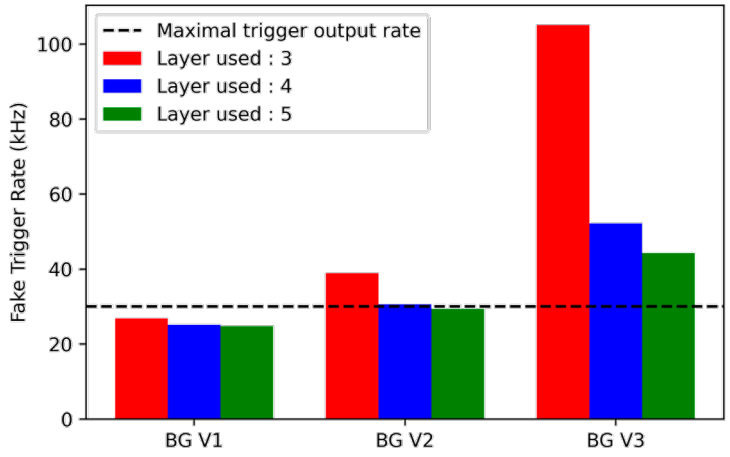
8 sriplets, ~100 ns latency

Simulation in Belle II

- Track reco VTX alone: hit-patterns stored in look-up table

=> Excellent efficiency & z-resolution / bad fake rate





➢ Now VTX+CDC combined
mitigate fake rate << kHz

Perspective for beam telescope

- Auto-trigger

Partners in this collaboration

TMCIT

- **Miho Yamada**

IPNS/KEK

- Yuji Enari
- Akimasa Ishikawa
- Katsuro Nakamura
- Toru Tsuboyama
- Shijie Wang (Master student)

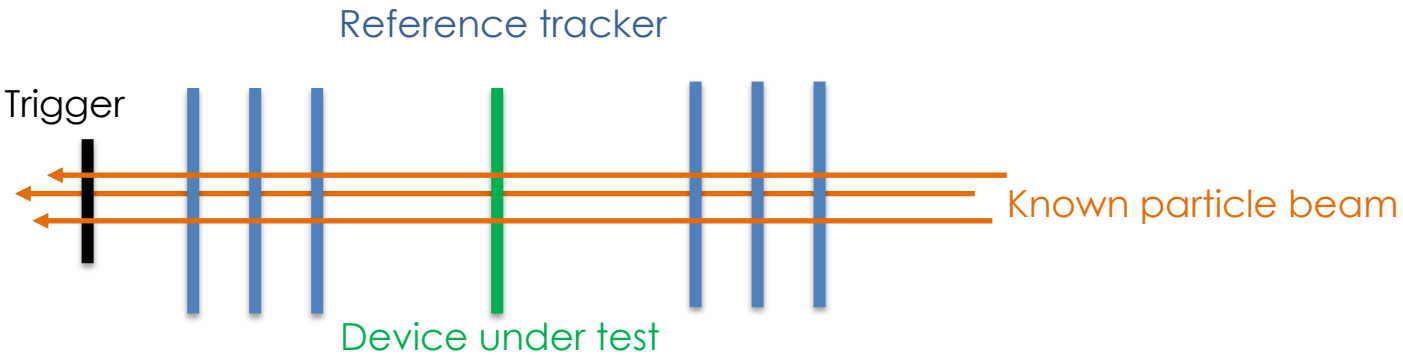
IPHC / TYL

- Jerome Baudot
- **Christian Finck**
- Mathieu Goffe
- Thomas Jacques (Master student)
- Mattéo Maushart (PhD student)
- Jérémy Marguin (Master/PhD student)
- Thomas Lauber (Master student)

Roles of beam telescopes

- Concept

TDAQ
& Control



- Sensor technology development

Comparing to refence
=> sensor performance

- System requirements
  - Tracker resolution ~ device tested
  - Tracker bandwidth yields statistics

- D_RD_39 project: evaluate OBELIX for Belle II & step up telescope
  - **Current phase**: prepare telescopes (SOI, MALTA) for OBELIX and others
  - **Next phase**: prepare telescope with OBELIX

SOI Telescope

- **Tracking reference planes**
  - INTPIX4 SOI sensor
  - Matrix (832x512) 14.1 x 8.7 mm^2
  - Pixel pitch 17 x 17 µm^2
  - Analogue pixel read-out
  - Digitized (12bits) in external SEABAS2 board

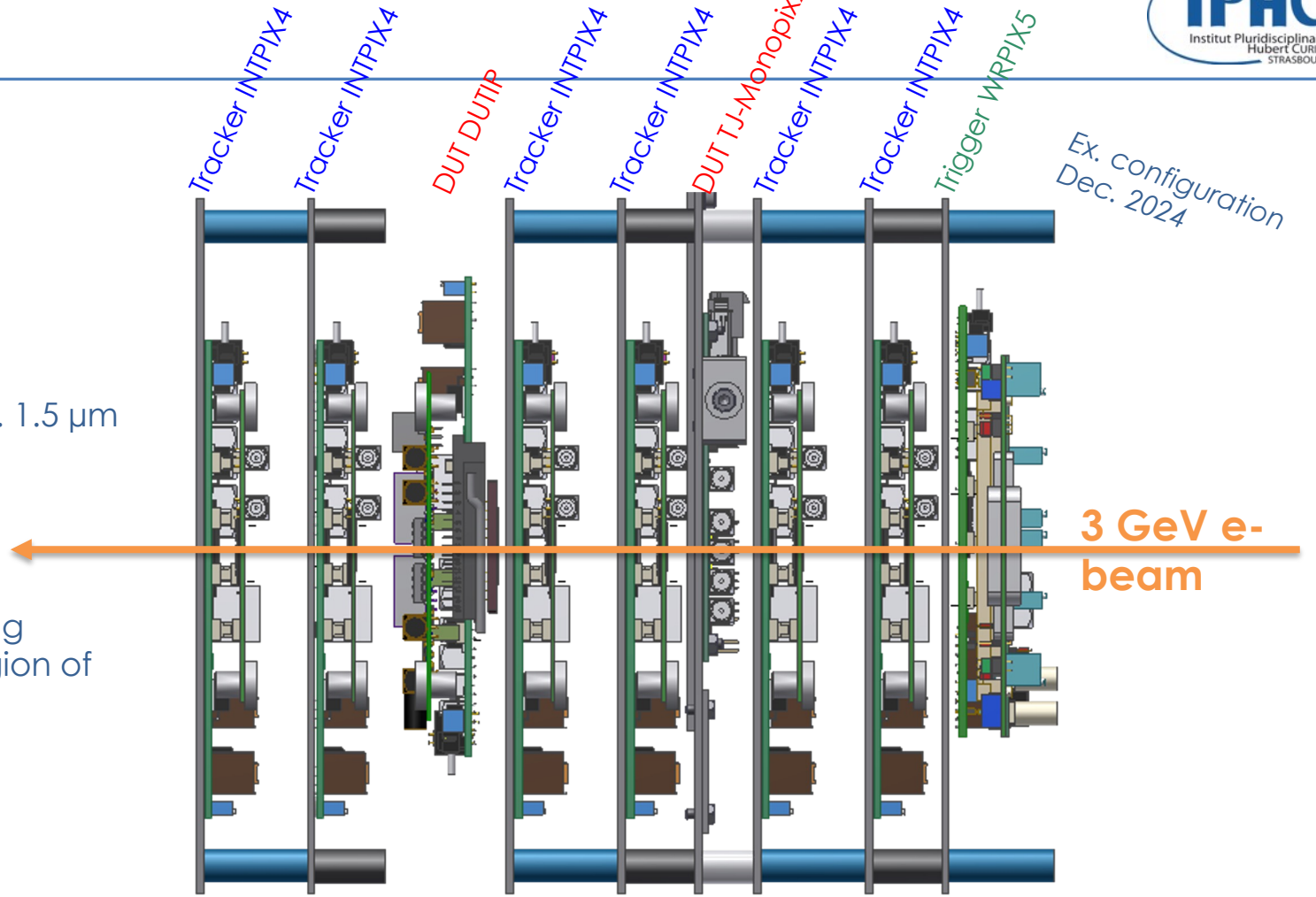
  } Position resol. 1.5 µm

- **Triggering planes**
  - XRPIX5 sensor
  - Matrix (608x384) 21.9x13.8 mm^2
  - Pixel pitch 36 x 36 µm^2
  - Binary pixel read-out

  } Triggering over region of interest

- **Verious devices already tested**
  - DuTIP SOI sensor
  - TJ-Monopix2 CMOS sensor

Outcome of D_RD_24



+ Newly developed trigger logic (USAGI) distributed to all boards

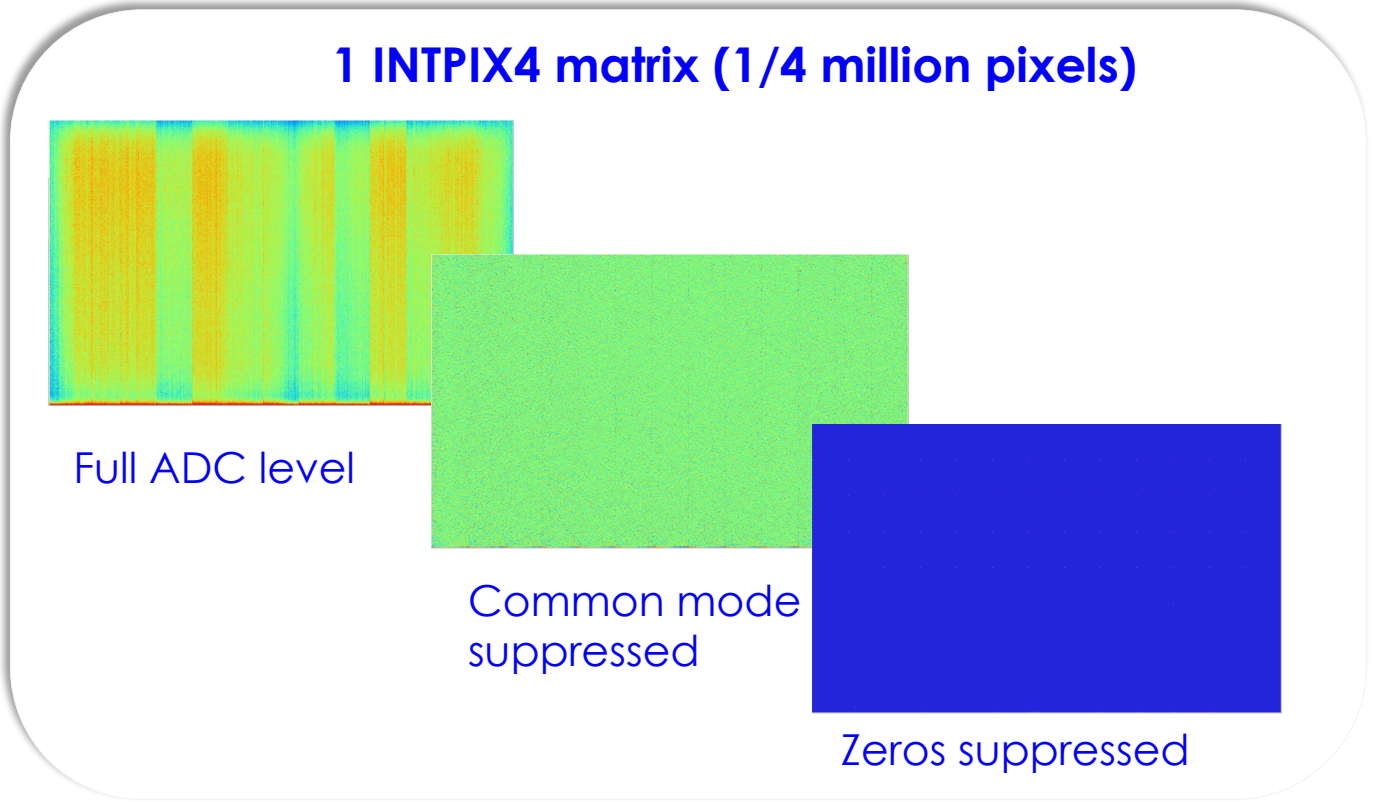
=> Typical track rate at DUT ~100 Hz

Improving the SOI telescope

- Event size issue
  - Analogue output yield **~900 kB / event** => ~300 GB / hour (test campaign ~week)

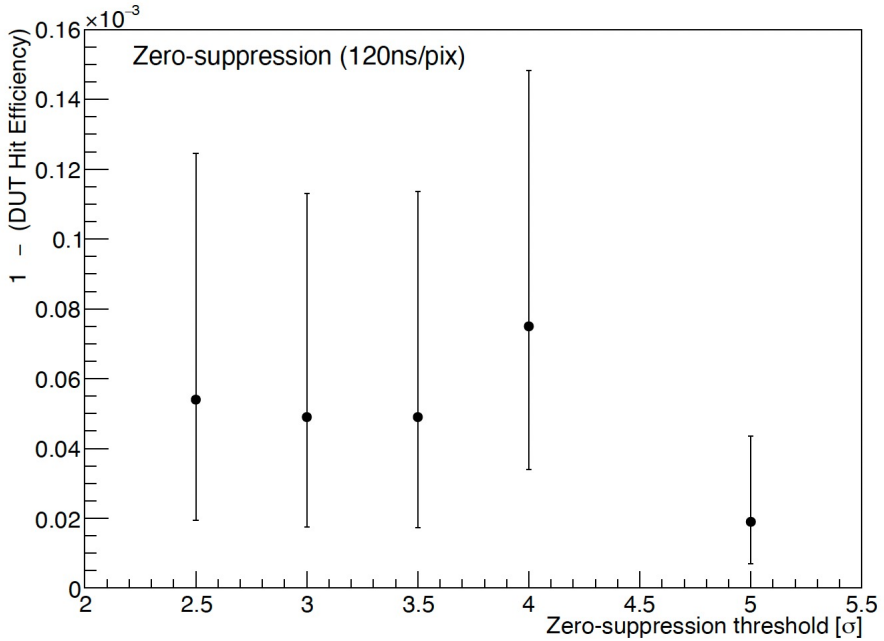
  => Storage and analysis issue

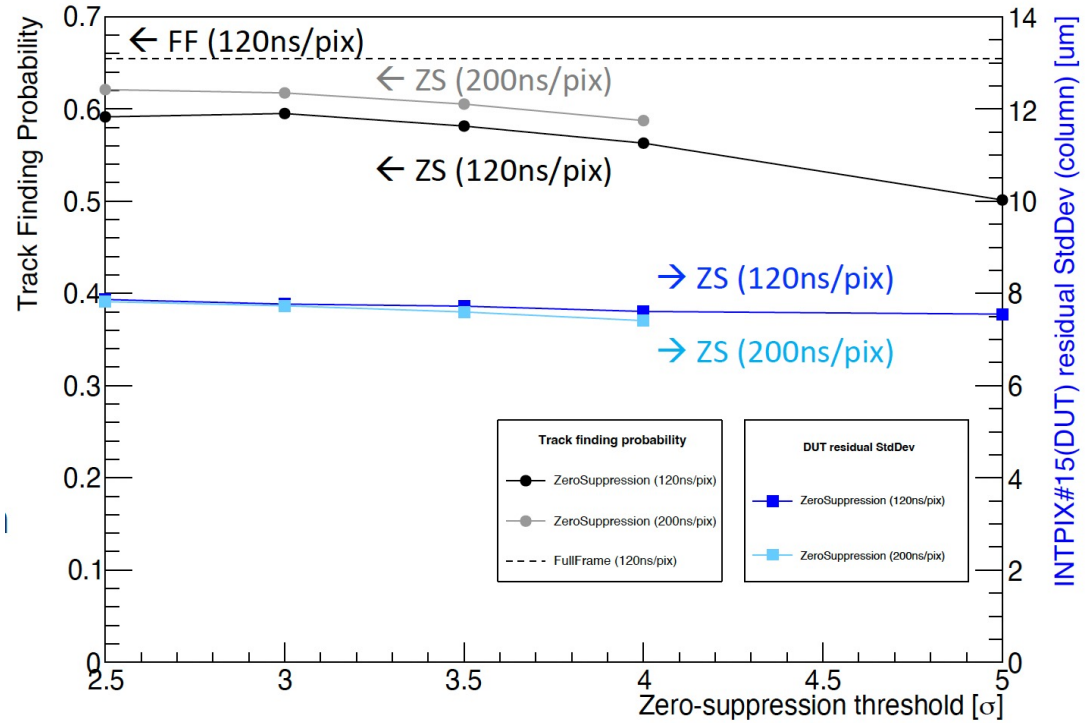
- Cure: introducing 0-suppression
  - Firmware upgrade on SEABAS2
  - Work implemented at KEK
    - Belle II VTX group (K. Nakamura *et al.*)
    - SOI-telescope group (M. Yamada *et al.*)
    - IPHC student visiting in Summer 2025 (T. Laubert)
  - Final size: **~500 B / event**



SOI-telescope: 0-suppression validation

- Beam test at KEK PF-AR beam line (Winter 2026)
  - 3 GeV electrons
  - 85 Hz event rate
  - 6 INTPIX4 sensors (one used as DUT)
  - Analysis framework (Corryvreckan), Shijie Wang





Inefficiency < 0.01%

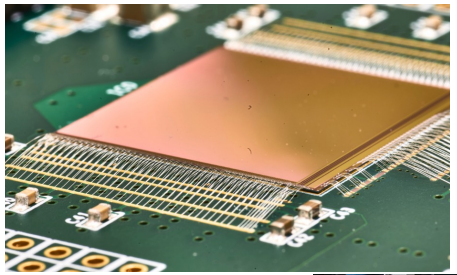
MALTA telescope: higher rate

Tracking reference plane

- MALTA sensor
- Matrix (512x512) 18.6 x 18.6 mm^2
- Pixel pitch 36.4 x 36.4 µm^2
- Binary pixel read-out Position resol. 10.5 µm

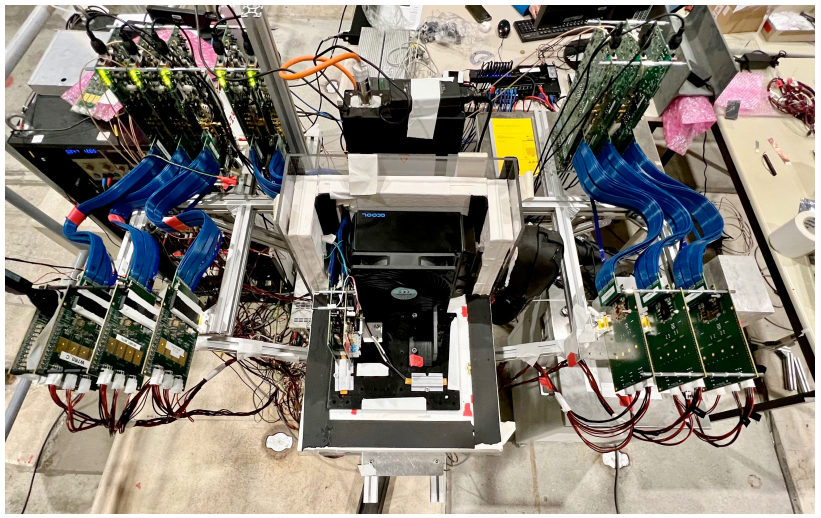
- Readout & trigger logic with commercial FPGA

Trigger rate up to 50 kHz

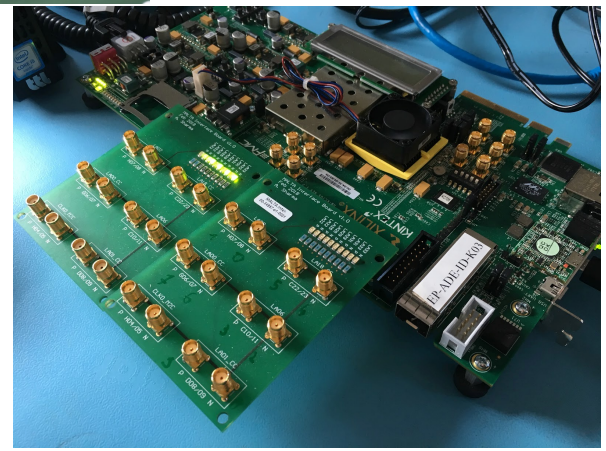


Malta sensor

FPGA boards readout & trigger



CERN SPS setup
Extrapolation resol. 4.1 µm
Time resol. 2.1 ns



Current activity

- ITDC group
- IPHC-student visiting in Summer 2026 (request pending)

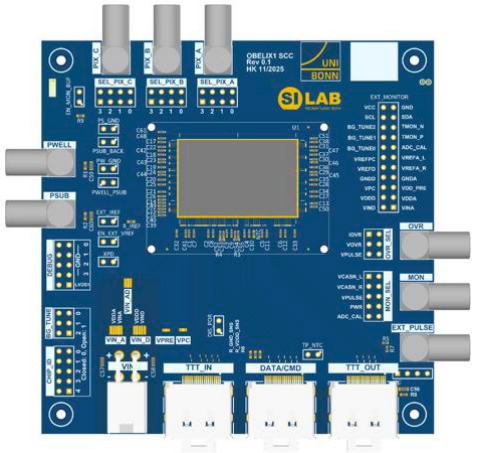
⇒ Commissioning MALTA planes
⇒ Setting up TDAQ system

Plan for OBELIX-based beam telescope

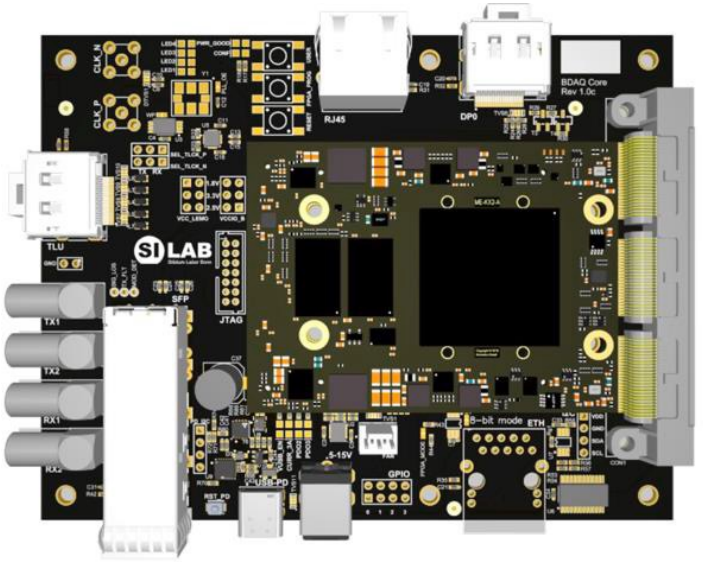
- New facility proposed in DRD3
  - Various European partners
  - Replicas of same telescope in CERN, DESY, KEK
  - 6 large area high-resolution / high-rate detector planes for tracking & triggering
  - DAQ & control, similar to Belle II-VTX system
  - Operated through standards (EUDAQ, Corry)

=> Proposed innovation:
track-trigger on beam particles

Boards prepared @ Bonn (VX collab.)



Chip carrier



BDAQcore

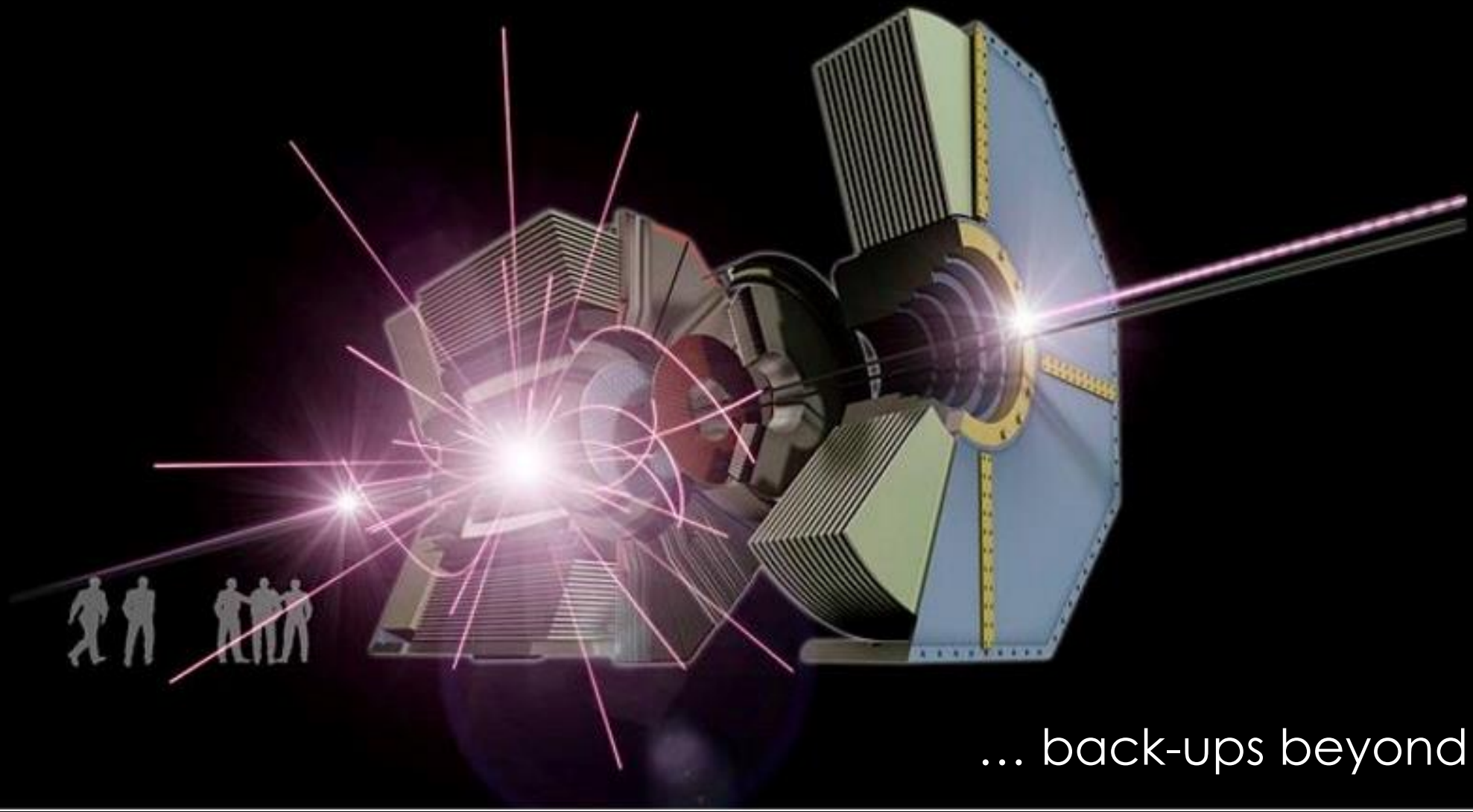
=> Major opportunity to
- Experience long period of data taking with OBELIX & associated system
- Enhance test facilities

Summary & Outlooks

- **Well established SOI telescope improved => ready for next test campaign**
- **MALTA telescope is main topic in 2026 => possibly first test campaign this Winter**
- **OBELIX-1 expected back ~October 2026 => to be characterised this Winter with both telescope**
- **Basic bricks for OBELIX-1 telescope being prepared**
  => OBELIX-telescope only a topic for 2027

Bridge in Hamamatsu park

Thank you …



… back-ups beyond this point

Proposal for new project 2025-2029

Slide from 2025

- Principle investigators: Miho Yamada (TMCIT), Christian Finck (IPHC)

- New generation of sensors to characterise
  - CMOS: OBELIX-1 starting in 2026, OBELIX-2 at the horizon of 2028
  - SOI: DuTiP-2 starting in 2025
  - Re-use of SOI telescope => possible modification of trigger logic

- New generation of beam telescope
  - Exploit all features of OBELIX-1 for high hit-rate & track-triggering
  - Potential commissioning in 2027

MAPS R&D between France & Japan

Science & R&D

Belle II

Vertex upgrade
with OBELIX sensor

ALICE

ITS upgrade
ALICE-3

- ***Other FJPPN talks***
  Y. Okazaki (D_RD_29)
  R. Guernane (nex)

DRD3

R&D for new MAPS generation
with TPSCo 65 nm

French groups

@ IN2P3

TYL / FJPPN

@ KEK

ITDC 測定器開発センター Instrumentation Technology Development Center

Japanese groups

Education

MAPS Academy

KEK, 23-30 July 2025
20 students Asia/America/Eu
https://wiki.kek.jp/display/mapschool/MAPS+Academy

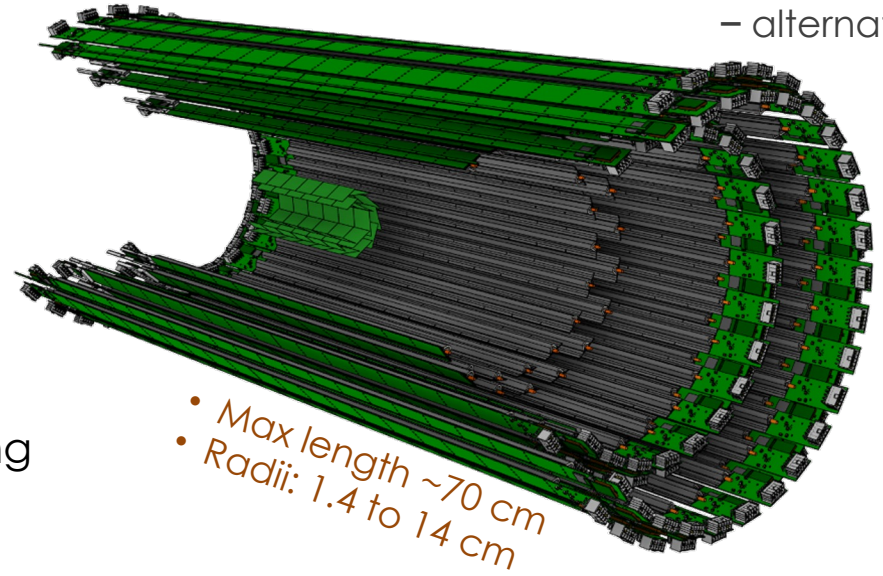
Test facility

AR Test Beam Line

VTX main concepts

- **2 inner layers: iVTX**
  - "On" beam pipe for IP resolution
  - Full-silicon concept:
    - material ≲ 0.2 % X_0 / layer
    - single-side connexion

- **3 to 4 outer layers: oVTX**
  - at least 3 points for track seeding
  - Light & thin support:
    - material ≲ 0.8% X_0 / layer
    - single-side connexion whenever possible
  - Straight sections => adaptable to any IR



- **Same sensor everywhere**
  - Space & time granularity
    => occupancy ≪ 1%
  - Depleted MAPS: **OBELIX**
    - alternative SOI: DuTIP

- **System**
  - Optical links asap

- **Fast track reconstruction**
  - Full resolution for High Level Trigger
  - Reduced granularity for L1 trigger

Framework Conceptual Design Report arXiv:2406.19421 [hep-ex]

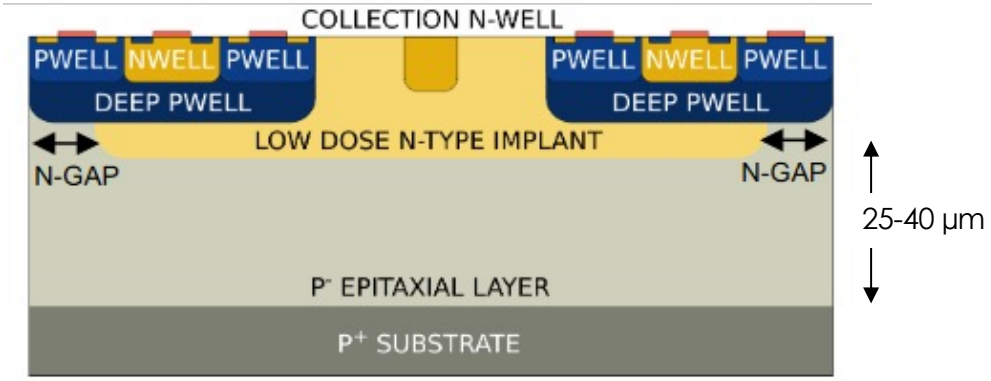
Recap of D_RD_24 project: 2021-2025

Context of Belle II vertex detector upgrade

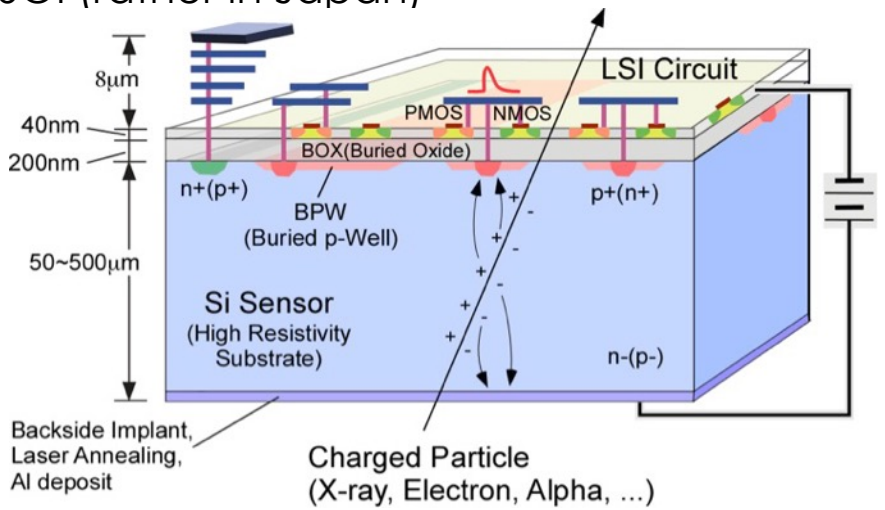
- Motivation: **more robustness against higher beam background** with higher lumi / current DEPFET and Strip sensors
- Proposed solutions: **single monolithic sensor & simple/light system**

2 technologies of monolithic sensors

- CMOS (rather in France)



- SOI (rather in Japan)



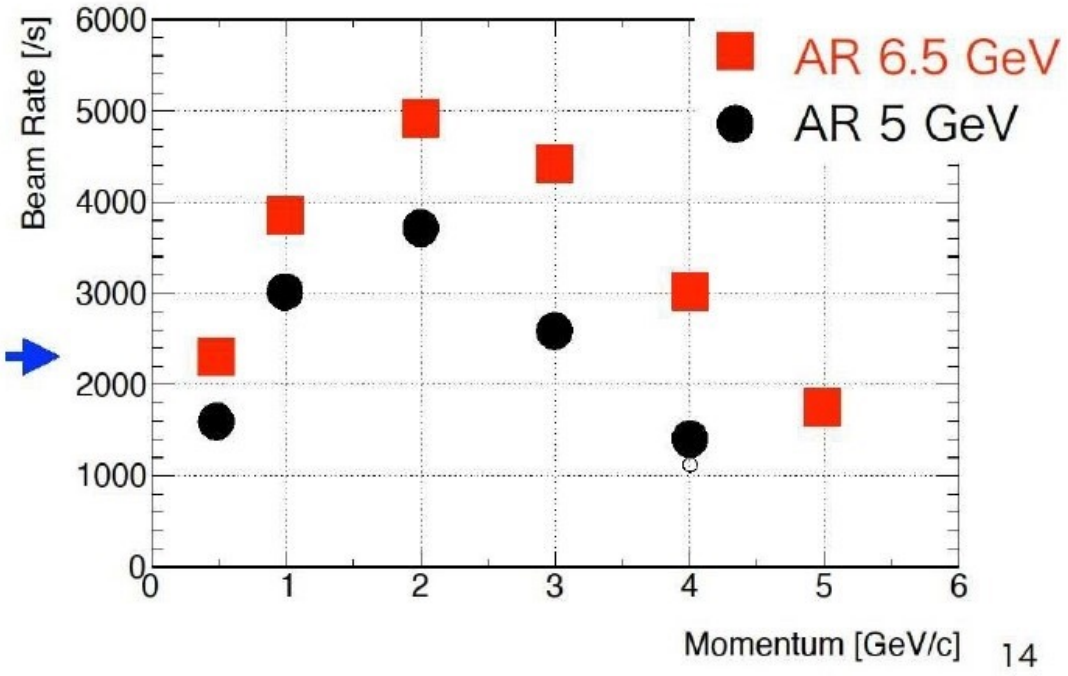
Franco-Japanese project to progress in parallel

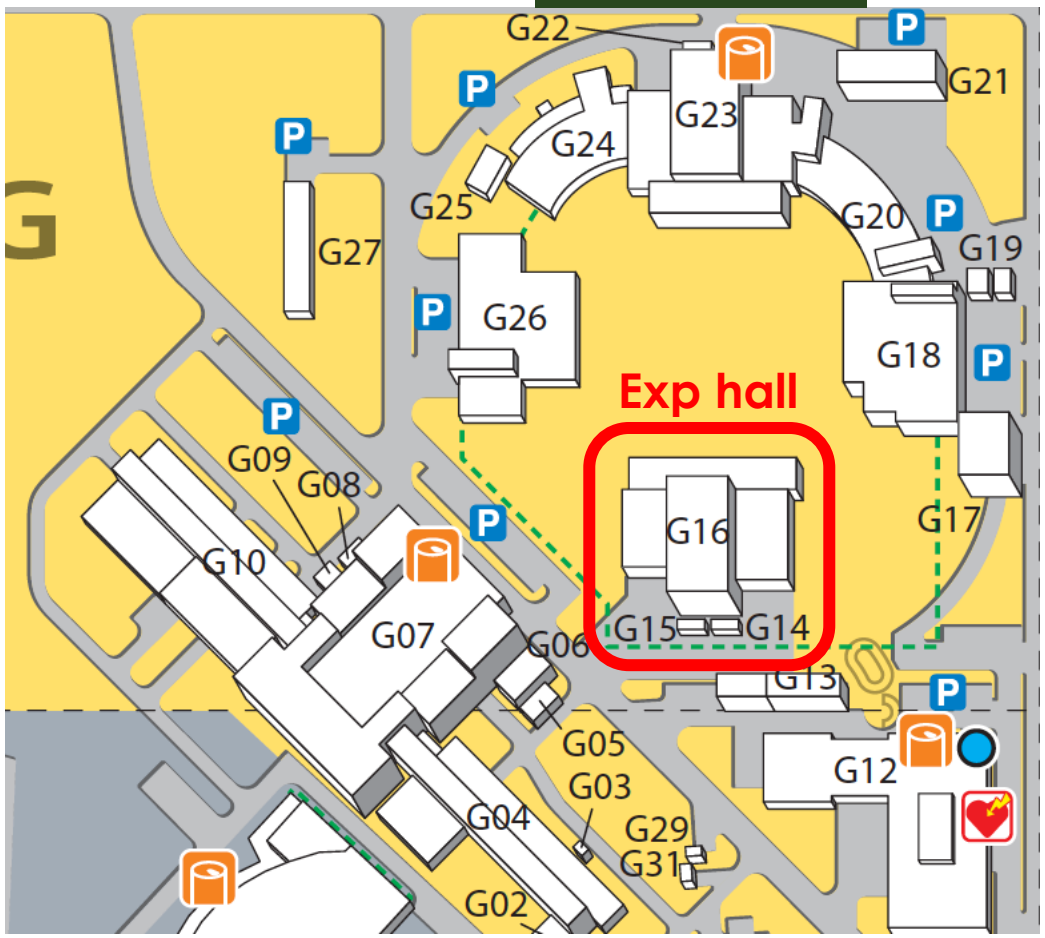
- Initial phase: discussing specifications & exchanging expertise on sensor design
- **Final goal: common beam test with both technologies**

KEK ITDC PF-AR test e- beam line

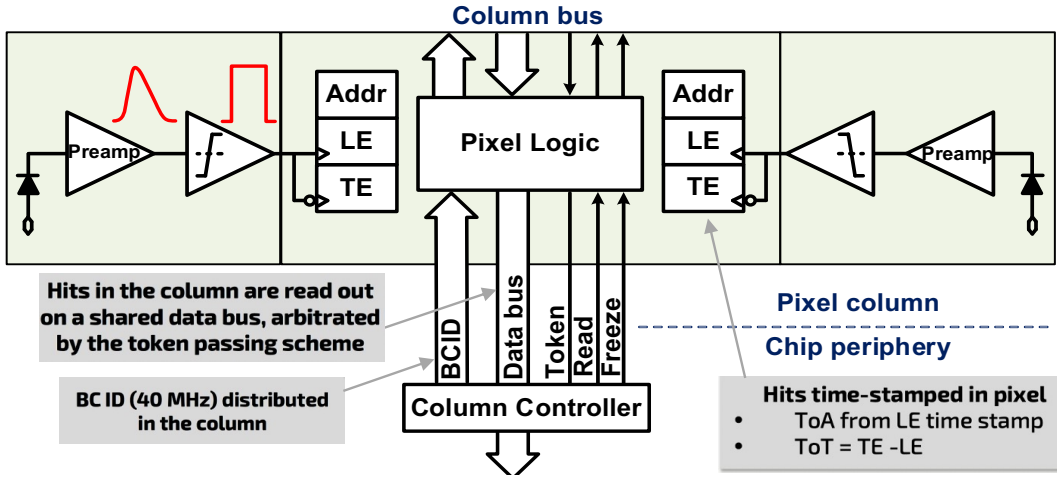
- https://itdc.kek.jp/testBeamLine/index.html
- K. Hanagaki, JPS 2020 Autumn Meeting https://kds.kek.jp/event/35569/

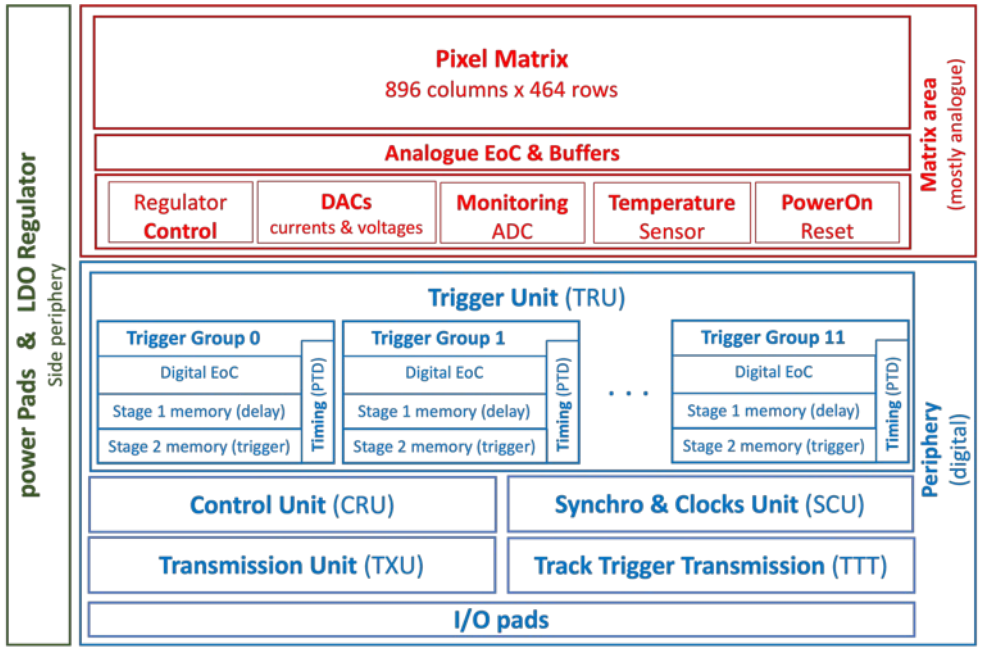
- Current max rate ≲ 1 kHz





Design of OBELIX-1

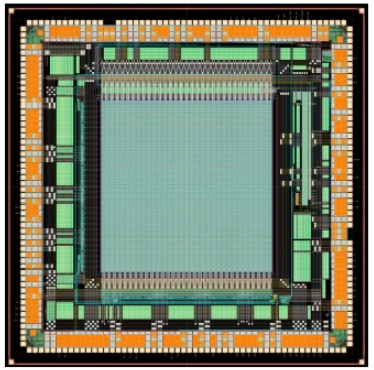




- ## Matrix design
  - Extended copy of TJ-Monopix2
  - 2 front-end falvours: **DC- and AC- casocode**
  - Clock for time-binning slowed down: 100ns
- ## Powering
  - LDO regulator for easier voltage distribution
  - Overall power depends on hit rate: 200-300 mW/cm^2
- ## Trigger Unit
  - Simulated with realistic inputs: 120 MHz/cm^2
  - Can sustain 800 MHz/cm^2 for 0.5 µs
- ## Fine time stamping
  - 6 ns achievable with end-of-column fast clock
    - Limited to hit rate <^ 10 MHz/cm^2
- ## Track trigger
  - Reduced granularity to 8 striplets (~4 x18 mm^2)
  - Increased transmission rate: 33 MHz

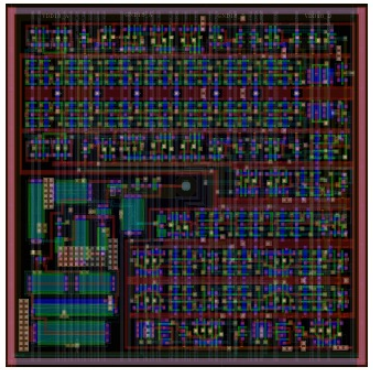
DuTiP series

DuTiP1 (2020—)



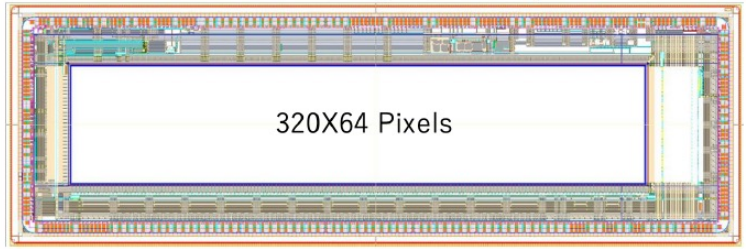
6 × 6 mm²

DuTiP1 Pixel



45 × 45 µm²

DuTiP2 (2021—)



18.4 × 6 mm²

DuTiP3 (2023—)

Pixel
- Pre. amplifier (ALPIDE type)
- Shaper
- Comparator
- Dual down time counters (7 bit)
- Timing memory (Previous/Current)

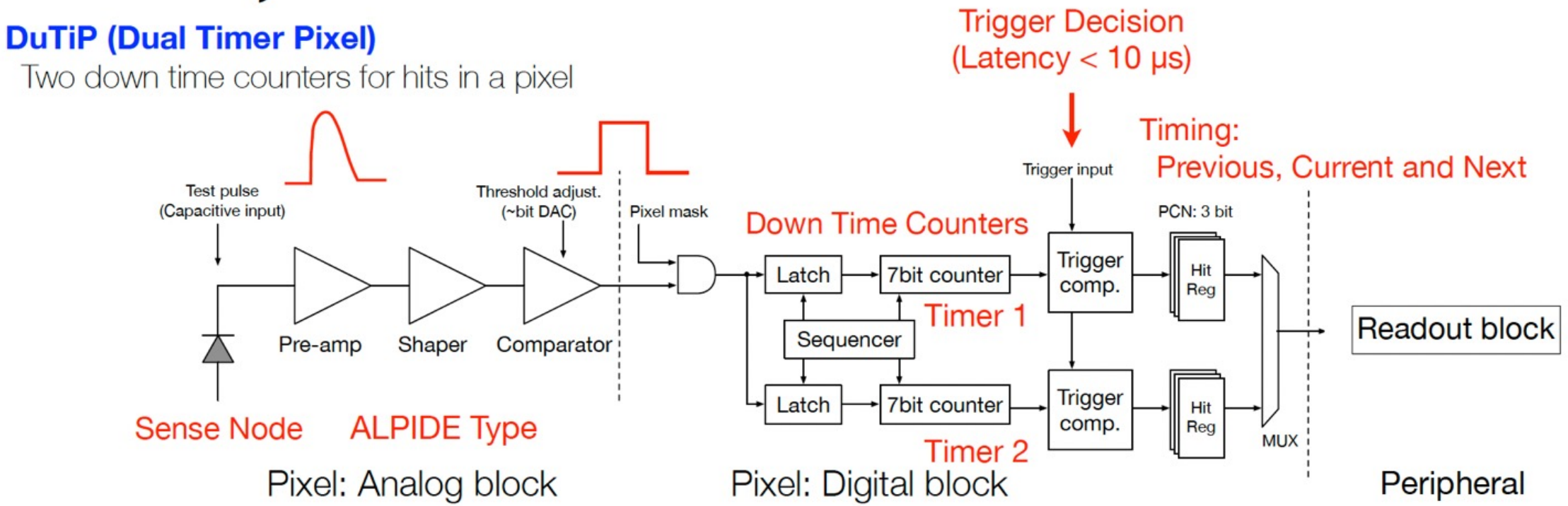
Readout
- Row address (5 bit)
- Column address (5 bit)
- 2 bit hit (Previous/Current)
- CMOS in/out

Design
- Dec. 2021 submitted → deliver in Spring 2022
- Pixel design is almost completed by DuTiP1
- Row 320 pixels (Full size for Belle II) for design of large-area sensor
- FIFO, LVDS in/out, DAC

Design
- June 2023 submitted, February 2024 delivered

Still significant amount of tests needed

DuTiP concept



Analog block: Usual configuration for the binary detector
Hit memory: Timing of Previous, Current and Next collision
Signal: Coincided with event trigger ← Down time counter corresponds to trigger latency
Background: Random, out of time window ← Suppressed by coincidence
Multiple hits in trigger latency: Multiple timer and memory are controlled by Sequencer