In radiation detector development, overall detector performance depends not only on the characteristics of the sensor but also on the electronics used to read out its signals. However, physics students involved in detector development rarely have opportunities to design and develop integrated circuits themselves.

This project originated from undergraduate research on radiation detectors, which sparked our interest in the design of their readout electronics. Starting with little prior knowledge or experience in transistor-level circuit design, we began by studying semiconductor device operation and analog circuit design, and took on the challenge of designing an ASIC from scratch.

As a first step, we designed a single-channel SiPM readout ASIC using a 0.18 $\mu$m CMOS process. The ASIC consists of a current-input stage, a pulse-shaping circuit, a comparator, and a time-over-threshold (ToT) circuit, among other blocks.

We carried out the full pre-fabrication design flow, from evaluating device characteristics using foundry-provided transistor models to circuit design, simulation, physical layout, and verification. In particular, we focused on designing the current-input stage to accommodate the large input capacitance of the SiPM while considering bandwidth, noise, and stability. The design has been submitted for fabrication through a multi-project wafer (MPW) run via VDEC, and preparations for chip evaluation are currently underway.

In this presentation, we describe the motivation behind our transition from detector development to ASIC design and the process leading to our first chip submission. We also share the technical challenges encountered and lessons learned during this first design cycle, and discuss future directions for student-led ASIC development.