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We present a new hybrid Si-CMOS imaging sensor developed for X-ray imaging and spectroscopy. The device consists of a 500 μm-thick silicon sensor bump-bonded to a CMOS readout chip with 640 × 640 pixels at a pitch of 20 μm, providing a sensitive area of 12.8 × 12.8 mm^2. A major improvement over the previous version is the integration of column-parallel ADCs on the chip, eliminating the need for external ADCs and enabling fully digital output at frame rates of up to 300 frames/s.

To investigate the trade-offs between readout architectures, the prototype chip incorporates source-follower (SF) and capacitive transimpedance amplifier (CTIA) readout circuits in separate regions. Measurements using Am-241 X-rays at −10 °C show that the apparent charge spreading is larger with SF than with CTIA readout. Similar spreading was observed in an earlier SF-only prototype (Yoneda et al., NIM A 912 (2018) 269), although its origin was not established at that time. Our current comparison suggests that capacitive coupling between neighboring pixels contributes to the larger apparent charge spreading in SF readout.

We compare the noise characteristics, charge-sharing behavior, and energy resolution of the SF and CTIA configurations. By selecting a suitable sensor region and applying block-wise gain corrections, the CTIA high-gain mode achieves an energy resolution of 0.82 keV FWHM at 13.9 keV for four-pixel clusters. This presentation will describe the sensor development, initial performance evaluation, and implications for future readout design.