

# Development of Advanced Monolithic Pixel Detector

Marc Winter\*

Auguste Besson

Jérôme Baudot

Maciej Kachel

Christine Hu-Guo

Andreï Dorokhov

Frédéric Morel

Yasuo Arai\*

Ikuo Kurachi

Akimasa Ishikawa

Toshinobu Miyoshi

Toru Tsuboyama

Kazuhiko Hara

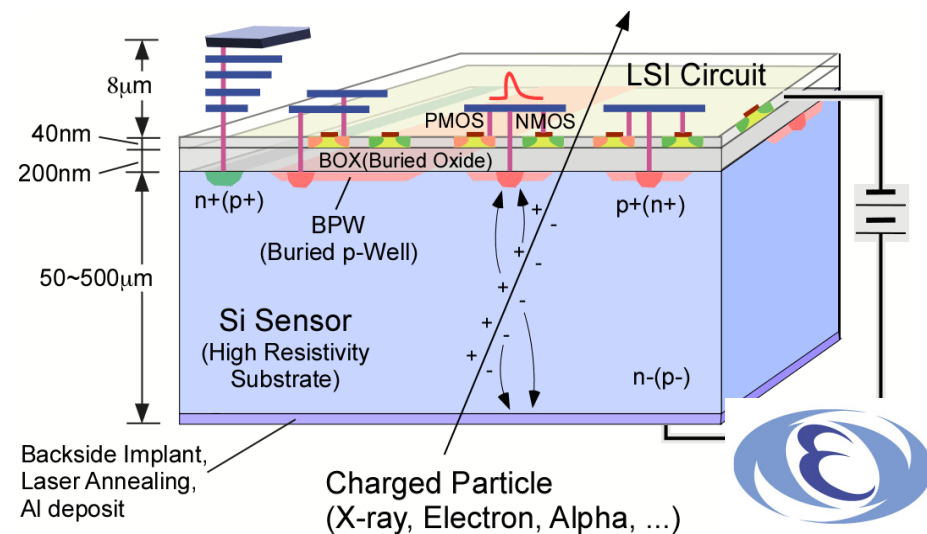
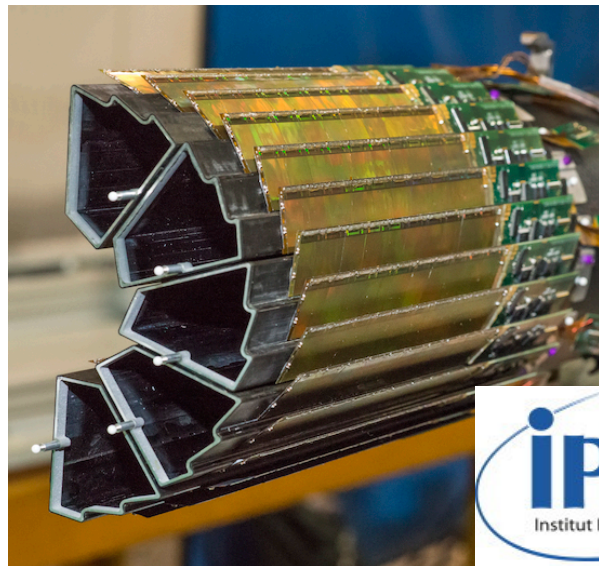
Miho Yamada



Contact address: [yasuo.aria@kek.jp](mailto:yasuo.aria@kek.jp)

# Collaboration Objective (2017~)

- Develop Advanced Monolithic Pixel Detector technology for future high-energy physics and X-ray experiments.
- Share mutual experience in pixel detector development through communication and exchange of researchers
- Challenge to meet the demanding requirements of future experiments such as ILC.



# IPHC activities in TYL/FJPPL

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## Translation of MIMOSIS pixel into the SOI technology

- MIMOSIS pixel architecture is the IPHC baseline for the future ILC sensor
- With SOI the goal is to shrink the pixel size by utilising the technology-intrinsic features: transistor merging and 3D integration.

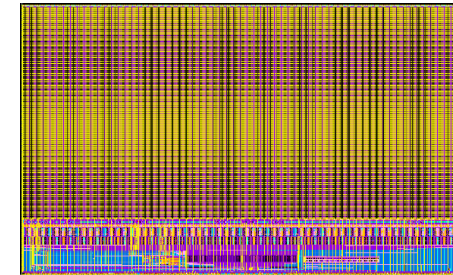
## Utilisation of SOI for spectroscopic imaging applications

- Thicker detector ( $\gg 100 \mu\text{m}$ ) than in CMOS Pixel Sensors allows efficient operation with highly penetrating X-rays and increased signal for energy measurement.

## Exploration of 3D interconnection with partners introduced by KEK

- Thanks to the FJPPL collaboration contacts, a trusted industrial partner was selected to perform the fine pitch (pixel to pixel) bonding.

### MIMOSIS



- Technology: CMOS 180 nm
- Pixel array: 504 x 1024 pixels
- Pixel pitch: 26.88 x 30.24  $\mu\text{m}^2$
- Active area: 30.97 x 13.55  $\text{mm}^2$
- Chip dimension: 31.1 x 17.2  $\text{mm}^2$
- Integration time: 5  $\mu\text{s}$

# Details of the second IPHC SOI prototype submission

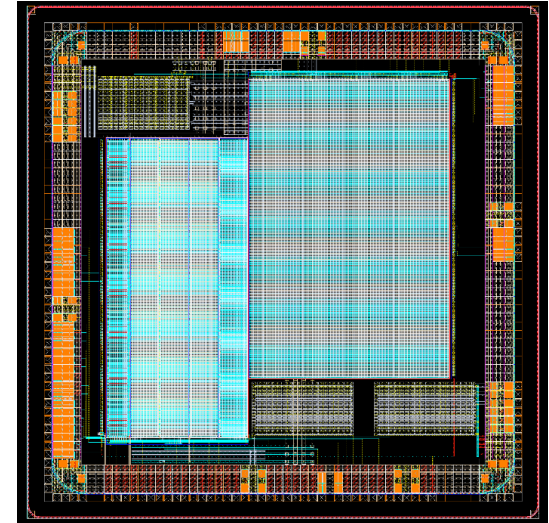
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## Technology study:

- 4 Different collecting diode designs
  - 18 $\mu\text{m}$  pitch
  - Different buried well configurations
- Synthesized block with SPI receiver

## Architecture study:

- Two different versions of MIMOSIS based pixels
  - Targeting small pitch (18x18 $\mu\text{m}$ )
  - Safe/challenging solutions
- General purpose linear amplifier:
  - Signal digitization with time-over-threshold (TOT) based pixels
  - Low noise amplifier for X-ray spectroscopy
- Matrix of global shutter pixels for X-ray experiments (pump-probe, etc.)

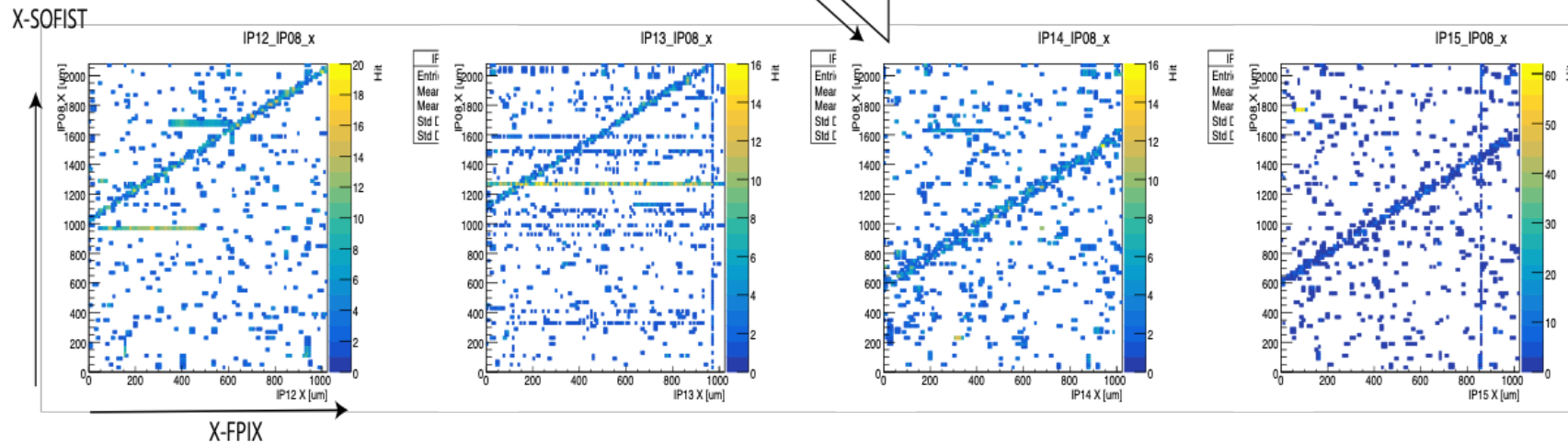
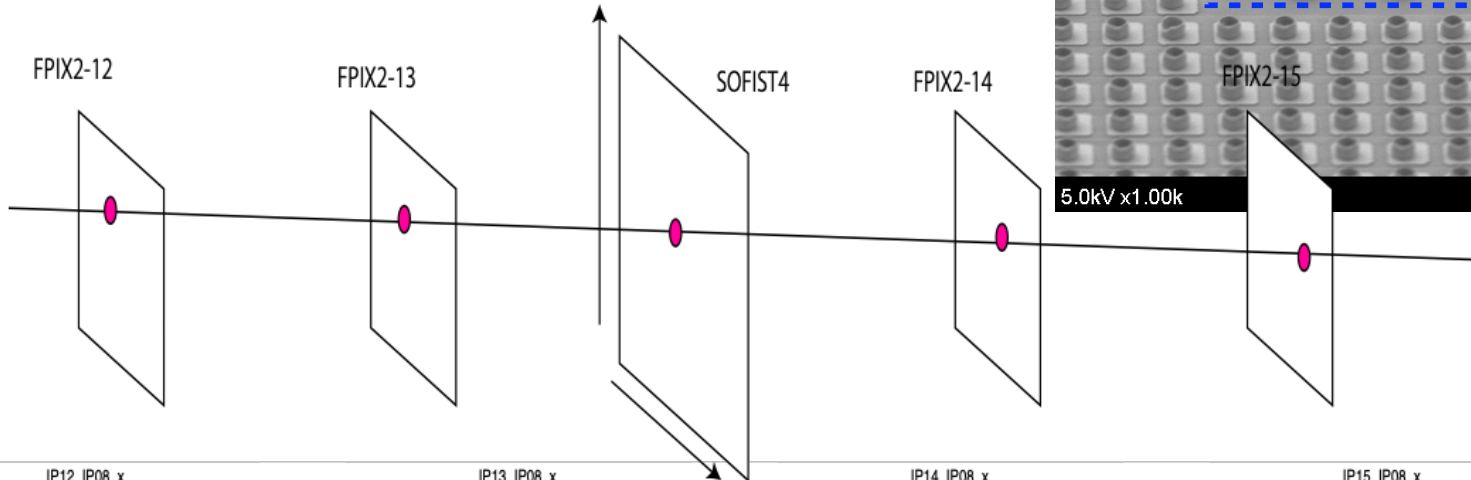
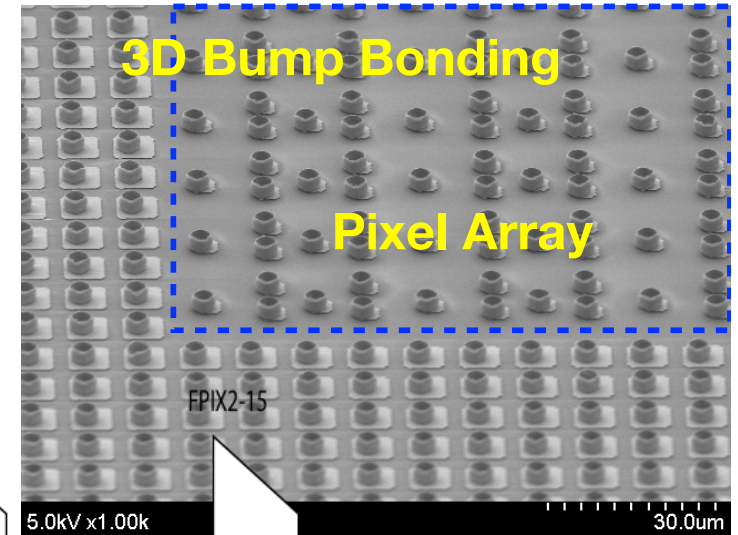


- Technology: 0.2 $\mu\text{m}$  SOI-CMOS pixel process
- Total dimension: 6 x 6 mm<sup>2</sup>

# KEK Activity of SOFIST detector

(SOFIST: SOI sensor for Fine measurement of Space & Time for ILC)

- 3D SOFIST chips were successfully bonded with cylinder bumps.
- First Beam Test of 3D SOFIST was done at Fermilab in March.



# Plan in FY2020

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- Short term visit to KEK by IPHC engineer is approved in KEK. (The schedule is postponed by the COVID-19.)
- Modified version of the IPHC SOI prototype will be submitted around June with the help of KEK.
- Digital Library for the SOI process is being developed at IPHC and ported to KEK.
- Next SOI Multi Project Wafer (MPW) run is planned at latter half of this fiscal year.
- Unfortunately, the meeting of French-Japan collaboration planned after the TYL-FJPPL workshop was cancelled. We continue to communicate through video conference.