D_RD_17 Development of high-speed detector readout system

S. YAMADA (KEK) AND D. CHARLET (IJCLAB)

Contact address : satoru.yamada@kek.jp charlet@lal.in2p3.fr

Motivation for this project

In HEP experiments;
- Improvement of accelerator
  - Higher luminosity -> higher event rate
- Improvement of detector and electronics
  - Higher granularity (e.g. silicon strip detector)
  - More information of signal (e.g. waveform digitization)

Larger amount of data

Typical data acquisition system

Detector -> A/D converter -> readout system -> event-building -> software trigger -> storage

Scalability is not so good.

After event-building :
Scalable system by parallel processing

- Readout system could be the bottleneck of DAQ system.
-> development of high-speed readout system is important to improve the total throughput of system

Goal of the project :
Upgrade the readout system of **the Belle II experiment**

The Belle II experiment

➤ Search for new physics beyond the Standard Model via high precision measurement with high statistics samples of B/D/tau decays.
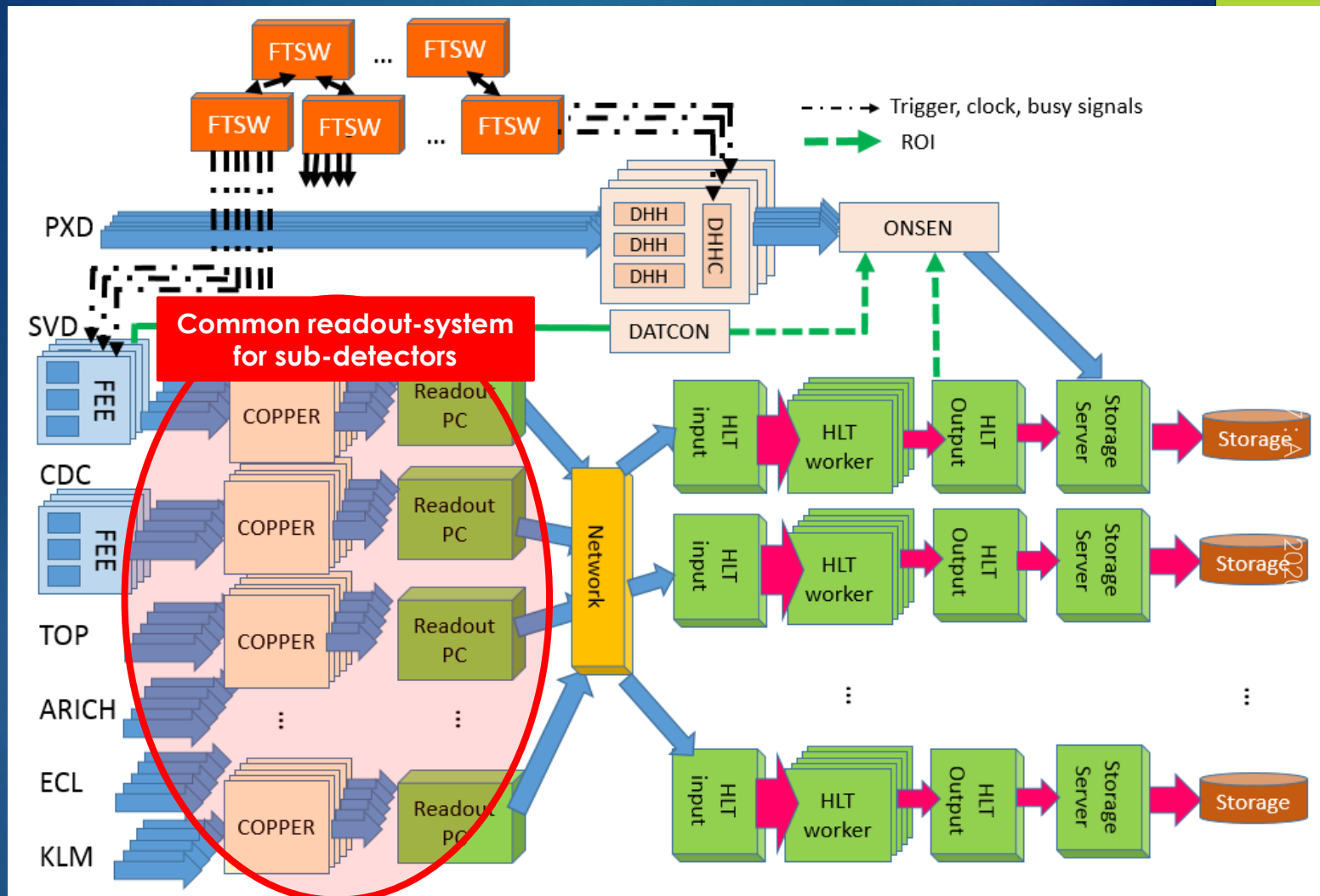
➤ **SuperKEKB accelerator**
- ➤ Designed luminosity: 40times as large as KEKB
- ➤ 50 ab^{-1} in 10 years
  (cf. 1ab^{-1} @ Belle experiment)

Belle II collaboration :
~1000 collaborators from 26 countries/regions

Increase of beam cur x2 : luminosity
Smaller beam size x20   x40
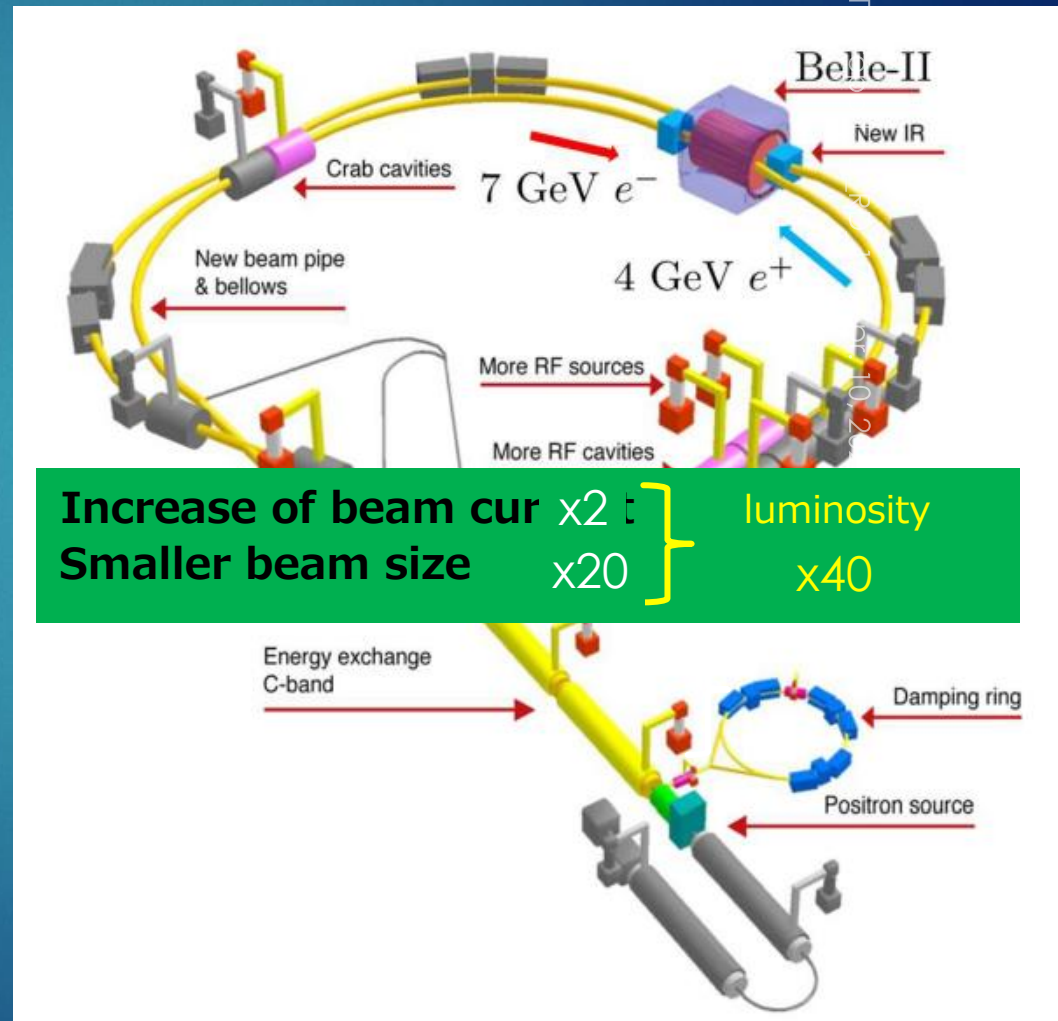
- ➢ Readout data from FEE(Front-End Electronics)s for six sub-detectors other than Pixel detector
- ➢ Formatting, data-checking and partial event-building should be done

4

Issues to be considered for the current readout system

Difficulty in maintenance during the entire Belle-II experiment period

- ➢ Four different boards, COPPER(main VME9U board) and its three daughter cards, should be taken care of.
- ➢ The number of discontinued parts is increasing.

Limitation in the improvement of performance of DAQ

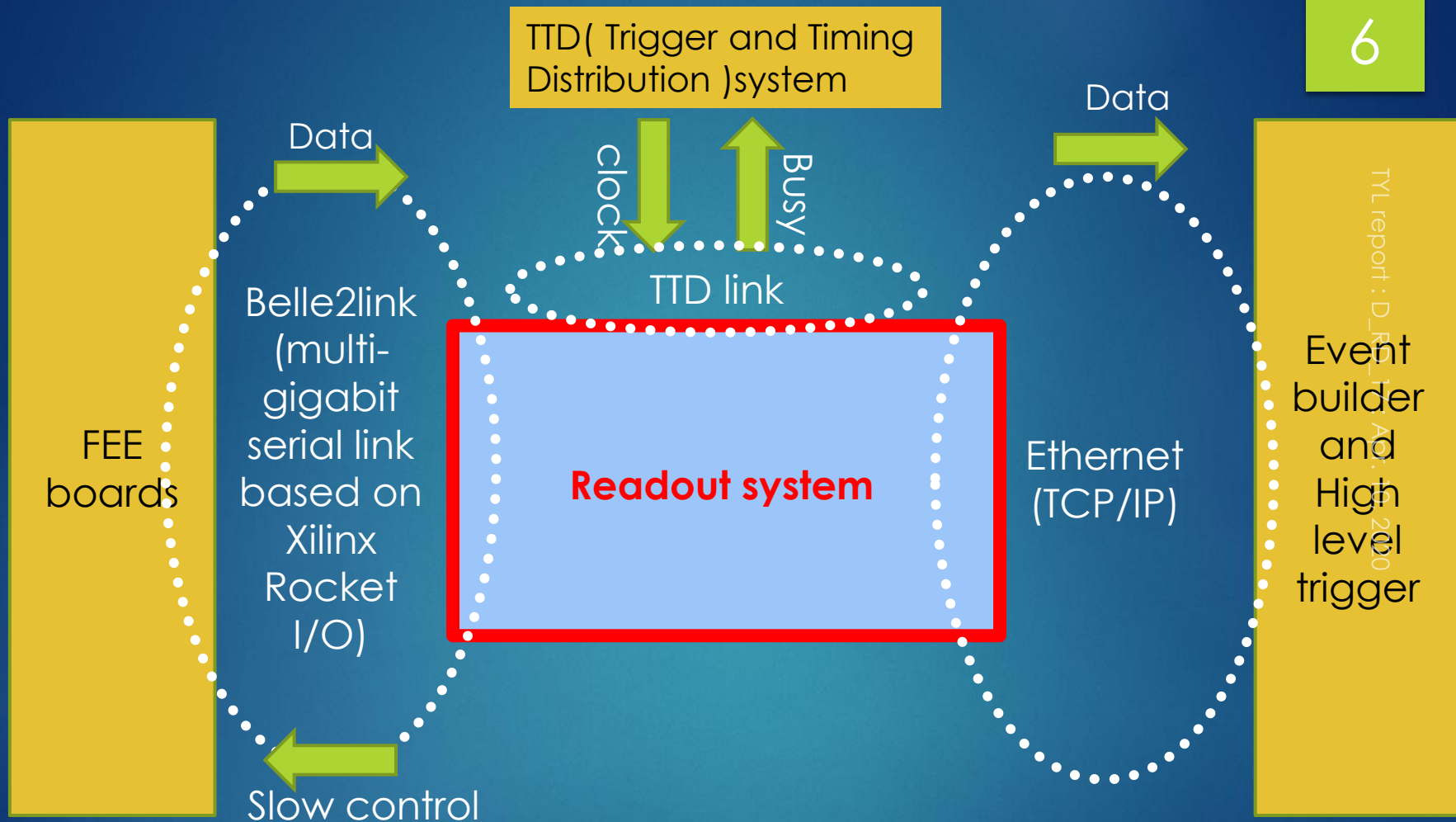- ➢ A. Bottlenecks of the current COPPER readout system
  - ➢ CPU usage on COPPER
    - ➢ About 60% COPPER-CPU is used at "30kHz L1 trigger rate with 1kB event size/COPPER"(=Belle II DAQ target value)
  - ➢ Data transfer speed from a COPPER board
    - ➢ 1Gbps/COPPER (Gigabit ethernet)
- ➢ B. Bottleneck due to network output of ROPC
  - ➢ 1Gbps/COPPER (Gigabit ethernet)
- ➢ We need to upgrade the readout system when
  - * luminosity of SuperKEKB exceeds expectations.
  - * Higher background than expected
  - * Lower threshold of L1 trigger is used or trigger-less DAQ is realized.

TYL report : D_RD_17 : Apr. 10, 2020

TTD(Trigger and Timing Distribution)system

Data

Data

clock

Busy

TTD link

Data

FEE boards

Belle2link (multi-gigabit serial link based on Xilinx Rocket I/O)

Readout system

Ethernet (TCP/IP)

Event builder and High level trigger

Slow control

➢ Three interfaces with the other part of the DAQ system should be kept so that It does not require further modification of the other subsystems.

- Proposal based on PCIe40 boards used by ALICE and LHCb for their detector upgrades (full detector readout at 40 MHz and software trigger)

- Final hardware available and well tested at CERN

- Based on large Intel/Altera Arria 10 FPGA, with 48 bidirectionnal links

| item	people
PCIe40 firmware and driver software	**D.Charlet , P.Robbe, ,E.Jules , E.Plaige ,M.Taurigna (IJCLab)**
Slow control firmware/library	**Q. Zhou (KEK),** H. Purwar(Hawaii) (+ **P. Robbe and D. Charlet**)
User logic part of FW, DAQ software on readout PC	**S. Yamada (KEK) (+ P. Robbe and D. Charlet)**
FW development of TTD interface in PCIe40	**T. Kunigo, M. Nakao(KEK),** H.Purwar(Hawaii)
Readout test and commissioning	**Q. Zhou, S. Yamada(KEK),** H. Purwar(Hawaii)
Slow control software upgrade for handling larger # of channels	O. Hartbrich (Hawaii), **S. Yamada, Q.Zhou(KEK)**

- ➤ PCIe40 related firmware and software (e.g. Belle2link, PCIexpress interface, driver software etc.) -> IJCLab experts
- ➤ Implement of Belle II DAQ functionalities (data-formatting, checking ,slow control etc.) -> KEK DAQ group + UH group
- ➤ Test and commissioning   : KEK DAQ group + UH UH group

Test setups in KEK and IJCLab

➢ There are three test benches for new PCIe40 readout system.
➢ FEEs of sub-detectors(TOP, CDC, SVD and ARICH) can be connected.
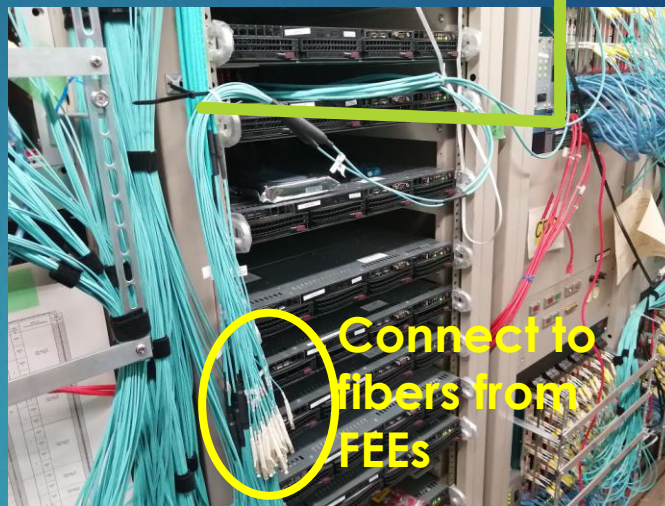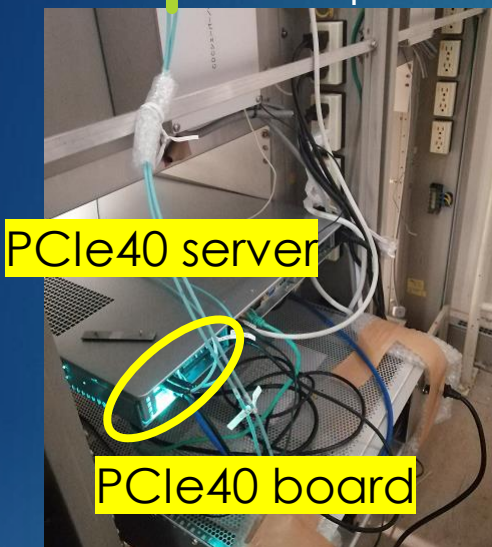
KEK Tsukuba Hall test bench
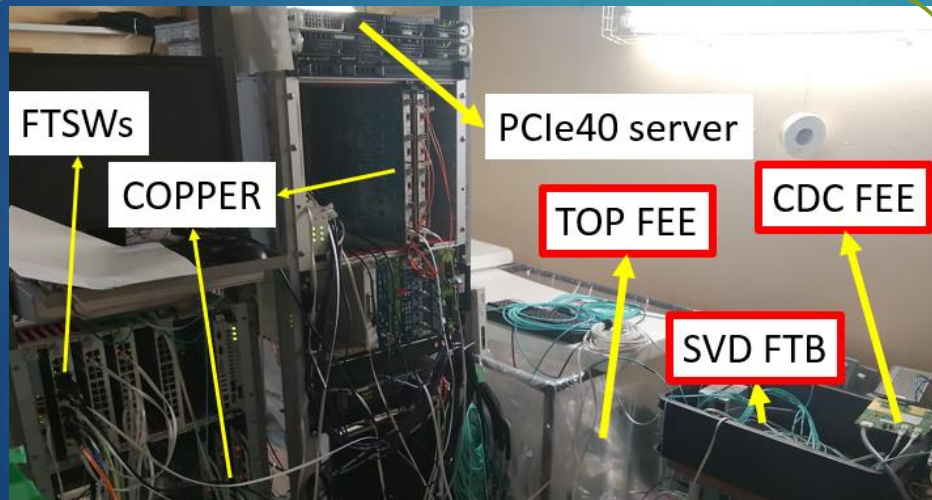
IJCLab test bench

CDC
+
ARICH
FEEs

TYL report : D_RD_17 : Apr. 10, 2020

READOUT TEST AT KEK

Optical fibers (12cores cables)

PCIe40 server

PCIe40 board

Connect to fibers from FEEs

Example of read-out data

TOP readout test with 4 FEEs (The FEEs were not configured yet.)

```
00000034 7f7f0001 02c13f00 0000001e 27b853a7 5e269114 1a160060 00000000
0000000a ffaa0100 27b872f0 0401a04a 00000005 013a2145 ffff011e 00000a00 001eb623 ff554103
0000000a ffaa0101 27b872c0 0401a058 00000005 013a2145 ffff011e 00000a00 001e0a90 ff554202
0000000a ffaa0002 27b872c0 0401a029 00000005 013a2145 ffff011e 00000a00 001e4075 ff554302
0000000a ffaa0003 27b872b0 0401a067 00000005 013a2145 ffff011e 00000a00 001e452d ff554401
7fff0000 7fff0004 7fff0005 7fff0006 7fff0007 7fff0008 7fff0009 7fff000a
```

Data from 4 FEEs

➢ Currently just dumping data from PCIExpress to PC's disk.
  ➢ CRC check/Unpacker software's check needs to be done

PCIe40 proposal was selected by Belle II collaboration in Oct. 2019

| : Committee meeting

2018

2019

2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10

B2GM   B2GM   QWS   TRGDA   B2GM   B2GM   B2GM   B2GM

Preparation of Requirements documents

Call for proposals

Recommendation
of the committee :
R&D phase until
2019 Oct.

LoI for R&D phase from 3 proponents

R&D phase

Readout test At TOP test bench
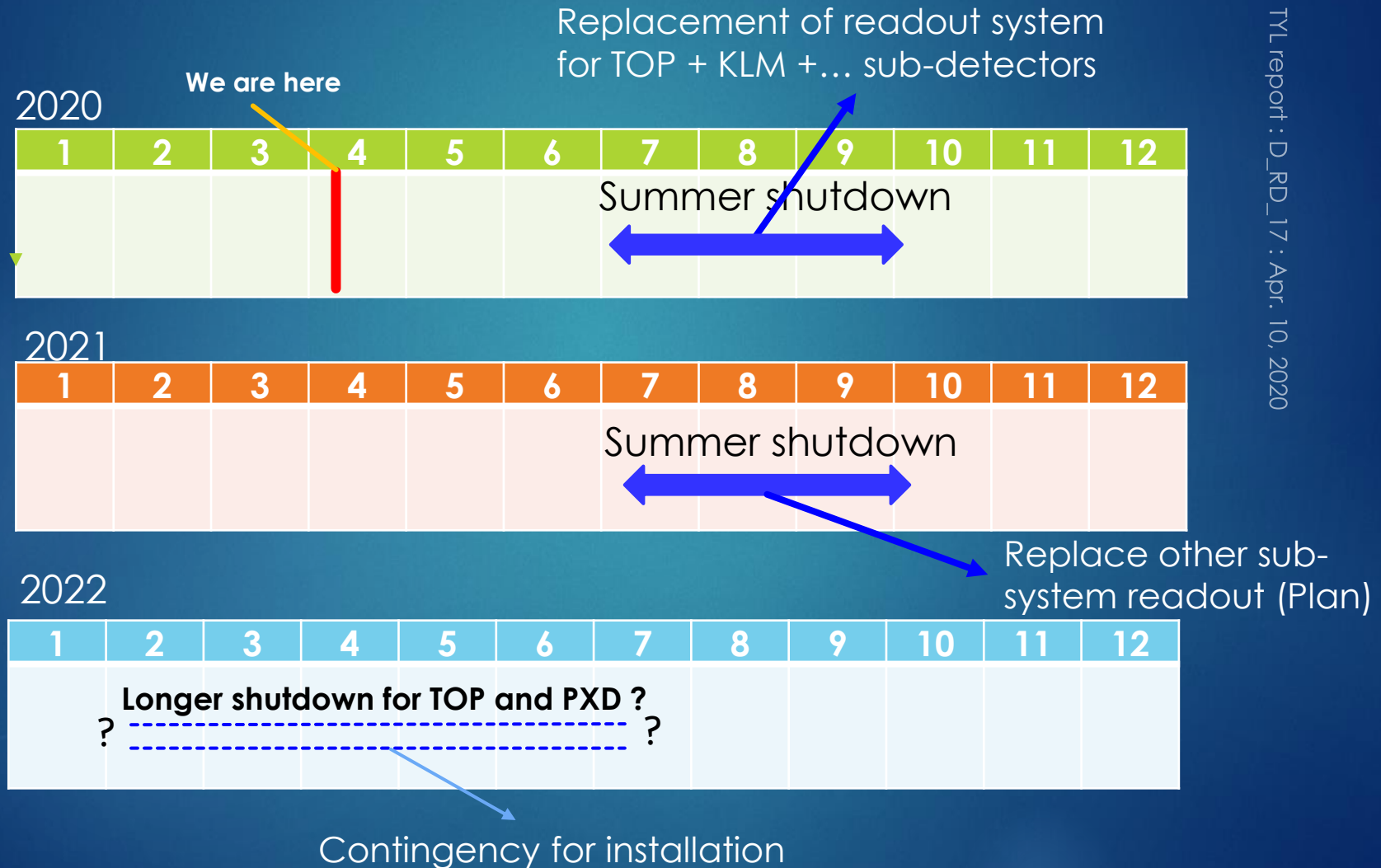
Down-selection
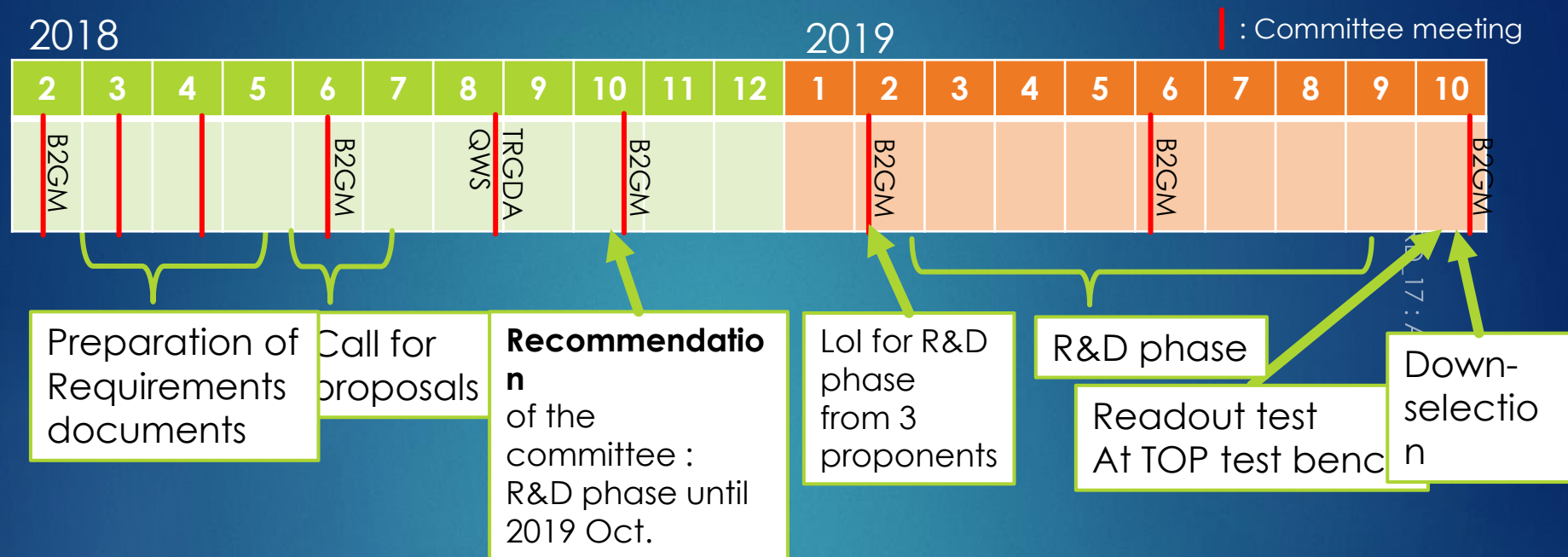
- ➢ The committee was formed to make recommendation for the upgrade
- ➢ Call for proposals for the DAQ upgrade to gather collaboration-wide resources and expertise
- ➢ A simple readout test was performed by proponents at TOP(a PID detector of the Belle II) test bench to demonstrate the capability of new systems.
- ➢ PCIe40 proposal was selected by the Belle II management.

Installation plan

➢ Installation will be done during accelerator shutdown period
➢ Running the current system+PCIe40 system in parallel
(The current readout system will be in hot-standby operation)

Replacement of readout system
for TOP + KLM +… sub-detectors

We are here

2020

1	2	3	4	5	6	7	8	9	10	11	12

Summer shutdown

2021

1	2	3	4	5	6	7	8	9	10	11	12

Summer shutdown

Replace other sub-system readout (Plan)

2022

1	2	3	4	5	6	7	8	9	10	11	12

Longer shutdown for TOP and PXD ?
? -- ?

Contingency for installation

Current Members of the D_RD_17 project

French group		Japanese group	
Name	Laboratory	Name	Laboratory
Daniel Charlet	IJCLab	Satoru Yamada	KEK
Christophe Beigbeder	IJCLab	Ryosuke Itoh	KEK
Eric Jules	IJCLab	Mikhiko Nakao	KEK
Emi Kou	IJCLab	Qidong Zhou	Nagoya univ.
Francois Le Diberder	IJCLab	Takuto Kunigo	KEK
Eric Plaige	IJCLab		
Patrick Robbe	IJCLab		
Monique Taurigna	IJCLab		

Collaborative efforts are ongoing between IJCLab and KEK

Belle II DAQ upgrade project

IJCLab

KEK members
visited in Feb. 2020

IJCLab members
visited at KEK a few times in JFY2019

KEK

TYL report : D_RD_17 : Apr. 10, 2020

Summary

➤ High-speed readout system is one of the key component in HEP DAQ system to keep up with the improvement of accelerator and detector.

➤ The Belle II experiment started operation in February, 2018 and our target is to upgrade its readout system.

➤ PCIe40 board-based solution was proposed to the Belle II collaboration and was approved in Oct. 2019.

➤ Develoepment of firmware and software are ongoing and successfully read data from front-end electronics of Belle II sub-detectors at a test bench.

➤ Partial replacement of the Belle II readout system is planned in the summer of 2020.