# Development of Advanced Monolithic Pixel Detector for the ILC experiment (D_RD_25)


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On behalf of

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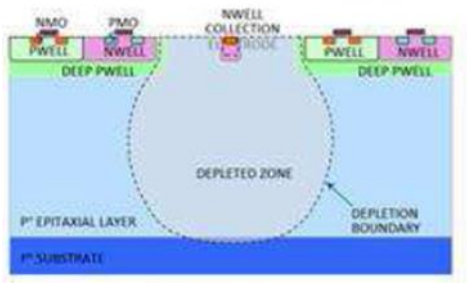
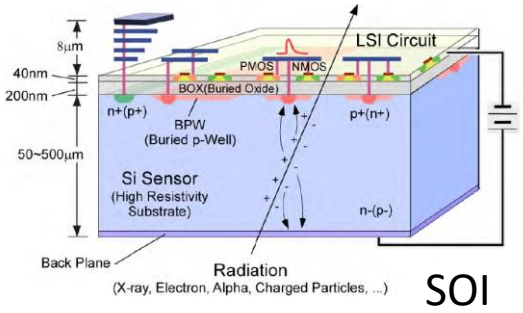



CMOS

- Motivations
- Current activities
- Future Plans




SOI

(SOI figures taken from Y. Arai presentations)

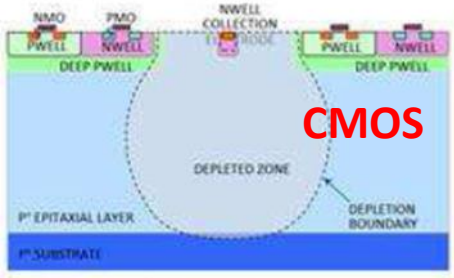
# Motivations

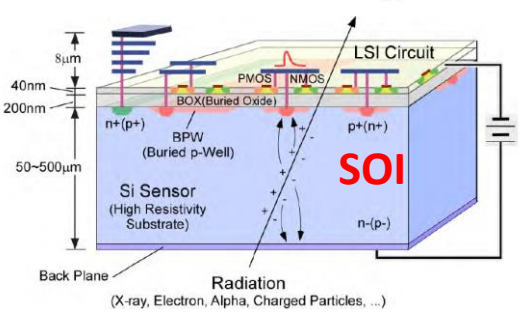
- Scientific target:
  - ✓ Vertex detector for future Higgs/top factories (ILC)
    - Physics program ⇨ Flavour tagging (b, c, τ), low momentum jets, jet charge determination.
    - High granularity needed
      - ($\sigma_{sp}$ ~ 3 μm) ⇨ pitch ~15-20 μm
    - Low material budget and low power consumption
      - (~0.1-0.3 %$X_0$/ layer and P ~ 20-50 mW/cm$^2$)
    - Time resolution of the order of 1 μs to cope with the beam background
      - Bunch tagging capabilities ?
  - ⇨ monolithic pixel detector technology

$$\sigma_b < 5 \oplus \frac{10}{p\beta \sin^{\frac{3}{2}}\theta}\ \mu m$$

- Framework of this application:
  - ✓ 2 suited technologies (CMOS & SOI) developped by the partners
    - Different levels of maturity and advantages ⇨ complementarity
  - ✓ Explore the possible synergies between the different technologies and know-how

✓ Most mature monolithic technology
✓ Widely used industrial process



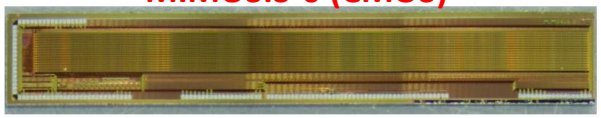



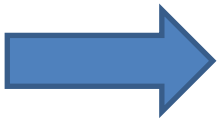

✓ High density layout
✓ 3-D vertical integration
✓ Radiation hardness

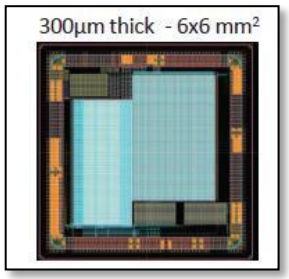
# Activity 1: CMOS to SOI translation

- MIMOSIS-0 @ IPHC (fabricated in 2019)
  - ✓ 1st Prototype developped for the CBM experiment program, based on ALPIDE (ALICE-ITS) architecture (⇨ demonstrator for Higgs factory)
    - Priority encoder read-out, $t_{r.o.}$~ 5 µs, $\sigma_{sp}$~ 5 µm
- **Idea:** Translation from CMOS 4-Well TJ (180nm) to SOI LAPIS (200nm)

MIMOSIS-0 (CMOS)





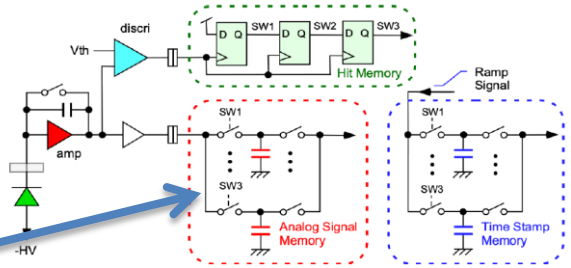



  - ✓ Mask issue ⇨ 2nd submission
  - ✓ **2 chips expected back from foundry in May 2021** (LAPIS 200 nm)
    - 1st: HEP applications ⇨ test Alpide/Mimosis-like pixels (FE), charge collection
    - 2nd: imaging ⇨ 192×128 pixels with rolling shutter or global shutter readout. Spectroscopic capabilities
  - ✓ Complementarity with SOFIST family (KEK)
  - ✓ **Digital library developped in cooperation with KEK**

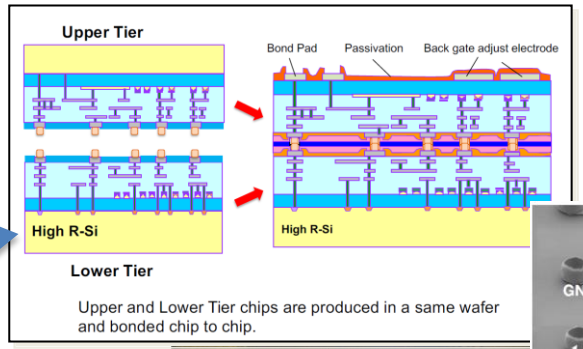
Architecture devpt. in CMOS ⇨ SOI: to be pursued

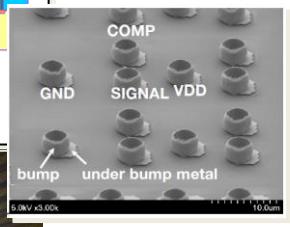
# Activity 2: SOI & SOFIST

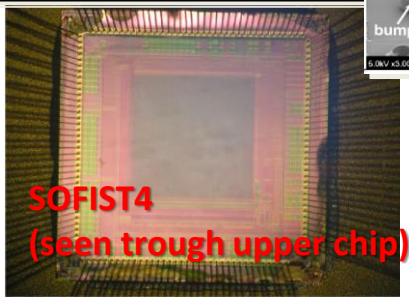
- SOIPIX @ KEK: SOFIST (SOI-LAPIS 200nm)
  - ✓ Target: development for ILC-ILD vertex and inner tracking detectors
- **Concept:**
  - ✓ ILC beam = 200 ms dead time between bunch trains
  - ✓ **Time stamp** & **analog charge** storage inside the pixel
  - ⇨ bunch timing
  - ✓ Challenge: power




- Last prototype: SOFIST-4
  - ✓ Privileged access to the T-Micron company
  - ✓ **Includes 3D integration technology**
    - **Allows smaller pitch 20 µm**
  - ✓ Promising results ⇨ Tests continuing

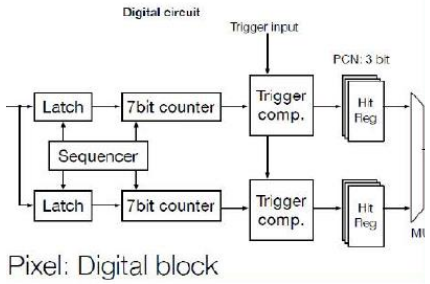



(SOI figures taken from Y. Arai presentations)

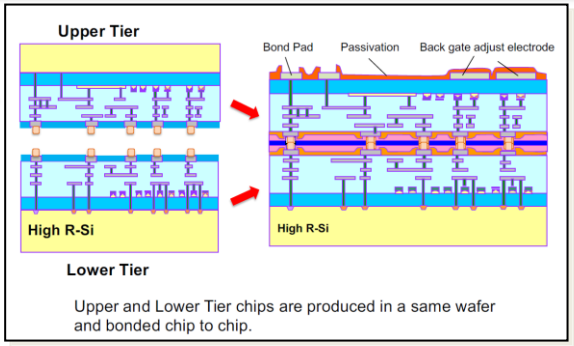
- Plans:
  - ✓ Dev. **Binary read-out** to mitigate Power
    - **from CMOS ALPIDE/MIMOSIS architecture**
    - Power mitigation
  - ✓ Exploration of a new concept
    - **Dual Timer Pixel** (DuTiP)
    - Idea: Store timing but can receive a trigger input
    - Multi-hit timing possible

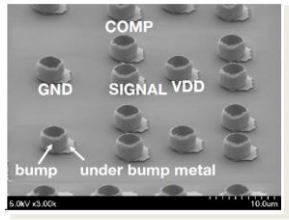


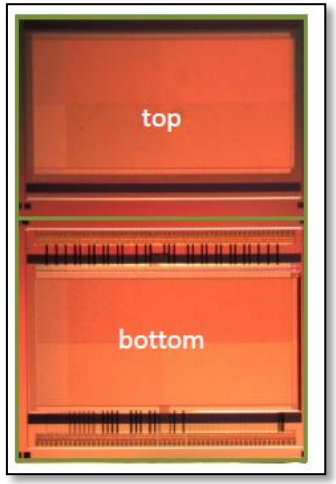

Devpt. of SOI: to be pursued

# Activity 3: CMOS & double-tier exploration

- **Idea:** Explore the Double-tier « 3D » in CMOS TJ 180nm (4-Well) technology
  - ✓ Bonding performed by T-micron
    - (same company used for SOFIST)
    - Bonding pitch = 10 µm.
    - Pitch = 20 µm
    - Both chips are sensitive + ouput logic in bottom chip
  - ✓ First try Issue: Unpassivation of pads not done properly
  - ✓ 2nd submission expected back from foundry ~ July 2021
- Goal: study
  - ✓ Direct read-out from bottom chip
  - ✓ **Read-out after transmission trough bonding from top chip**
    - Test capacitive noise between the 2 layers
    - Test pixel dispersion




3D stacking used in SOI ⇨ CMOS : to be pursued

# Summary & program

- R&D towards granular and thin pixel detectors
  - ✓ Target: ILC and beyond
    - CMOS & SOI technologies offer complementarity
  - ✓ Timescale of Higgs factories not precisely known (upgrades, etc.)
    - Final technology choices can be made only O(5) years before data taking
    - Need to continue to explore different technologies with different maturity/climax/advantages

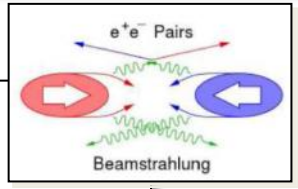
- Collaboration between partners
  - ✓ Fruitful synergies produced significant outcomes in both technologies
    - Cross-fertilization.
  - ✓ Access facilitation to CMOS, SOI and 3D-stacking pixel technology
  - ✓ Ground floor for future collaboration @ ILC
  - ⇨ Pursue/extend the current collaboration

- Request
  - ✓ Mainly travel expenses
    - ⇨ further develop. digital library, design reviews, etc.
      - e.g. Visit to Japan: M. Kachel (engineer) for 2 weeks

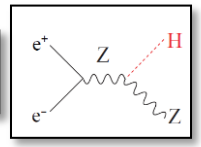
# Back up

# Vertex detector technology figure of merit

ILC, FCCee




e+e- requirements




Physics performances dominated

$e^+ \times e^-$

CMOS

Spatial resolution

R&D

Heavy ions experiments

Material budget

Power

Radiation hardness

Readout speed

$p \times p^{(-1)}$

Hybrid pixels

Running conditions dominated

FCC-hh

HL-LHC

- Heavy flavor tagging (b, c, τ)
- Low momentum tracking (pT ~ 100 MeV/c)
- Vertex/Jet charge determination

Spatial resolution
$\sigma_{sp}$ ~3 µm (pitch ~ 17 µm)

Material Budget
~ 0.15% $X_0$ / layer

Low occupancy

Impact parameter

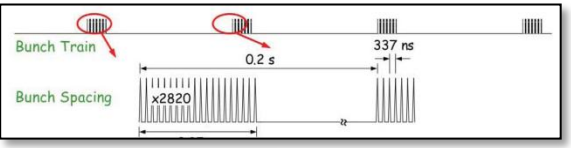
$$\sigma_b < 5 \oplus \frac{10}{p\beta \sin^{\frac{3}{2}}\theta} \ \mu m$$

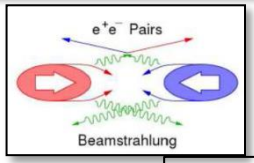
Time resolution
O(1-4 µs)

Challenge:

⇨Keep excellent spatial resolution, low material budget, moderate Power consumption and push towards better time resolution (BX)

# ILC VXD requirements




Physics (<Hz/cm²)

Beam background (~ 5 hits/BX/cm² on layer 0)

Beam background

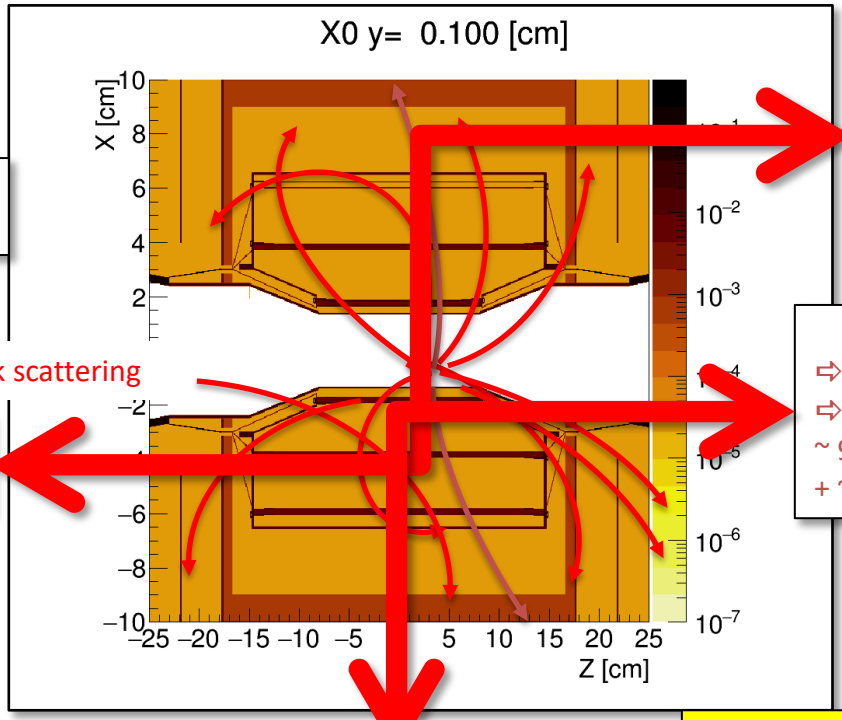
Radiation hardness
O(100kRad/yr) & O($10^{11}$)$n_{eq}$/yr

Rad.Tol. devices

Read-out speed
O(1-10 µs)

Power consumption
~< 50mW/cm²

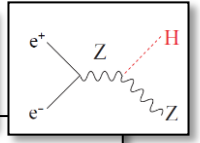
Fast read-out & low Power architectures




Back scattering

Cooling
Stiffness / Alignment

$$\sigma_b < 5 \oplus \frac{10}{p\beta \sin^{\frac{3}{2}}\theta}\ \mu m$$




Physics
⇨ Flavour tagging
⇨ Low pT tracks

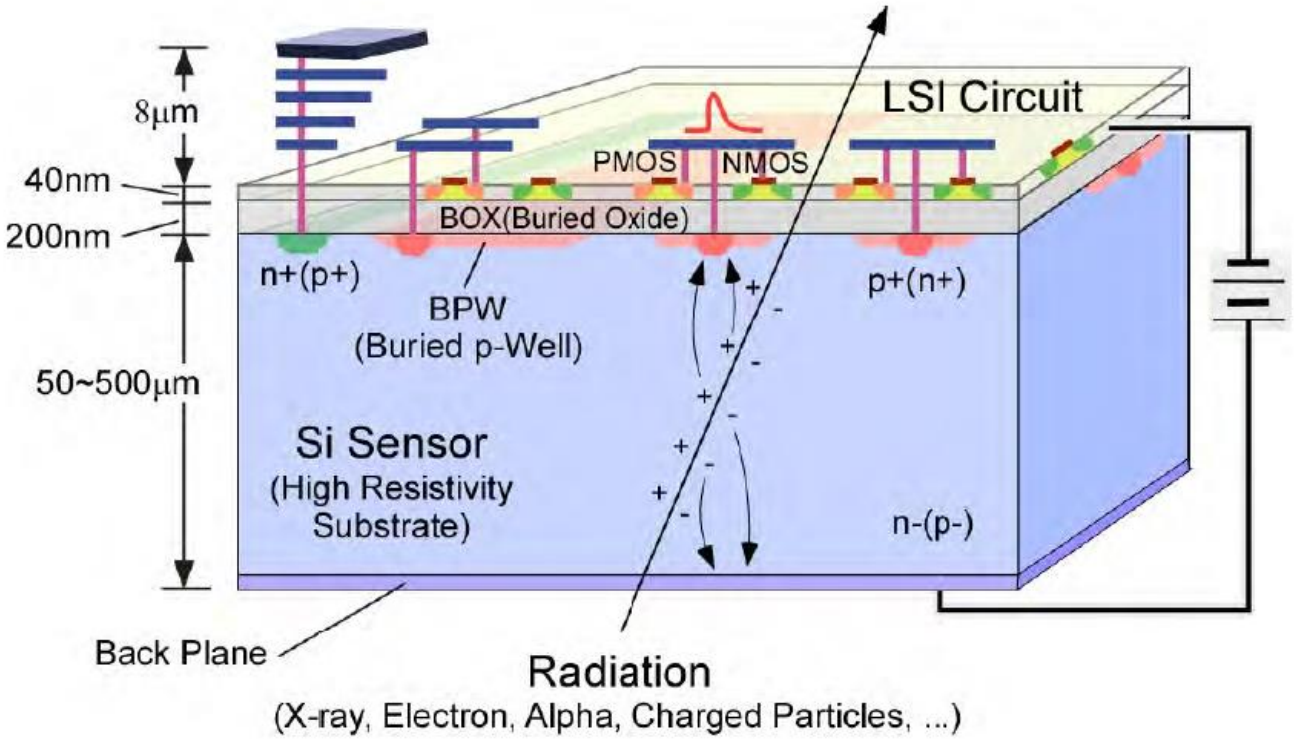
Vertex reconstruction
⇨ granularity
⇨ Pitch ~17 um
⇨ ($\sigma_{sp}$ ~3 um)

Material Budget
⇨ ~ 0.15% $X_0$ / layer
⇨ < 1% $X_0$ for the whole VTX
~ 900 µm Si
+ ~0.14% $X_0$ for the beam pipe

Low material detectors & supports structures

Challenge : meet the requirements all together

# II. SOI Pixel Technology




- Fully depleted sensor : Fast signal, Good S/N
- CMOS logics without well structure : High density layout
- The detector can be very thin : Low material budget.

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(slide taken from Y. Arai presentations)

# CMOS pixel sensor (CPS) for charged particle detection

- Main features
  - ✓ **Monolithic** (Signal created in low doped thin epitaxial layer ~10-30 µm)
  - ✓ Thermal diffusion of e- (Limited depleted region) + drift
  - ✓ Charge collection: N-Well diodes (Charge sharing)
  - ✓ Continuous charge collection (No dead time)
- Main advantages
  - ✓ **Granularity**
  - ✓ **Material budget**
  - ✓ Signal processing integrated in the sensor
    - Low signal & **Low Noise**
  - ✓ Flexible running conditions (Temperature, Power, Rad. Tol.)
  - ✓ **Industrial** mass production
    - Advantages on costs, yields, fast evolution of the technology,
    - Possible frequent submissions
- Main limitations
  - ✓ Industry addresses applications far from HEP experiments concerns
  - ✓ **Needs adapted processes**